The Trigger Readout Electronics for the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeters

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ABSTRACT: For the Phase-I luminosity upgrade of the LHC a higher granularity trigger readout of the ATLAS Liquid Argon (LAr) Calorimeters is foreseen to enhance the trigger feature extraction and background rejection. The new readout system digitizes the detector signals, grouped into 34000 so-called Super Cells, with 12bit precision at 40MHz and transfers the data on optical links to the digital processing system, which computes the Super Cell transverse energies. In this paper, development and test results of the new readout system are presented.

KEYWORDS: ATLAS Upgrade; Trigger; LTDB; Liquid Argon Calorimeters

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1. Introduction

The LHC upgrade is planned to enhance the instantaneous luminosity to $2\text{--}3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ during Run 3 from 2021 through 2023. The Phase-I upgrade of the trigger readout electronics for the ATLAS Liquid Argon (LAr) Calorimeters [1] will be installed on the ATLAS detector [2] during the second long shutdown of LHC in 2019/2020. In this upgrade, so-called Super Cells are introduced to provide higher granularity, higher resolution and longitudinal shower shape information from the LAr calorimeters to the Level-1 trigger processors [3]. The trigger energy resolution and efficiency will be improved for selecting electrons, photons, tau leptons, jets, and missing transverse momentum, while enhancing discrimination against pile-up. The readout of the trigger signals will process 34,000 Super Cells at every LHC bunch-crossing, frequency of 40 MHz, at 12-bit precision.

Figure 1. Example of an electron with 70 GeV of transverse energy in the existing Level-1 Calorimeter trigger electronics (left) and the upgraded trigger electronics (right). On the left, trigger towers sum the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. On the right, Super Cells provide information for each calorimeter layer for the full η range of the calorimeter, and finer segmentation ($\Delta\eta \times \Delta\phi = 0.025 \times 0.1$) in the front and middle layers of the EM calorimeter.

The improvement of granularity is shown in Figure 1, which compares the energy deposition of an electron in the existing trigger readout system to that of the upgraded system. The Super Cells will provide information for each layer of the calorimeter and a finer segmentation in the front and middle layer. The spatial granularity is thus improved by a factor of 10 compared to the existing Level-1 system.

Figure 2. The upgraded LAr trigger readout system architecture. The red outlines indicate the new components.

The architecture of the Phase-I trigger readout is shown in Figure 2 [4]. The original functionality of the Front-end Boards (FEBs) [5] is preserved so that the standard readout of the LAr Calorimeter cells and the legacy trigger system can be operated as before. New Layer Sum Boards (LSB) and new base planes are upgraded to replace the existing pieces, and new LAr Trigger Digitizer Boards (LTDB) will digitize the Super Cell signals and send processed data to the back-end electronics, where data are transmitted to the trigger processors. Each LTDB will process up to 320 Super Cell signals, which will be digitized by 12-bit ADCs on the LTDB. The output data connection of an LTDB consists of up to 40 optical fibers, each of which carries the data at 5.12 Gbps through a custom serializer and optical link to back-end LAr Digital Processing System (LDPS), which convert the samples to calibrated energies in real-time and interface to the FEX processors. With a total of 124 LTDBs in the system, the total rate to the back end electronics is approximately 25 Tbps.

2. The LAr Phase-I Demonstrator

A demonstrator system has been developed in the LHC long shutdown from 2013 to 2015 [6]. The demonstrator system that is about 1/60 of the full trigger readout consists of two LTDB demonstrators, two ATCA test board for Baseline Acquisition (ABBA) that used as digital

processing boards and receive the data from the LTDB demonstrators via optical links. These boards together with two new base planes were installed on ATLAS in summer 2014.

Measurements and data analysis have been done after the installation of the demonstrator system. Test results show that the observed noise level is consistent with noise levels in the current system. The demonstrator system successfully finished the data taking in 2015. These data are used to understand effect of pileup and to develop new filtering algorithm. The preliminary data analysis shows a good agreement for ATLAS main readout and ABBA readout. Now it restarted collecting data with start of LHC in May 2016.

3. Phase-I Front-End Electronics

Three key components are being developed to meet the requirements from the LAr Phase-I upgrade. The new LSB produces finer granularity Super Cell signals in the front and middle layers. The new base planes will allocate new slot(s) for the LTDBs, while keeping the other front-end electronics boards slots intact. The LTDB is the key electronics board to be built for the Phase-I upgrade. It will be responsible for the formation of the legacy layer sum signals as well as the digitization of Super Cell signals. Developments of these components are ongoing, and some of the prototypes are being tested. The design of LTDB is described in detail in the following subsections.

3.1 Radiation-Tolerant Custom ASICs for LTDB

The LAr front-end electronics will run in higher radiation levels in the upgraded LHC [7]. A radiation-tolerant custom 12-bit Nevis ADC [8] and a radiation-tolerant custom sterilizer LOCx2 [9] have been developed for LTDB.

The radiation-hard quad-channel 12-bit 40MS/s pipeline SAR Nevis ADC consists of four pipeline A/D channels with 12-bit resolution each. The sampling information derived from the rising edge of differential input SLVS 40MHz clock. The data is sent out serially using 320MHz DDR SLVS clock signaling. The ADC consumes around 43 mW per channel. It has I2C interface allows to control all internal functions of the chip. The final prototypes have been produced and tested on 64-ch LTDB prototype.

The LOCx2 consists of two channels and each channel encodes ADC data with an overhead of 14.3% and transmits serial data at 5.12 Gbps with a latency of less than 27.2 ns. LOCx2 is fabricated with a commercial 0.25- μ m Silicon-on-Sapphire CMOS technology. The power consumption of LOCx2 is around 843 mW. The early prototype has been tested on 64-ch LTDB prototype, and the final prototype is being tested.

3.2 LTDB pre-prototype

In order to evaluate technical and performance aspects, a pre-prototype board has been developed with commercial FPGAs and radiation-tolerant custom ASIC Nevis ADC and optical transmitter MTx. As shown in Figure 3, the pre-prototype consists of analog section, digital section and power section. The analog section provides the appropriate gain, shaping, offset and common mode. The digital section digitizes the analog signals and send processed data to back-end electronics. The digital section has 10 Artix-7 FPGA, 80 Nevis ADCs, 20 MTx modules and 2 GBTx for data processing, clock distribution, slow control and monitoring. The power section is designed as a mezzanine and provides proper power supply.

Evaluation tests of digital section have been done and results show the digital section work properly. All optical links ran a long time for link speed test at 4.8Gbps, the estimated

BER is better than 10^{-15} and good eye openings were obtained. It is confident that the LTDB pre-prototype is stable and it is ready for the performance test.

Figure 3. Assembled LTDB pre-prototype (left) and test setup (right).

3.3 64-ch LTDB Prototype

While the custom ASICs are being designed, an LTDB 64-channel test board has been developed to verify the design and to exercise the radiation-tolerant custom ASICs. The board is 1/5 of the LTDB prototype and will process 64 Super Cell signals. As shown in Figure 4, there are 16 custom 12-bit ADCs and 4 custom LOCx2 devices to interface with the ADC. There are also 4 custom MTx dual channel optical transmitters to transmit the data to the LDPB, 1 GBTx, 1 GBT-SCA and 1 MTRx to configure on-board devices, control the power supply and monitor the voltage, current and board temperature.

Figure 4. Assembled 64-ch LTDB prototype (left) and test setup (right)

The performance tests have been done, as shown in Figure 5. The RMS of ADC noise is less than 1 ADC count. ADC output values as a function of calibration pulse amplitude, which shows the dynamic range of the analog chain upstream of the ADC. The linear region of such plots can be used to evaluate the non-linearity of the system. In figure 5, the Non-linearity is around 0.12%. Crosstalk between two channels in same and neighbor is also measured. The maximum crosstalk is around 0.1%.

Figure 5. Noise (left) and Non-linearity (right) measurement of ADC

4. Phase-I Back-End Electronics

The LTDB sends data to back-end electronics LAr Digital Processing System (LDPS). It receives 12 bits ADC data from the LTDBs at 5.12 Gbps/fiber, extract the transverse energy for each Super Cell every 25 ns, and transmit these data to the Level-1 calorimeter trigger system (L1Calo) at 9.6/11.2/12.8 Gbps. There're two key elements in LDPS, one is LAr Trigger prOcessing Mezzanine (LATOME), and the other one is LAr Carrier (LArC).

Figure 6. Assembled LATOME.

The LATOME is an AMC mezzanine card, as shown in Figure 6. It has one ARRIA-10 FPGA, 8 MicroPods and 2 Gbits DDR3 SDRAM. The FPGA processes received data and send it out through optical links. The DDR3 SDRAM is used for data buffering. The LATOME has been fully tested and the board works as expected. It supports various optical link speeds (6.4, 9.6, 11.2 and 12.8 Gbps) for different applications.

Figure 7. Picture of assembled LArC and RTM

The LArC is an ATCA carrier board, as shown in Figure 7. Each LArC holds four LATOMEs and provides a variety of different communication functionalities. It's a challenge to achieve a reliable high rate of transmission for clock distribution and data rates at 10GbE on large ATCA boards. The integration tests with LATOME have been successfully done. The baseline link speed of 11.2Gbps has been agreed upon.

5. Conclusion

To improve the Level-1 trigger performance for all the objects involving the LAr calorimeters, a new trigger readout system for the Phase-I upgrade of the ATLAS LAr Calorimeters is being designed. A demonstrator system has been installed on the ATLAS detector. Preliminary data analysis shows a good agreement for ATLAS main readout and demonstrator readout. Based on the demonstrator system, further prototypes for the trigger readout system with radiation-tolerant custom ASICs are being developed and tested. The full integration of the trigger readout system for the Phase-I upgrade of the ATLAS LAr Calorimeters will take place in 2017.

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