ATLAS Trigger and Data Acquisition Upgrades for High Luminosity LHC

CHEP 2016, San Francisco (USA), 10-14 October 2016

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On behalf of the ATLAS Collaboration
High Luminosity LHC

Latest LHC long term schedule

PHASE I


- LS1: splice consolidation button collimators R2E project
- EYETS
- LS2: injector upgrade cryo Point 4 Civil Eng. P1-P5

30 fb⁻¹

150 fb⁻¹

300 fb⁻¹

PHASE II

2024 2025 2026 2027

- LS3: HL-LHC installation

3000 fb⁻¹

7 TeV 8 TeV 13-14 TeV

75% nominal luminosity

nominal luminosity

2 x nominal luminosity

radius damage

energy

TDAQ Phase-I: Construction

Commissioning & Integration

Maintenance & Operations

TDAQ Phase-II: R&D

Construction

Commissioning & Integration

Maintenance & Operations

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ATLAS upgrade for High Luminosity LHC

- Motivation: high luminosity $\Rightarrow$ high pile up*, increased radiation and readout bandwidth
- New Inner TracKer – silicon strips and pixels
- New Trigger & Data AcQuisition system
- Upgraded calorimeter and muon detectors
- Upgraded computing and software

* Multiple interactions per bunch crossing
TDAQ System Design
Overview of one of the two design options

- Level-0 Muon & Calo used to make initial fast rejection and identify Regions of Interest
- Level-1 hardware track trigger and high resolution calo data provide further rejection
- DAQ comprises readout, regional requests, data handling and storage
- Storage Handler decouples Event Filter from DAQ so it can work continuously, between fills
- Event Filter combines commodity processor farm and hardware tracking
Trigger strategy for HL upgrade

- High rate of low threshold inclusive single lepton triggers to maximize electroweak physics. Higher thresholds would significantly limit physics potential.
- Lower rate triggers for multiple low-\(p_T\) leptons, taus, jets and missing transverse energy
- Robustness against pileup through early use of high granularity calorimeter information and hardware tracking
- Upgrades to improve muon efficiency
- Trigger as close as possible to offline selection, to improve efficiency and minimise systematics
- Note: Level-1 rates projected to HL far exceed 100 kHz limit of Run 3 system

Estimated rates and thresholds for architectures described on following pages

| Item                  | Offline \(p_T\) Threshold [GeV] | Offline \(|\eta|\) | L0 Rate [kHz] | L1 Rate [kHz] | EF Rate [kHz] |
|-----------------------|--------------------------------|-----------------|---------------|---------------|---------------|
| isolated single \(e\) | 22                             | < 2.5           | 200           | 40            | 2.20          |
| forward \(e\)         | 35                             | 2.4 – 4.0       | 40            | 8             | 0.23          |
| single \(\gamma\)     | 120                            | < 2.4           | 66            | 33            | 0.27          |
| single \(\mu\)        | 20                             | < 2.4           | 40            | 40            | 2.20          |
| di-\(\gamma\)         | 25                             | < 2.4           | 8             | 4             | 0.18          |
| di-\(e\)              | 15                             | < 2.5           | 90            | 10            | 0.08          |
| di-\(\mu\)            | 11                             | < 2.4           | 20            | 20            | 0.25          |
| \(e - \mu\)           | 15                             | < 2.4           | 65            | 10            | 0.08          |
| single \(\tau\)       | 150                            | < 2.5           | 20            | 10            | 0.13          |
| di-\(\tau\)           | 40,30                          | < 2.5           | 200           | 30            | 0.08          |
| single jet            | 180                            | < 3.2           | 60            | 30            | 0.60*         |
| large-\(R\) jet       | 375                            | < 3.2           | 35            | 20            | 0.35*         |
| four-jet              | 75                             | < 3.2           | 50            | 25            | 0.50*         |
| \(H_T\)               | 500                            | < 3.2           | 60            | 30            | 0.60*         |
| \(E_T^{miss}\)        | 200                            | < 4.9           | 50            | 25            | 0.50*         |
| jet + \(E_T^{miss}\)  | 140,125                        | < 4.9           | 60            | 30            | 0.30*         |
| forward jet\(^{*}\)   | 180                            | 3.2 - 4.9       | 30            | 15            | 0.30*         |

Total: \(\sim 1000\) \(\sim 400\) \(\sim 10\)

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ATLAS Phase-II Upgrade Scoping Document CERN-LHCC-2015-020
Level-0 Trigger

- **L0 Calo**
  - Coarse calorimeter data sent to three feature extractors (em/tau, jet and global) to find different types of trigger objects (TOBs)
  - Firmware upgrade; largely same hardware as Run 3

- **L0 Muon**
  - New readout and improved coverage to increase efficiency
  - Latency now long enough to use precision MDTs for sharper turn on

- **“L0Topo/CTP/RoIEngine”**
  - Receives trigger objects from L0 Calo and L0 Muon
  - Performs complex trigger selections (invariant mass, missing transverse energy, etc.) and applies the L0 trigger menu
  - On L0 Accept, the RoIEngine calculates the Regional Readout Requests (R3) to send back to the detectors via FELIX
  - RoIs cover at most 10% of detector => 100 kHz equivalent rate for readout
Level-1 Trigger

**L1Global**
- Low latency aggregation network for calo data; time multiplexed event processing in FPGA/GPU
- Process finer-grained calo information using all cells to improve $e$, $\gamma$, $\tau$, jets, $E_T^{\text{miss}}$
- Combine refined calo objects and L0 muons with tracks from **L1Track**
- Make topological combinations

**L1Track:**
- Hardware tracking using AM chips to match data to patterns
- Finds tracks with $p_T > 4$ GeV in RoIs at 1 MHz
- For electron identification and to reduce the pileup background to multi-object events

See talk by B Allbrooke
Level-0-only option

- L1 hardware trigger and RoI Engine relocated to EF hardware & software
  - Consequently no major EF CPU increase
- Readout less complex but less flexible
- DAQ scaled for 1 MHz readout from all detectors
- Also looking at L0+L1 option in which lower latency is traded for higher L0 accept rate
Data Acquisition

• **Trends from custom to commodity hardware, and hardware to software**

• **Front End Link eXchange (FELIX)**
  - Routes between custom serial links and commodity multi-gigabit networks
  - Building on initial use in Phase-I

• **Data Handler**
  - Detector-specific data processing and monitoring.
  - Software toolkit and commodity computers replace custom hardware & firmware

• **Event Builder**
  - May be logical or physical
  - Data compression drives resources

• **Storage Handler**
  - Decouples Event Filter from DAQ so **EF can work continuously, between fills**
  - Requires storage volume of the order of **50 PB**, able to concurrently receive and serve a few TB/s

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High Level Trigger CPU and software evolution

<table>
<thead>
<tr>
<th>LHC Run 1</th>
<th>LS1</th>
<th>LHC Run 2</th>
<th>LS2</th>
<th>Run 3</th>
<th>LS3</th>
<th>Run 4 HL</th>
</tr>
</thead>
<tbody>
<tr>
<td>2023</td>
<td>2024</td>
<td>2025</td>
<td>2026</td>
<td>2027</td>
<td>2028</td>
<td>2029</td>
</tr>
</tbody>
</table>

**Commodity CPUs**
- 8-12 cores e.g. E5540, E5420, X5660
- 12-24 cores e.g. E5-2680v3
- 24+ cores Co-processors?

**Event processing**
- Multiple independent processes
- Offline algorithms wrapped
- Multi-processes with shared memory
- Offline algorithms wrapped
- Multi-thread, multiple events in flight
- Seamless integration of offline algorithms
- Multi-thread, multiple events in flight
- More thread-safety, parallelism, optimisation

**PHASE I**
- Multi-threading, multiple events in flight
- Offline algorithms wrapped

**PHASE II**
- Many cores? Hardware accelerators?
- 24+ cores Co-processors?

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See talks by B Wynne, P Conde Muino
Event Filter: tracking expected to dominate CPU time

- Software/hardware hybrid solution
- Software for seeded precision tracking in RoIs
- Hardware for unseeded tracking
  - \textbf{FTK++}: AM chips, same board as L1Track
  - $p_T > 1$ GeV, for pileup suppression, b-tagging, $E_T^{\text{miss}}$, jet calibration, etc.
- Also studying
  - Hardware/software interplay
  - Software algorithms, parallelisation
  - Use of other hardware accelerators, e.g. GPUs

\textbf{Current approach does not scale}

\textbf{ATLAS Simulation}
Monte Carlo $t\bar{t}$ events $\sqrt{s} = 14$ TeV
2016 Online software

\textbf{Online beamspot algorithm}

\textbf{CPU time [ms]}

\textbf{pileup interaction multiplicity}
Summary & conclusions

- ATLAS has a TDAQ design to meet the challenges of HL-LHC
- Two-level hardware trigger based on Regions of Interest, also a single level option.
- Hardware tracking in L1 and EF used to tackle high pileup
- Trend in DAQ from custom hardware to commodity hardware and software
- Baseline will be documented in a TDR, due around the end of 2017
Backup material
HL-LHC physics motivation

- Studies of the light Higgs boson require precision at electroweak scale.
- Precision measurement of Higgs couplings are a window into new physics (including much higher mass scales than the LHC).
- Searches for physics Beyond the Standard Model (BSM) may require low cross section processes with large backgrounds, e.g. SUSY.
- Subtle BSM physics can only be found if the SM is well understood.
- European Strategy report (ECFA), P5 (DOE/NSF): HL-LHC needs at least 3000 fb$^{-1}$ (10 years at $\mathcal{L} = 7.5 \times 10^{34}$ cm$^{-2}$s$^{-1}$).
Motivation: Limitations of Run 3 TDAQ system at HL

<table>
<thead>
<tr>
<th>Item</th>
<th>Run 1 Offline $p_T$ Threshold [GeV]</th>
<th>Run 3 Level-1 system performance at $L = 7.5 \times 10^{34}$ cm$^{-2}$ s$^{-1}$</th>
<th>Level-1 Rate [kHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>isolated Single $e$</td>
<td>25</td>
<td>22</td>
<td>200</td>
</tr>
<tr>
<td>single $\mu$</td>
<td>25</td>
<td>20</td>
<td>80</td>
</tr>
<tr>
<td>di-$\gamma$</td>
<td>25</td>
<td>25</td>
<td>8</td>
</tr>
<tr>
<td>di-$e$</td>
<td>17</td>
<td>15</td>
<td>90</td>
</tr>
<tr>
<td>di-$\mu$</td>
<td>12</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>$e - \mu$</td>
<td>17.6</td>
<td>17,12</td>
<td>8</td>
</tr>
<tr>
<td>single $\tau$</td>
<td>100</td>
<td>150</td>
<td>20</td>
</tr>
<tr>
<td>di-$\tau$</td>
<td>40,30</td>
<td>40,30</td>
<td>200</td>
</tr>
<tr>
<td>single jet</td>
<td>200</td>
<td>180</td>
<td>60</td>
</tr>
<tr>
<td>four-jet</td>
<td>55</td>
<td>75</td>
<td>50</td>
</tr>
<tr>
<td>$E_T^{miss}$</td>
<td>120</td>
<td>200</td>
<td>50</td>
</tr>
<tr>
<td>jet + $E_T^{miss}$</td>
<td>150,120</td>
<td>140,125</td>
<td>60</td>
</tr>
</tbody>
</table>

Level-1 rates projected to HL far exceed 100 kHz limit of Run 3 system.

Without upgrade, higher thresholds significantly curtail physics potential.
Upgrade motivation: computing evolution

Shift away from clock speed scaling to increasing numbers of cores and other parallel processing features.

Commoditisation of co-processors/accelerators.

Evolution in programming paradigms, tools and libraries.

Computing models and software must adapt.

Gaudi/Athena design year ~2000

Charles Leggett, LBL
Read Out architecture

Front End LInk eXchange (FELIX), routes between **custom serial links** and **commodity multi-gigabit networks**

Data Handler

For detector-specific data processing and monitoring. Software toolkit and commodity computers replace custom hardware & firmware