Differential Phase Detector for Precise Phase Alignment

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Abstract—This paper presents a differential phase detector circuit, whose phase-to-voltage characteristic has an extremum when its two input signals are exactly in phase. In this condition all its digital signals are of 50 % duty cycle so that the circuit characteristic does not have a dead zone. This feature allows a precise indication of the zero-phase condition, which is independent of the detector power supply and the offset of its ADC readout. Such a detector is used for a phase alignment of two reference clock signals with frequency about 11 kHz in front-ends processing signals from beam position monitors of the Large Hadron Collider (LHC) at CERN. The detector output voltage is digitized with a 24-bit ADC at the rate of the reference signals. The resulting samples are processed in the front-end FPGA and transmitted to the control system using an Ethernet data stream. After a detailed description of the differential phase detector its performance is demonstrated with laboratory measurements. The results show that this simple circuit allows a phase alignment resolution of the 11.2 kHz clock signals in the order of 0.0001 ° with a measurement bandwidth of 1 Hz.

Keywords—phase detector; precise phase alignment; zero-phase detection; phase detector dead zone

I. INTRODUCTION

The presented differential phase detector is used in so called Diode ORbit and OScillation (DOROS) system, designed for processing signals from beam position monitors of the Large Hadron Collider (LHC). One of the functionalities of the DOROS system requires a precise synchronisation of the phase of the ADC sampling clock to the reference phase of the particle beam circulating in the LHC [1, 2]. The required alignment accuracy is in the order of 0.001 °, that is some 3 parts per million (ppm) of the period of the phase detector input signals, corresponding to some 0.25 ns at the detector operational frequency f_{PD} of about 11.2 kHz. Such phase is too small to be measured in a DOROS front-end by classical counting techniques, as the fastest system clock frequency is 160 MHz allowing to resolve only phase differences corresponding to more than 6.25 ns. Therefore the feasibility of building an analogue phase detector achieving the required phase alignment was studied. In DOROS front-ends 24-bit 8-channel ADCs are used and one of their free channels is dedicated for reading-out the phase detector output. With digital low-pass filtering down to 1 Hz the ADCs have enough resolution to resolve signal changes at the ppm level, sufficient for achieving the required

phase measurement resolution. The offset voltages of the ADC inputs are however much larger, in the order of 50 ppm of the ADC full scale, which would introduce by far too large error if the phase alignment was indicated by an absolute signal level. This limitation could be overcome by using a phase detector having an extremum output voltage when the two input signals are fully aligned. The classical phase detector with XOR gate was rejected, as working with very short output pulses for very small phase differences, resulting in a dead zone [3]. In this paper a novel architecture of a differential phase detector is proposed, composed of two phase detectors with complementary outputs. When the input signals are exactly in phase all digital waveforms of the circuit are of 50 % duty cycle. This very interesting feature makes the detector free from the dead zone problem in the most important part of its characteristic. The simplicity of the final circuit, its interesting properties and achieved parameters encouraged the authors to publish its detailed description along with laboratory measurements documenting its performance.

II. THE PHASE DETECTOR PRINCIPLE

The diagram in Fig. 1 shows schematically the differential phase detector (DPD) circuit along with simplified signals in its most important nodes. Both input signals are assumed to be square waves with 50 % duty cycle and equal periods T . The time difference between the respective signal edges, denoted as τ , can change from $-T/2$ to $T/2$, however the circuit is designed to operate for $\tau \approx 0$. The NOR gate converts the time delay τ into duty cycle of the output signal. The signal is low-pass filtered, resulting in the average voltage V_{NOR} changing linearly with τ as:

$$V_{NOR} = V_{PS} \left(\frac{1}{2} - \frac{|\tau|}{T} \right) \quad (1)$$

where V_{PS} is the power supply of the gate. It is assumed that the gate output voltage is either 0 or V_{PS} , well approximated in practice by modern CMOS gates, especially when the low-pass (LP) filter has a high-impedance input.

Identical processing is performed with the OR gate, yielding the low-pass filtered voltage V_{OR} :

$$V_{OR} = V_{PS} \left(\frac{1}{2} + \frac{|\tau|}{T} \right) \quad (2)$$

Please note that voltages V_{NOR} and V_{OR} have respectively a minimum and a maximum when both input signals are exactly in phase, i.e. $\tau=0$, and they have the same amplitude, as at this condition the output signals of the NOR and OR gates have equal 50 % duty cycles. The V_{NOR} and V_{OR} voltages are then subtracted resulting in the output voltage V_D :

$$V_D = \pm 2V_{PS} \frac{|\tau|}{T} \quad (3)$$

The voltage equals zero when both input signals are exactly in phase and it is a minimum when subtracting V_{NOR} from V_{OR} or maximum when subtracting V_{OR} from V_{NOR} . The advantage of the differential phase signal V_D is that its extremum is equal zero and therefore it is independent of the power supply voltage, contrary to the “single-ended” voltages V_{NOR} and V_{OR} .

III. IMPLEMENTATION

Simplified schematic of the implementation of the DPD in the DOROS front-ends is shown in Fig. 2.

The 50 % duty cycle of the phase detector input signals is guaranteed by the two D flip-flops operating as simple frequency dividers. The detector operates at half of the input frequency, therefore its phase-to-voltage characteristic has twice smaller slope. The frequency dividers can be synchronised to operate in-phase using asynchronous reset inputs of the flip-flops (not shown on the schematic).

The OR and NOR functions of equal propagation time are implemented as a single OR gate and two EX-OR gates, one operating as an inverter and one as a buffer. The low-pass filters, identical for both circuit branches, are built as three simple RC sections. The subtraction is done by a circuit with two operational amplifiers in the configuration with the signal maximum for $\tau=0$. The dynamic range of the ADC is $[0, 2 V_{ref}]$, therefore the circuit adds V_{ref} to operate in the middle of the ADC dynamic range. The circuit amplifies the phase signal by factor 2, compensating the sensitivity loss caused by the input flip-flops.

The circuit output voltage is

$$V_O = V_{ref} - 2V_{PS} \frac{|\tau|}{T} \quad (4)$$

Fig. 2. Simplified schematic of the implementation of the differential phase detector in the DOROS system.

Fig. 1. Block diagram of the differential phase detector and simplified signals in its most important nodes.

It is converted by the ADC with the full scale of $2 V_{ref}$ into normalised digital signal S_O changing from 0 to 1:

$$S_O = \frac{1}{2} - \frac{V_{PS}}{V_{ref}} \frac{|\tau|}{T} \quad (5)$$

For $\tau=0$ the ADC signal $S_0=0.5$ and it is independent of the gates power supply V_{PS} (about 3.3 V) and the reference voltage V_{ref} (very close to 2.5 V). These voltages set only the slope of the phase-to-voltage characteristic, whose actual value is not important for the precise phase alignment. The feature is very important for the final achieved performance of the circuit.

A lot of attention was paid to achieve as good symmetry as possible of the both branches of the circuit. The input flip-flops are part of one chip, similarly the EX-OR gates and the operational amplifiers. To minimise drifts the circuit uses precision operational amplifiers and passive components with

good thermal stability. To minimise temperature gradients, the DOROS front-ends are built as 19" 1U thermally optimised cases with thick aluminium walls. A photo of the front-end unit in a laboratory test setup is shown in Fig. 3. The power dissipation is maintained at the level allowing reliable operation without internal fans, which would introduce temperature fluctuations perturbing operation of circuits relying on fine compensation of thermal drifts. Whenever needed, the temperature of a DOROS front-end can be lowered by blowing air next to the large external surfaces. This way one avoids temperature fluctuations inside the units, which are by far more perturbing than common slow temperature drifts.

IV. MEASUREMENTS

The performance of the DPD was measured in a laboratory. Changes of the detector output signal upon shifting the delay between the input signals in 1 ns steps are shown in Fig. 4, each step lasting about 10 s. The plot left axis is scaled in ppm of the ADC full scale (FS) and the right axis in the corresponding nanoseconds calculated from (5) for $V_{PS}=3.3$ V, $V_{ref}=2.5$ V and $T=89.3$ μ s. The used 1 ns steps are very clean as seen on the detector output, in spite of the fact that each of them corresponds to the change of about 11 ppm of the ADC full scale of 5 V, that is some 55 μ V.

From the asymmetry of the amplitude steps next to the characteristic maximum it can be concluded that the true maximum was slightly missed. It is interesting that the steps further from the maximum do not have the expected equal amplitudes. The effect is better seen in Fig. 5, showing the detector output signal around the maximum. In blue it is shown the same measurement as in Fig. 4 and in red the corresponding characteristic but measured with the delay between the detector input signals changing in the other direction. Both characteristics superimpose quite well, with the largest differences on the slopes defined by the first order IIR filter used to filter the ADC samples. The IIR filter cut-off frequency for all presented measurements was 1 Hz. It can be seen that for the steps between 117 and 127 s both measurements show more noise than for other steps. This phenomenon and the curious characteristic steps with uneven amplitudes are still under investigation. It is not yet known whether the observed effects are caused by the DPD itself or rather by some imperfections in the generation of its phase-shifted input signals done in the DOROS system FPGA. The effects are however not critical for the DPD application in the DOROS system. It is seen that the achieved phase resolution is larger than 0.1 ns, corresponding to about 0.0004° at 11.2 kHz, the frequency at which the DPD operates in the DOROS system. Such resolution is by far enough for phase alignment in the DOROS system.

The long term stability of the DPD was measured in a zero-phase condition achieved by connecting both DPD inputs to the same signal. The DOROS DPD circuit is accommodated on a digitizer board, which hosts also a multichannel ADC, whose one channel processes the DPD signal. The board is equipped with a temperature sensor chip for monitoring the average temperature of the board. A single DOROS unit contains two such digitiser boards and during the discussed measurements the DPD of each of them was examined.

Fig. 3. A photograph of the setup used for measurements discussed in the paper. The DOROS front-end is put between two 1U ventilation units. The upper ventilation unit was used for additional cooling forcing temperature changes.

Fig. 4. Differential phase detector signal digitised when the delay between the input signals was changed in 1 ns steps. The left vertical axis is in ppm of the ADC full scale (FS), while the right one is in the corresponding nanoseconds calculated from (5).

Fig. 5. In blue is the part of the characteristic in the above Fig. 4 zoomed around the maximum. The characteristic in red was measured with the phase changing in the opposite direction. The time of both measurements is adjusted for the best overlap.

Long-term stability of both DPDs was measured over 8 hours along with their response to a forced temperature change, applied approximately in the middle of the measurement. The temperature change was induced by switching on both fans of the top ventilation unit shown in Fig. 3, blowing the air above the closed DOROS unit. The resulting DPD signals with measured average board temperatures are shown in Fig. 6.

It can be seen that during the first 4 hours of the measurement when the temperatures of each board was quite stable the signals of both DPDs were fluctuating by some 0.4 ppmFS of the ADC full scale (ppmFS). This amplitude corresponds to some 30 ps, which is equivalent to the phase of about 0.00012° at 11.2 kHz. The forced temperature drop of approximately 3°C caused the changes in the DPD output signals by some 0.8 ppmFS for DPD 1 and 0.2 ppmFS for DPD 2, respectively, corresponding to the delay of 60 ps and 15 ps. The 8 hour measurement was repeated with the positions of the PCBs in the DOROS unit exchanged. This resulted in the corresponding exchange of the results, indicating that the measured DPD temperature responses are linked to the thermal parameters of the electronic components used in each DPD, rather than the cooling properties of the DOROS chassis. Reproducibility of the measurements was confirmed by repeating them several times.

It is interesting that the observed thermal sensitivity of the worse DPD 1 with the value in order of $1.5 \mu\text{V}/^\circ\text{C}$ can be fully explained just by the thermal stability of the ADC, as its datasheet typical offset drift is $0.8 \mu\text{V}/^\circ\text{C}$ and the gain drift in the middle of the input range is $3 \mu\text{V}/^\circ\text{C}$. Please note that the observed drift is also influenced by the ADC reference ($1 \mu\text{V}/^\circ\text{C}$), the operational amplifiers ($0.2 \mu\text{V}/^\circ\text{C}$) and their resistors ($25 \text{ ppm}/^\circ\text{C}$).

It was noticed that the performance of the DPD was changing once the DOROS front-end case was open. The effect was investigated in more detail, with the results shown in Fig. 7. The plots show a sequence of 5 measurements, each lasting about 15 minutes, when the front-end case was alternated between being covered with the top plate and open. It was observed that once the case is open, the DPD noise increased from 0.4 ppmFS to some 2.2 ppmFS for the worse DPD 2, that is by more than 5 times. The noise returns to its previous value right after the case is again closed. When the case was open for the second time the air flow was forced by the fans from the top ventilation unit installed as in the setup shown in Fig. 3. This time the DPD 2 noise increased even more, by a factor of 21, reaching some 8.6 ppmFS. The measurements indicate that the DPD and its related circuits work the best if they are enclosed and not exposed to air flows. This observation should be taken into account if the DPD is supposed to work with its best resolution.

V. CONCLUSIONS

The differential phase detector presented in this paper is a simple circuit designed for precise phase alignment of two signals of the same frequency. The detector output signal has an extremum when the two input signals are exactly in phase. In this condition all detector digital signals have 50 % duty-cycle, making its operation free of the dead zone problem. The detector differential architecture is crucial to achieve high accuracy and long term stability.

Fig. 6. Output signals of two differential phase detectors (DPDs) as digitised by their ADCs when the inputs of each DPD were receiving the same signal. The upper plot shows the temperatures of the boards accommodating the DPDs. The temperature change in the middle of the measurement was forced by switching on the upper ventilation unit seen in the setup of Fig.3.

Fig. 7. Output signals of two differential phase detectors (DPDs) as digitised by their ADC when both detector inputs were driven by the same signal. The changes in temperature were caused by opening and closing the front-end (FE) case cover. When the cover was raised for the second time the air flow was forced by the fans from the top ventilation unit installed as in the setup shown in Fig. 3. The upper plot shows the temperatures of the boards accommodating the DPDs.

The practical implementation of the detector in the DOROS system was discussed. The detector is built with three fast CMOS logic chips, two precision operational amplifiers and several passive components with good thermal stability. The detector output voltage is read by a 24-bit ADC and its samples are processed in the DOROS system FPGA.

The presented laboratory measurements show that the achieved phase resolution and one hour stability of the DOROS differential phase detector is in the order of 0.0001° for operation at 11.2 kHz and ADC samples low-pass filtered to 1 Hz. The presented differential phase detector may be interesting for applications in systems where available clock frequencies are not sufficient for digital phase measurement assuring signal phase alignment with sufficient resolution.

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