The Compact Muon Solenoid Experiment

Conference Report

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Upgrades to the CMS Cathode Strip Chamber Electronics for HL-LHC

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Abstract

Cathode strip chambers (CSCs) are used to detect muons in the end cap region of the CMS detector. The chambers are arranged in rings in four planes on each end of the detector. The inner rings of CSCs in each station have the highest flux of particles and this presents challenges to efficient readout at the luminosity, latency, and trigger rate foreseen at the HL-LHC. The existing front end electronics in Stations 2, 3, and 4 are based on switched capacitor arrays with limited buffering capability. Queuing models have shown that significant saturation of the buffers would occur for the luminosity, Level 1 trigger rates, and required Level 1 latency for running at the HL-LHC. In addition, the expected output rate of data is expected to exceed the 1 Gbps bandwidth of the optical links that carry data to the back end, resulting in loss of event synchronization. The upgrade of the inner ring of CSCs addresses these problems by replacing some types of electronics boards in these rings with upgraded boards. In particular, the existing cathode front end boards on the inner rings of Stations 2, 3, and 4 will be replaced with new digital cathode front end boards. These boards follow the design of those installed in the inner ring of Station 1 in the recent long shutdown of the LHC. The boards use flash ADCs and digital pipelines in place of the switch capacitor arrays used previously. The digital pipeline results in nearly deadtimeless operation and the capability to accommodate long latency requirements without loss of data. Also, new DAQ motherboards will be designed with optical output links with higher bandwidth to accept the higher data rate. Finally, the FED system, which is the interface between the CSCs and the central DAQ of the CMS experiment, will be replaced with a system that can receive the higher input rates. We present the measurements and calculations that predict the behavior of the CSC electronics under HL-LHC conditions. We describe the design of the electronics systems for the upgrade and show studies of expected performance.

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David M. Morse, on behalf of the CMS Muon Group

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We present the measurements and calculations that predict the behavior of the CSC electronics under HL-LHC conditions. We describe the design of the electronics systems for the upgrade and show studies of expected performance.

I. OVERVIEW

CATHODE strip chambers [1] are part of the muon detection system in the endcap regions of the CMS detector, shown in green in Fig. 1. The inner rings of CSCs (circled in red) have the highest particle flux, presenting significant challenges to efficient readout at the increased luminosity, trigger rate and latency expected at the HL-LHC. The instantaneous luminosity of the HL-LHC is projected to reach $0.75 \times 10^{35} \text{ s}^{-1} \text{ cm}^{-2}$, whereas the current maximum is $0.15 \times 10^{35} \text{ s}^{-1} \text{ cm}^{-2}$. Further, the Level 1 Trigger rate (L1A) and latency will be increased from about 100 kHz to 750 kHz and from $3.4 \mu\text{s}$ to $12.5 \mu\text{s}$, respectively [2]. These are expected to lead to data loss from CSC electronics in the following three ways:

Fig. 1: Quarter-view of the CMS detector, with CSC highlighted in green and inner rings circled in red

- 1) Buffer saturation in the cathode front end boards (CFEBs) of the inner rings (ME1/1, ME2/1, ME3/1, ME4/1)
- 2) Buffer overflow in anode local charged track (ALCT) boards in all chambers
- 3) Insufficient link bandwidth in the data readout path.

Several boards must be upgraded to maintain the high efficiency of CMS and avoid data loss in the CSC system [3]. The CSC system layout from chamber to DAQ output is shown in Fig. 2.

Fig. 2: CSC System Layout, with chamber, peripheral crate, and DAQ output

II. CFEB EVENT LOSS

Data-loss estimates have been made for HL-LHC conditions using a queuing + Poissonian loss model [4]. Application of this model to the inner rings of CSCs show event loss at a rate of more than 10% at the expected 750 kHz L1A rate, shown in Fig 3. This unacceptable data loss, caused by the present limited analog buffer storage, motivates the introduction of lossless digital cathode front end boards (DCFEBs).

Fig. 3: Event loss due to queuing + Poissonian loss model applied to inner rings of CSC

A. DCFEB Upgrade

DCFEBs use flash ADCs and digital pipelines in place of the switch capacitor arrays used on CFEBs. The Virtex 1 FPGA is upgraded to a Virtex 6, and the readout is changed from copper cabling to a fully optical readout. A comparison of DCFEB and CFEB performance in the same queueing model is shown in Fig. 4, with no event loss at expected HL-LHC luminosities for ME2/1. DCFEBs are based on those

Fig. 4: CFEB (black) and DCFEB (red) fraction event loss vs. luminosity at 750 kHz L1A rate

developed for upgrade of the inner-most station 1 CSC ring (ME1/1) during the first long shutdown (LS1) of the LHC. A CFEB-DCFEB comparison is shown in Fig. 5. DCFEBs will be installed during LS2 (2019-2020) in the inner ring stations ME2/1, ME3/1, ME4/1.

Fig. 5: CFEB-DCFEB board comparison

B. Trigger Readout

Current trigger readout from the CFEBs is done through copper cables which output to a trigger motherboard. The optically-connected DCFEBs require optical trigger motherboards (OTMBs), similar to those currently used in ME1/1.

III. ALCT DATA LOSS

The increased $12.5\mu s$ HL-LHC L1A latency will overflow the pipelines of the current Virtex E FPGA, leading to event loss. New modified mezzanine boards will be designed and fitted on the ALCTs, using a Spartan 6 FPGA and a higher bandwidth optical link to ensure lossless output.

IV. DATA READOUT

Current DAQ motherboards (DMBs) are read out via a 1.6 Gbps link. While sufficient for LHC Runs 1 and 2, data readout rates exceeding 10 Gbps are expected in HL-LHC conditions, as shown in Table I. New optical DMBs (ODMBs) will be designed with higher bandwidth optical links to the FED system, which is the interface between the CSCs and the central DAQ of CMS. Links capable of up to 20 Gbps will be developed to handle the increased data rate for all MEx/1 ($x=1,2,3,4$) chambers, providing an acceptable safety margin. FEDs will be replaced throughout with a new system that can receive the higher input rates.

TABLE I: Total HL-LHC CSC DAQ rate per chamber (Gbps)

ME1/1	12.5
ME2/1	6.8
ME3/1	4.6
ME4/1	4.4

V. FUTURE STUDIES

Studies are ongoing to further understand the effect of increased luminosity and more stringent trigger requirements

on CSC chambers and electronics, and to ensure efficient operation of the CSCs for decades to come. One such study uses a muon beam and the CERN GIF++ 14TBq Cs-137 source to simulate the harsher background conditions expected at the HL-LHC. This is important to understand, as more background hits in the chambers pose problems for triggering and reconstructing muons. Fig. 6 shows an event from this study in one CSC chamber. The three views show the anode hits, the cathode information for triggering, and the precision cathode pulse-heights, on each channel in the chamber. The muon can be seen as the blue line in the bottom left, and the Cs-137 decay photons are the scattered hits in the top two views. The gray region in the bottom view was not read out. Possible aging effects on the CSC chambers and electronics from these high background conditions are also being studied.

Fig. 6: Cosmic muon event with gamma background hits at CERN GIF++

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