The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

08 December 2016 (v3, 14 December 2016)

Phase 1 upgrade of the CMS Pixel Detector

Anirban Saha for the CMS Collaboration

Abstract

The pixel tracker of the Compact Muon Solenoid (CMS) experiment is the innermost sub-detector, located close to the collision point, and is used for reconstruction of the tracks and vertices of charged particles. The present pixel detector was designed to work efficiently with the maximum instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. In 2017 the Large Hadron Collider (LHC) is expected to deliver a peak luminosity reaching up to $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, increasing the mean number of primary vertices to 50. Due to the radiation damage and significant data losses due to high occupancy in the readout chip of the pixel detector, the present system must be replaced by a new one in an extended end-of-year shutdown during winter 2016/2017 in order to maintain the excellent tracking and other physics performances. The main new features of the upgraded pixel detector are the a ultra-light mechanical design with four barrel layers and three end-cap disks, digital readout chip with higher rate capability and a new cooling system. In this document we discuss the motivations for the upgrade, the design and technological choices made, the status of the construction of the new detector and the future plans for the installation and commissioning.

Presented at *IPRD16 14th Topical Seminar on Innovative Particle and Radiation Detectors*

PREPARED FOR SUBMISSION TO JINST

14TH TOPICAL SEMINAR ON INNOVATIVE PARTICLE AND RADIATION DETECTORS (IRPD16)

SIENA

3 – 6 OCTOBER, 2016

Phase 1 upgrade of the CMS Pixel Detector

Anirban Saha^a on behalf of the CMS collaboration

^a*INFN Sezione di Perugia, Università di Perugia,
Perugia, Italy*

E-mail: Anirban.Saha@cern.ch

ABSTRACT: The pixel tracker of the Compact Muon Solenoid (CMS) experiment is the innermost sub-detector, located close to the collision point, and is used for reconstruction of the tracks and vertices of charged particles. The present pixel detector was designed to work efficiently with the maximum instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. In 2017 the Large Hadron Collider (LHC) is expected to deliver a peak luminosity reaching up to $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, increasing the mean number of primary vertices to 50. Due to the radiation damage and significant data losses due to high occupancy in the readout chip of the pixel detector, the present system must be replaced by a new one in an extended end-of-year shutdown during winter 2016/2017 in order to maintain the excellent tracking and other physics performances. The main new features of the upgraded pixel detector are the a ultra-light mechanical design with four barrel layers and three end-cap disks, digital readout chip with higher rate capability and a new cooling system. In this document we discuss the motivations for the upgrade, the design and technological choices made, the status of the construction of the new detector and the future plans for the installation and commissioning.

KEYWORDS: Pixel detector; Upgrade; CMS.

Contents

1	Introduction	1
2	Upgraded detector design	2
3	Readout chip and modules	3
4	Construction status	5
5	Testing, installation and commissioning	6
6	Conclusion	7

1 Introduction

The innermost layers of the current CMS [1] tracker are built out of pixel detectors arranged in three barrel layers (BPIX) and two forward disks in each end cap (FPIX) region. The pixel detector provides space points that are used as seeds in the track finding and those are crucial for resolving track ambiguities in high occupancy environments like the core of jets and for tagging products of the decay of heavy flavor quarks. The original CMS detector was designed to operate at a maximum instantaneous luminosity of $1 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ which has already been exceeded in 2016. We foresee a further increase in the luminosity in 2017. The limited size of the buffers and readout bandwidth on the pixel readout chips (ROCs) introduce a dynamic inefficiency that results in a loss of tracking efficiency. In 2017 The Large Hadron Collider (LHC) is expected to deliver a peak luminosity reaching up to $2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$, increasing the mean number of primary vertices per bunch crossing (pileup) to 50. Under such conditions, the present pixel system is expected to experience significant hit inefficiencies (16% in the innermost layer), mainly due to buffer overflow in the present ROC, which would cause a significant degradation of the physics performance of the CMS detector. To overcome these limitations the CMS collaboration has started the construction of a new pixel detector in 2012 [2]. The main new features of the upgraded pixel detector are the a ultra-light mechanical design with four barrel layers and three end-cap disks, digital readout chip with higher rate capability and a new cooling system. It also improves the power of the b-tagging algorithms for events with a large number of collisions per bunch crossing (pileup).

The following sections give an overview of the concept and the design of the Phase 1 upgrade of the CMS pixel detector. In this proceedings we discuss the upgraded detector design, readout chips, modules, the construction status and the installation of the final detector along with its testing and commissioning.

2 Upgraded detector design

The new detector features new digital readout chips with larger buffers and increased data transmission bandwidth to overcome the main limitation of the current detector. One additional tracking layer both in the barrel and in the end cap region, and measures to reduce the amount of material in the tracking volume, help the new detector to achieve good tracking efficiency and b-tagging performance. The rate of fake tracks is also improved even for the events with many primary vertices i.e., with high pileup. Additional benefits arise from a reduction of the radius of the first tracking layer from 4.4 cm to 2.9 cm, following the installation of a new beam-pipe with reduced radius during the 2012-2014 shutdown. The addition of one more tracking layer will compensate for possible losses of efficiency in the silicon strip tracker that may occur as that detector continues to operate until 2023, when the entire tracker is slated for replacement. Most of the services for the upgraded pixel detector (power distribution, readout and control optical fiber plants) are kept from the original detector, in order to reduce the time needed for installation. The addition of one tracking layer and the increase of the outer radius covered by the pixel detector result in a doubling of the total number of channels, from 48M to 79M for BPIX, and from 18M to 45M for FPix. A comparison of the geometries of the original detector and of the phase 1 upgrade is shown in Fig. 1. The geometrical layout of the upgrade system consists of four cylindrical barrel layers placed at radii of 29, 68, 109, 160 mm and three disks in each of the forward regions placed at a distance from the nominal interaction point of 291, 396 and 516 mm. This layout is optimised in order to offer full 4-hit tracking coverage up to pseudorapidities of 2.5, with an increased redundancy compared to the present system.

Figure 1. Comparison of the geometrical layouts of the current (bottom) and upgraded (top) CMS pixel detectors.

The amount of material of the upgraded detector is comparable to the one of the present detector in the central region, despite the addition of an extra detector layer, and it is significantly reduced at higher pseudorapidities. This is achieved due to the usage of the new light-weight support structures and to a new CO₂ evaporative cooling system, replacing the present C₆F₁₄ mono-phase cooling system, and optimised layout of the services. The heat removal of the new two-phase cooling system is more effective compared to that of a single phase system. The service electronics is displaced from inside the tracking volume covered by the silicon strip tracker ($|\eta| < 2.5$) to larger pseudorapidities¹. This effectively reduces the material budget. Further material reduction is

¹CMS uses a right-handed coordinate system. The x-axis points to the center of the LHC ring, the y-axis points up

achieved in FPIX by building the disk supports with carbon based compounds instead of aluminum as in the present detector.

The new detector will employ a new μ TCA-based data acquisition system (DAQ), replacing the present VME-based DAQ. A total of 1184 modules constitute the BPIX layers, while 672 are used for the FPIX disks. Both the Phase1 and the present system are built out of 285 μm thick n^+ -in- n silicon sensors that cover an active area of $16.2 \times 64.8 \text{ mm}^2$. The sensor is bump-bonded to an array of 2×8 ROCs comprising 66 560 pixels.

3 Readout chip and modules

The readout chip for the upgraded detector, named *psi46digv21respin*, is based on the present *psi46* readout chip [3]. The same fabrication technology (250 nm CMOS) is used for the new pixel detector as done in the present pixel detector. It is demonstrated to be able to sustain the radiation dose of the data that will be collected until 2023. Thin flexible printed circuits called the high density interconnect (HDIs) are glued on top of the sensor and connected via wire bonds to the readout chips for control and readout purposes. The HDI is connected to the sensor as well to provide the bias voltage. Each HDI routes the data from the ROCs to one or two token bit manager (TBM) ASICs that organize the readout and aggregate and format the data. The data from 4, 8 or 16 ROCs (depending on the layer, 4 for BPIX layer 1, 8 for BPIX layer 2, and 16 for the remaining detectors) is shipped off the module at 320 MBit/s through 4/5 bit encoded data streams. This represents a gain of a factor eight in the data throughput compared to the original detector, where the readout bandwidth was limited to 40 MBit/s. The BPIX and FPIX modules differ mostly for the HDI technology and the cable used for the readout. Different vendors and different types of bump bonding have been used for the construction of the modules, but similar quality and yields have been obtained.

The ROCs use a similar zero-suppressed and column drain architecture in the chip used for layers 2-4 of BPIX and for FPIX, while a completely new readout architecture (PROC600) is used for layer 1 of BPIX which needs to sustain higher readout speed. Each ROC comprises 80 rows and 26 double columns. To increase the bandwidth, the 40 MHz analogue readout has been changed to 160 Mbit/s digital readout, requiring the addition of an 8 bit ADC. The data streams from two banks of ROCs are merged in the TBM to achieve the module data transmission rate of 320 MBit/s. The buffer depths of the hit and time-stamp buffers have been increased from 32 to 80 and from 12 to 24, respectively. Furthermore an additional readout buffer has been added. The cross-talk inside the ROCs has been reduced and the comparator in each pixel cell is improved, leading to a reduction of the threshold from about 3200 electrons to about 2000 electrons. This increases the efficiency and the lifetime of the detector under irradiation, given that clusters with total smaller charge can be identified, and also leads to an improvement of the intrinsic position resolution for each of the pixel modules. The version of the chip used for layers 2-4 of BPIX and FPIX has been characterized in beam tests, where it ran stably with a threshold as low as 1800 electrons [4]. The ROC was also tested after irradiation with 23 MeV protons to doses of 0.6 MGy and 1.2 MGy, corresponding to

vertically and the z-axis points along the beam direction. The azimuthal angle ϕ is measured in the xy-plane and the radial coordinate is denoted by r. The polar angle θ is defined in the rz-plane and the pseudorapidity is $\eta = -\ln \tan \frac{\theta}{2}$

the doses expected in layer 2 and 1 after integrated luminosities of 500 fb^{-1} , which is the expected amount of data collected by 2023. Simulation of the readout speed and efficiency measurements in the high occupancy environments indicate that the dynamical inefficiency of the ROCs is below 2% for layer 2 of BPIX, while a dedicated version of the ROC is needed for the innermost layer of BPIX, where the dynamical inefficiency would be too high. The ROC used for layer 1 of BPIX uses a new readout architecture where clusters of 2×2 pixels are formed in the double column and transferred in a single step, instead of transferring individual pixels [5]. This new dynamic cluster column drain mechanism, coupled with the increase in the number of double columns that can be simultaneously transferred to the ROC periphery, results in an increase of the maximum rate that can be sustained by the layer 1 BPIX modules with a limited ($< 2\%$) inefficiency to approximately 600 MHz/cm^2 , which is compatible with the expected rate in the CMS experiment. The detailed views of the pixel modules are shown in Fig. 2.

Figure 2. The detailed views of the pixel modules with all the components for Layer 1 (left) and Layer 2 to 4 (right).

After the modules are assembled they are tested and calibrated in order to identify faulty modules and discard them prior to the installation in the CMS detector, which consists of a series of functionality tests at low temperature (-20°C) before and after a series of thermal cycles, and at room temperature ($+17^\circ\text{C}$) after the thermal cycles. Dedicated setups reproducing the environmental conditions of the final pixel system are used to carry out the module qualification. The sensor is characterised through a measurement of its leakage current as a function of the bias voltage (IV measurement), performed both at low and room temperature. A grading system was developed in order to automatically divide modules into three classes, A, B and C. The last class contains the discarded modules, based mainly on pixel defects and sensor leakage current. Modules are also tested in X-ray setups. The X-ray beam is used to simulate intense readout traffic in the ROCs and to measure single-hit efficiency and other properties in those conditions. The ROC energy-response is also measured using fluorescence lines as reference.

At the time of the Siena Conference (first week of October) the module construction and qualification for barrel layers 2-4 was completed. The assembly and testing of additional spare modules for layer 2 was still progressing. The construction of the modules for the innermost barrel layer using the new PROC600 readout chip was ended in October. The construction and qualification of the modules for the forward disks was completed at that time.

4 Construction status

The BPIX shells and the FPIX disks are supported by two sets of half cylinder supports, called supply tube in the case of BPIX and service cylinders in the case of FPIX. The readout, control and powering electronics boards are included in these support tubes. The construction of the barrel and forward part of the phase 1 CMS pixel detector is distributed among multiple institutions in Europe for BPIX and the US for FPIX. The completed parts of the detectors, the two halves of BPIX and the four half cylinders of FPIX, are assembled and tested at PSI in Switzerland and Fermilab in the US, respectively. The half shells supporting the BPIX modules are near to completion and modules have already been installed on three half shells for layers 2-4. The four supply tubes (two on each side of the BPIX barrel half shell) have been completed with the installation of all the service electronics and are currently under test. The installation of the modules on all the half shells for BPIX is complete. The first half of the detector (the four half shells for layers 1-4 of the barrel and the two supply tubes on either side of the barrel) was assembled by the end of November. The second half of the detector will be ready by the end of December. Photos of the first layer 2 half shell with all its modules installed and of the first complete supply tube are shown in Fig. 3.

Figure 3. Photo of the first complete layer 2 BPIX half shell with all its modules installed and cabled (left) and photo of the first complete BPIX supply tube, with all the readout, control, and power electronics installed (right).

The construction of the mechanical supports (disks and half cylinders) for the forward disks was completed in early September, and all the electronics was installed in the service cylinders at the beginning of October. The installation of the modules on the half disks for FPIX was completed by the end of October. The four FPIX half cylinders were fully assembled at Fermilab by installing the half disks inside the half cylinder, performing all the electrical and cooling connections. Three half cylinders were tested at Fermilab, then they were dismantled removing the disks from the half

cylinders, prior to their transport to CERN. For the last one the disk insertion in the half cylinder will be performed at CERN. Two complete half cylinders were delivered to CERN and reassembled with all the half disks in October. The remaining two half cylinders were assembled at CERN in November. A photo of three half disks (split into an inner and an outer part) installed in the first complete half cylinder is shown in Fig. 4.

Figure 4. Photo of three FPIX half disks installed in the first completed half cylinder.

5 Testing, installation and commissioning

Two different approaches were taken for the testing of the completed BPIX and FPIX detectors prior to their installations. For BPIX the initial tests of the readout chain are performed by moving the connections of a reference set of modules to all the channels of a supply tube, performing a sequence of tests, which are pretty similar to that of FPIX. The supply tube is first tested at room temperature and then in the cold condition. After the connection of the supply tube to a set of half shells the same tests can be performed by reading out only one sector at a time at room temperature, due to the limitations introduced by the available cooling power at PSI and by the number of readout electronic channels. These tests will be repeated, possibly also at the target operating temperature of $-23\text{ }^{\circ}\text{C}$, after the transport of the detector to CERN at the beginning of February 2017.

Each FPIX half cylinder is tested in conditions as close as possible to those after the installation in CMS first at Fermilab and then at CERN. After the installation of disks into the half cylinder all electrical, optical, and cooling connections are made, and then the pressure and leak tests for the cooling systems are performed. At that point the half cylinder is tested with the final μTCA readout system. After the mapping of the channels are checked, for each individual module appropriate

delays relative to an external trigger are established for the readout and phases are set for each individual TBM core. The initial calibrations are obtained with the digital test boards as starting point and then the functionality checks are repeated on each of the modules. Then sensor leakage current, pixel by pixel noise and bump bonding quality are checked again to identify modules that may have been damaged during the installation of the disks into the half cylinders or during the transportation to CERN. Damaged modules can be replaced at this point, although the most commonly encountered problem is that of loose connections of cables and electronic components. All these tests are performed first at room temperature and then with the CO₂ cooling temperature set to -20°C. At Fermilab one entire half disk was read out, while at CERN enough readout and power channels are available to perform these tests on one entire half cylinder. The full calibration of the half cylinder at the target operating temperature of -23 °C is scheduled to be done in December and January.

The current pixel detector will be removed in January 2017 and in the following weeks part of the services will be replaced. The original cooling lines will have to be replaced to allow for the transition from C₆F₁₄ cooling to CO₂ cooling and optical fibers in the same region will also be replaced. The new BPIX and FPIX detectors will be installed at the end of February over a period of two weeks. Initial tests of the detectors will be performed at room temperature and only after the sealing of the water vapor barriers and the closure of the CMS end caps the detector will be operated in cold environment. Then the full calibrations of the new pixel detector will be performed prior to having circulating beams in the LHC, and cosmic data will also be collected, which could help with the alignment of the forward disks along the beam direction. Further refinements of the alignment will require more data and possibly additional cosmic ray data in between two collision runs.

6 Conclusion

The CMS pixel system will be replaced by an upgraded detector in an extended year end shutdown period just before the starting of the 2017 data taking, with a minimal impact on the data taking. The new pixel system will have one extra layer, while minimising the material budget of the whole tracking volume. It will be able to operate at significantly higher rates and perform excellently at the increasing instantaneous luminosities of the LHC in the coming years.

References

- [1] The CMS collaboration, *The CMS experiment at the CERN LHC*, [JINST 3 \(2008\) S08004](#).
- [2] The CMS collaboration, *Technical design report for the pixel detector upgrade*, [CERN-LHCC-2012-016 \[2012\]](#).
- [3] The CMS collaboration, *Design and performance of the CMS pixel detector readout chip*, [Nucl. Instr. Methods A565 \(2006\) 188](#).
- [4] S. Spannagel, Status of the CMS phase 1 pixel detector upgrade, [Nucl. Instr. Methods A831 \(2016\) 71](#).
- [5] A. Starodumov, High rate capability and radiation tolerance of the new CMS pixel detector readout chip PROC600, CMS CR – 2016/269, to be published in JINST, proceedings of PIXEL 2016.