The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

29 November 2016 (v4, 12 December 2016)

PS-Module prototypes with MPA-light readout chip for the CMS Tracker Phase 2 Upgrade

Johannes Grossmann for the CMS Collaboration

Abstract

During the HL-LHC era an instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ will be reached and possibly 3000 fb^{-1} integrated luminosity will be delivered. This results in the requirement for a major upgrade of the CMS Outer Tracker detector. This contribution briefly reviews the module types and the front end readout electronics foreseen in the preparation program known as phase 2 upgrade. R&D towards the construction of full module prototypes for the Pixel-Strip (PS) module is ongoing. The module combines a macro-pixel sensor and a strip sensor and has p_T -discrimination capability at module level. The current experience from module construction with a demonstrator assembly and initial laboratory testing with an alternative module concept for the PS-module is shown. A possible calibration method is introduced.

Presented at *IPRD16 14th Topical Seminar on Innovative Particle and Radiation Detectors*

PREPARED FOR SUBMISSION TO JINST

14TH TOPICAL SEMINAR ON INNOVATIVE PARTICLE AND RADIATION DETECTORS

3 - 6 OCTOBER 2016

SIENA, ITALY

PS-Module prototypes with MPA-light readout chip for the CMS Tracker Phase 2 Upgrade

J. Grossmann,¹ for the CMS collaboration

*Institute of High Energy Physics,
Nikolsdorfer Gasse 18, 1050 Vienna, Austria*

E-mail: Johannes.Grossmann@oeaw.ac.at

ABSTRACT: During the HL-LHC era an instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ will be reached and possibly 3000 fb^{-1} integrated luminosity will be delivered. This results in the requirement for a major upgrade of the CMS Outer Tracker detector. This contribution briefly reviews the module types and the front end readout electronics foreseen in the preparation program known as phase 2 upgrade. R&D towards the construction of full module prototypes for the Pixel-Strip (PS) module is ongoing. The module combines a macro-pixel sensor and a strip sensor and has p_T -discrimination capability at module level. The current experience from module construction with a demonstrator assembly and initial laboratory testing with an alternative module concept for the PS-module is shown. A possible calibration method is introduced.

KEYWORDS: Particle tracking detectors, solid state detectors, Si microstrip and pad detectors, front end electronics for detector readout, electronic detector readout concepts (solid-state)

¹Corresponding author.

Contents

1	The CMS Tracker Phase 2 upgrade	1
2	Module concepts and prototypes	1
3	Macro-Pixel ASIC	3
4	Noise sources theoretical predictions and calibration algorithm	4
5	Studies of noise and Sr-90 signal	5
6	Conclusion and Outlook	8

1 The CMS Tracker Phase 2 upgrade

For the high luminosity LHC era the CMS tracker detector [1–3] will undergo a major upgrade, which is designed to record 3000 fb^{-1} of integrated luminosity. An average of 140 interactions per bunch crossing will occur at nominal luminosity and a L1 trigger rate of 750 kHz is expected. The tracker will have on module data reduction and will provide tracking information, which is given by the p_T -modules, at 40 MHz for the L1 trigger system. Simulations predict $1.12 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ fluence at $R = 20 \text{ cm}$ in the innermost layer of the outer tracker, which requires R&D activities to verify the radiation hardness of chosen sensor base materials and to identify a robust sensor design.

2 Module concepts and prototypes

The p_T -modules combine two closely spaced silicon sensors and have on module p_T -discrimination functionality at a programmable threshold around $p_T \approx 2 \text{ GeV}$. The readout chips of the p_T -modules have binary readout and integrated on-chip logic capabilities. The p_T -discrimination is achieved by a coincidence window, which correlates the hits in two silicon sensors within one module (Figure 1). A bent track, which corresponds to a low p_T -particle, produces a hit outside the coincidence window. If a compatible hit pair, with a hit inside the window, is detected, this is defined as a stub and data are sent to the trigger system. One obtains a uniform p_T threshold in all module locations with an offset correction and an adjustment of the sensor spacing.

In Figure 2 a layout of the tracker is shown. In parts of the barrel region PS modules are tilted with respect to the beam axis. This reduces the material budget in certain pseudorapidity (η) regions and the fraction of tracks which would not generate trigger stubs.

Two types of modules are foreseen. The PS-Module (Figure 3) is composed of a macro-pixel sensor (PS-p) with $100 \mu\text{m} \times 1446 \mu\text{m}$ cells and a strip sensor (PS-s) with $100 \mu\text{m}$ pitch and 2.5 cm long strips. The distance of the sensors is 1.6 mm, 2.6 mm or 4 mm. These distances are fixed with

Figure 1: The principle of p_T -discrimination at module level [2]. A coincidence window selects hit pairs compatible with the p_T -threshold. The acceptance window (green) and the sensor spacing are tuned to have a uniform p_T -threshold in all tracker regions.

Figure 2: The CMS outer tracker tilted layout, with 2S-modules in red and PS-modules in blue [3].

a carbon-fiber reinforced aluminium (Al-CF) precision spacer. The macro-pixel sensor is readout by the Macro-Pixel ASIC (MPA). The pixels are directly coupled to the readout chip using the bump bonding technique. The PS-s sensor is read out by 16 Short Strip ASICs (SSA), which send sparsified hit information to the MPA. The main logic functionality for the correlation of the hits is integrated in the MPA. The concentrator IC (CIC) buffers, sparsifies and aggregates the data from the MPAs on the module and sends them to the service hybrid.

The 2S-Module combines two identical silicon strip sensors with $90\,\mu\text{m} \times 5\,\text{cm}$ strips [4, 5] and has sensor spacings of 1.8 mm or 4 mm. For this module the foreseen readout chip is the CMS Binary Chip (CBC) and the strips are AC-coupled to the chip via the wire bonding technique. A more detailed description is found in [3].

The PS-modules (in blue in Figure 2) cover the inner region of the outer tracker, where higher granularity is required to keep the occupancy at the $O(1\%)$ level. The pointing resolution in z -direction should allow to identify the interaction point within the trigger data. The 2S modules (in red in Figure 2) are situated in the outer region of the tracker.

Small size prototypes ($5.4\,\text{mm} \times 12.7\,\text{mm}$) of the Macro-Pixel-Sub-Assembly (MaPSA, Figure 4) were built to study the performance of the sensor layout and the functionality of the MPA. The MaPSA-light demonstrator incorporates MPA demonstrator readout chips (MPA-light) bump bonded to one PS-p prototype sensor (PS-p-light). The baseline design connects the sensor with bump bonds to the readout chip and uses wire bonds to connect the chip with the front end hybrid. In an alternative design, called the inverted MaPSA, the connection to the hybrid is made with wire bonds on the sensor (Figure 5). Prototypes for the two different designs were built and tested.

This inverted approach is different with respect to the baseline, since digital IO and power lines of the readout chip are fed through a dedicated routing area on the periphery of the inverted PS-p-light sensor (Figure 6). The routing area is surrounded by a floating guard ring and the implant area underneath the metal strips is depleted. This ensures a good electrical isolation of the signal lines. For this design, ionizing particles in the depletion region underneath the routing area produce a signal, which may couple to the microstrips. The amplitude of these signals is small with respect to the signal levels of the readout chip, nonetheless this may result in additional noise. Advantages of the inverted approach are that the readout chips are cooled from the backside, the possibility of

Figure 3: The PS module has a macro-pixel and a strip sensor, [2].

Figure 4: A cross section of the baseline PS module [2]. The Macro-Pixel-Sub-Assembly (MaPSA) is the bottom part of the sketch, which incorporates the PS-p sensor and the MPA readout chip.

Figure 5: A cross section of the PS module with the inverted MaPSA, where wire bond connections are to the sensor only.

scattering in between the two sensors is reduced and no wire bonding is necessary to connect the MPA to the hybrid.

3 Macro-Pixel ASIC

In the following the functionality of importance for the tests of the MPA [6, 7] is introduced. The analog front end of the chip has a charge sensitive preamplifier, a shaper and a discriminator. A feedback circuit is integrated to provide leakage current compensation up to 200 nA for the DC-coupled sensor. A digital-to-analog converter (DAC) sets a common threshold for all pixels (TDAC). In order to compensate for pixel to pixel variation each channel has a trimming DAC (TRIMDAC) offset correction. The simulated least significant bit (LSB) value under nominal conditions for the TDAC is $107 e$ and for the TRIMDAC $275 e$ [8, 9]. The MPA-light demonstrator chip reads out 48 channels in 3 rows of 16 macro-pixels. For the full MaPSA-light prototype six MPA-light chips connect to 288 channels of the PS-p-light sensor. At the chip edges the corresponding macro-pixels on the sensor have $200 \mu\text{m}$ width and therefore a higher pixel capacitance. A block diagram of the

Figure 6: The prototype sensor is bump bonded to two MPA-light demonstrator chips. The picture shows one half of the inverted assembly with a single MPA-light chip.

Figure 7: The simplified block diagram of the data acquisition system used for the test.

readout chain used for conducting the tests is found in Figure 7. Each channel is equipped with a 16 bit ripple counter, which samples the discriminator output with a rate of 40 MHz. A shutter signal defines the integration time. This asynchronous readout mode can be used for connectivity tests and calibration. Each channel has a on-chip test capacitance, which can be used for test pulse injection.

4 Noise sources theoretical predictions and calibration algorithm

The input capacitance C_{in} for the charge sensitive amplifier is assumed to be smaller than

$$\begin{aligned} C_{in} &= C_{\text{pixel}} + C_{\text{BondingPad}} + C_{\text{ESD}} \\ 495 \text{ fF} &= 280 \text{ fF} + 55 \text{ fF} + 160 \text{ fF}, \end{aligned} \quad (4.1)$$

where C_{pixel} is the capacitance of the pixel, $C_{\text{BondingPad}}$ is the capacitance of the bonding pad and C_{ESD} is the capacitance of the ESD protection [6]. C_{in} is the most important contribution to single channel equivalent noise charge (ENC_{channel}), which is expected to be $ENC_{\text{channel}} = 200 e$ [6] for this scenario. The total ENC is given by

$$ENC_{\text{tot}} = \sqrt{ENC_{\text{channel}}^2 + ENC_{\text{spread}}^2}, \quad (4.2)$$

where ENC_{spread} is the channel-to-channel variation of the threshold. The goal of a calibration algorithm is to minimize ENC_{spread} . A calibration is possible with and without an injected test pulse. In this work the test pulse was not used. An estimation for the theoretical minimum value of ENC_{spread} in units of LSB_{TDAC} is

$$\begin{aligned} Min(ENC_{\text{spread}}) &= \sqrt{\frac{1}{12} \times (LSB_{\text{TRIMDAC}}/LSB_{\text{TDAC}})^2} \\ &= 0.74, \end{aligned} \quad (4.3)$$

Figure 8: The setup in a light-tight metal box. The Sr-90 source is indicated in orange.

using $Q_{rel} = 0.5 \times \text{LSB}_{\text{TRIMDAC}} / \text{LSB}_{\text{TDAC}}$ and assuming that the probability for the pedestal value P_i of channel i out of n channels to be in an interval $I = [\bar{P} - Q_{rel}, \bar{P} + Q_{rel}]$ after the calibration is uniform, where $\bar{P} = 1/n \sum_i^n P_i$.

The calibration of the MPA-chip was done in an iterative way using the asynchronous shutter readout mode. For the initial configuration standard values are loaded for the TRIMDAC values. Then a threshold scan is performed with the precision of $1 \text{ LSB}_{\text{TDAC}}$. For each TDAC setting the noise hits are counted using the ripple counter. The normalized noise spectrum is described by the difference of two error functions for the rising and the falling edge of the discriminator. A gaussian function is used to fit each pixel curve, since the distance of mean values of the two error functions is small. P_i is defined by the gaussian mean. The gaussian standard deviation describes the single channel noise σ_i . The next step in the calibration predicts from linear extrapolation for each channel a TRIMDAC value with the lowest distance to the preset mean and after a configuration step the threshold scan is repeated.

This Newton algorithm is iterated and it was achieved to minimize ENC_{spread} within three iterations, which is possible due to the good linearity of the DACs [9]. Statistical fluctuations in the production process of the chip and the sensor may result in hot pixels or channels that cannot be trimmed. These pixels can have P_i outside the interval I and should be switched off.

5 Studies of noise and Sr-90 signal

One baseline prototype and one inverted prototype were tested. The full data acquisition chain can be seen in Figure 7. For all tests the sensor was biased at 100 V. The baseline prototype available for this study has 5 responding MPA-light chips, which results in a total number of 240 channels. The inverted prototype has 2 MPA-light chips with in total 96 channels. The setup was placed in a light-tight metal box (Figure 8). After the calibration a noise figure σ_i was extracted for every channel. The chosen integration time was 0.3 s at each TDAC value. For ENC_{tot} and ENC_{spread} the channels with $P_i \notin I$ are excluded. All values presented in this section are in units of LSB_{TDAC} .

The recorded pedestal curves for all channels with the corresponding fit functions for the inverted concept are shown in Figure 9 and the corresponding σ_i obtained are shown in Figure 10. It was observed that some channels pick up additional noise, which is visible as non gaussian tail towards low TDAC values in the pedestal distribution (Figure 9). These channels correspond to the

Figure 9: The recorded pedestals and the gaussian fit functions for each pixel of the inverted concept. Each color corresponds to one pixel.

channels at the edge of the readout chip. The absolute value in the flat region of the tails is related to the number of shutter openings.

For the baseline prototype the extracted σ_i from a similar scan are shown in Figure 11. For both module prototypes the channels at the interchip boundaries have slightly higher σ values, due to greater capacitance of the pixels of 200 μm width.

The extracted noise figures are shown in Table 1. $\overline{ENC}_{\text{channel}}$ for both module types tested in this study is comparable and the differences may originate in six badly connected pixels for the inverted module, the variations in the quality and the type of the bump bonding process and the different PCB technology used. ENC_{spread} was observed to be close to the expected value. Figures for reference modules are given in [9].

A Sr-90 source was placed on top of the assembly and the asynchronous readout was used to test the homogeneity of the gain and to identify unresponsive pixels (Figures 12 and 13). One observes a broad continuous spectrum, which is due to the continuous energy spectrum of the electrons and the asynchronous recording. Only small pixel-to-pixel variations were found for the entire dynamic range of the TDAC. The position of the source relative to the board was fixed and the integration time was equal for both modules in order to make a comparison of the relative efficiency. The measured spectra have similar shapes for both modules.

Table 1: Extracted noise figures in units of LSB_{TDAC} .

Prototype	$\overline{ENC}_{\text{channel}}$	$StdDev(ENC_{\text{channel}})$	ENC_{spread}	ENC_{tot}
Baseline design	2.86	0.52	0.85	2.98
Inverted design	1.92	0.20	0.83	2.61

Figure 10: The obtained sigma values from the gaussian fits to the pedestals for the inverted module with two MPA-light chips.

Figure 11: The obtained sigma values from the gaussian fits to the pedestals for the baseline module with five working MPA-light chips. Columns with slightly higher noise correspond to the pixels at the chip edges with $200\mu\text{m}$ width.

Figure 12: The signals of a Sr-90 source for the inverted module. The gaussian fit functions indicate the noise contribution.

Figure 13: The signals of a Sr-90 source for the baseline module. No channels were switched off after calibration.

6 Conclusion and Outlook

Small size demonstrator modules of the MaPSA were produced in two different flavors. Two of these prototype modules were used to investigate the noise and homogeneity of response to signals from a Sr-90 source. The analog front end of the MPA-light chip was characterized and a noise figure compatible with the predicted value from simulation was found. For the inverted module concept no additional noise is observed and ENC_{tot} is slightly lower than for the tested module of the baseline concept. The tests of the inverted concept showed promising results. Test with particles from a Sr-90 source show good homogeneity of gain among all pixels. Further detailed studies are necessary to compare the efficiency and common mode noise figures.

References

- [1] CMS Collaboration. The CMS experiment at the CERN LHC. *JINST*, 3:S08004, 2008. doi: 10.1088/1748-0221/3/08/S08004.
- [2] CMS collaboration. Technical proposal for the phase-II upgrade of the compact muon solenoid. Technical Report CERN-LHCC-2015-010. LHCC-P-008. CMS-TDR-15-02, CERN, Jun 2015.
- [3] Giacomo Sguazzoni. Upgrades of the CMS outer tracker for HL-LHC. *NIM*, article in press 2016. doi: 10.1016/j.nima.2016.06.033.
- [4] A. König. Exploring the quality of latest sensor prototypes for the CMS tracker phase II upgrade. *NIM*, article in press 2016. doi: 10.1016/j.nima.2016.05.068.
- [5] T. Bergauer. Silicon sensor prototypes for the phase II upgrade of the CMS tracker. *NIM*, A831: 161–166, 2016. doi: 10.1016/j.nima.2016.03.019.
- [6] D. Ceresa, A. Marchioro, K. Kloukinas, J. Kaplon, W. Bialas, V. Re, G. Traversi, L. Gaioni, and L. Ratti. Macro pixel ASIC (MPA): the readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC. *JINST*, 9(11):C11012, 2014. doi: 10.1088/1748-0221/9/11/C11012.
- [7] Davide Ceresa. *Electronic systems for intelligent particle tracking in the High Energy Physics field*. PhD thesis, Politecnico di Torino, 2016. URL <http://dx.doi.org/10.6092/polito/porto/2642937>.
- [8] D. Ceresa, J. Kaplon, K. Kloukinas, and A. Marchioro. *MPA-light user manual*. CERN PH-ESE-ME, 1.1 edition, March 2015.
- [9] D. Ceresa, J. Kaplon, R. Francisco, A. Caratelli, K. Kloukinas, and A. Marchioro. A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS Tracker at HL-LHC. *JINST*, 11(01):C01054, 2016. doi: 10.1088/1748-0221/11/01/C01054.