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The Phase-1 Upgrade of the CMS Pixel Detector

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Abstract

The innermost tracking device of the CMS experiment is a silicon pixel detector. It has to cope with high particle fluxes and radiation damage, and was built to withstand the LHC design luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. This luminosity was already exceeded in 2016 and it is foreseen that it will increase further, potentially reaching two times the design value before 2018. Under such conditions the inefficiencies due to a limited readout bandwidth will increase by as much as 16% in the innermost layer. To maintain high tracking efficiency, the CMS collaboration has built a new pixel detector that was installed in March 2017. In this paper, the design of this so-called Phase-1 pixel detector is summarised, the production and the qualification of the pixel modules is described and the current status of the project is reported.

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The Phase-1 Upgrade of the CMS Pixel Detector

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ABSTRACT: The innermost tracking device of the CMS experiment is a silicon pixel detector. It has to cope with high particle fluxes and radiation damage, and was built to withstand the LHC design luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. This luminosity was already exceeded in 2016 and it is foreseen that it will increase further, potentially reaching two times the design value before 2018. Under such conditions the inefficiencies due to a limited readout bandwidth will increase by as much as 16% in the innermost layer. To maintain high tracking efficiency, the CMS collaboration has built a new pixel detector that was installed in March 2017. In this paper, the design of this so-called Phase-1 pixel detector is summarised, the production and the qualification of the pixel modules is described and the current status of the project is reported.

KEYWORDS: Particle tracking detectors, Solid state detectors

Contents

1	Introduction	1
2	Phase-1 Pixel Detector Design	1
3	Pixel Modules	3
4	Module Production and Qualification	4
5	Integration and Commissioning	6
6	Summary	6

1 Introduction

The CMS experiment [1] at the CERN Large Hadron Collider (LHC) features a silicon pixel detector as its innermost device. It provides space point measurements of charged particle trajectories within a pseudorapidity up to $|\eta| = 2.5$. The original pixel detector, which is hereafter referred to as the Phase-0 pixel detector, consists of a three-layer barrel detector (BPIX) and two endcaps in the forward regions, each comprising two disks (FPIX). The pixel detector was designed to withstand the LHC design luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and a bunch spacing of 25 ns. Due to continuous improvements of the LHC this luminosity was already exceeded in 2016, and it is foreseen that it will be increased further, reaching up to twice the design value before 2018. This will increase the number of interactions per bunch crossing (known as pileup) to 50 or more. As a result, dynamic inefficiencies in the pixel detector, caused by a limited readout bandwidth, will also rise. For example, the data loss in the innermost barrel layer is expected to reach up to 16 % [2] in such an environment. Figure 1 shows how the single hit efficiency decreased with increasing luminosity for all layers during the 2016 data taking period. By the end of 2016 a drop of 5 % in the innermost layer was already evident.

To maintain and even improve the tracking performance during the next few years, CMS has developed and built a new pixel detector as a part of the Phase-1 upgrade. It was successfully installed in March 2017 during an extended year-end technical stop.

2 Phase-1 Pixel Detector Design

Two of the main design drivers for the new detector were the short timescale for installation (it was installed in the extended winter break between the 2016 and 2017 data-taking periods) and the desire to minimize the impact on subsequent data taking. This was achieved in part by making the Phase-1 pixel detector very similar in layout to the original one, making installation simpler

Figure 1. Measured single hit efficiency per layer as a function of the instantaneous luminosity [3]. The data were taken with the Phase-0 pixel detector during 2016.

Figure 2. Comparison of the layouts of the Phase-1 detector (top) and the Phase-0 detector (bottom) [2].

and therefore quicker. The new pixel detector features an additional fourth layer of pixel modules in the barrel and a third disk per side in the endcap region. The number of channels has almost doubled (from 66 million to 124 million), giving a four-hit coverage in the whole tracking region up to $|\eta| = 2.5$. To improve the vertex resolution and the b-tagging efficiency, the radius of the innermost layer has been reduced from 44 mm to 29 mm. This means that a new beam pipe was also required, which was already installed during the Long Shutdown 1 in 2013/2014. A comparison of the Phase-0 detector and the new detector design is shown in Figure 2.

The material budget of the Phase-1 pixel detector has been significantly reduced by moving from a C_6F_{14} liquid cooling system to a two-phase CO_2 cooling system. In the latter, the evaporative cooling allows lower coolant mass flows by making use of the latent heat, and the pipes can be much smaller due to the thermodynamic properties of CO_2 . A further reduction of the material budget was achieved by moving services out of the active volume and by using an ultra-light carbon fiber support structure.

A constraint for the new pixel detector was that the existing power cables had to be reused

because it was not possible to replace them during the relatively short installation period. The number of channels of the new pixel detector has grown by a factor of 1.9, implying corresponding increases in the currents. As a result, the power losses in the cables were expected to increase by a factor of 3.6. To overcome this problem, a new power system based on DC-DC conversion was developed. The existing power supplies have been modified to deliver a voltage of 11 V to the DC-DC converters that are located on the pixel service structures, outside the tracking volume but still within the CMS detector. The DC-DC converters provide the required digital and analog voltages of around 3.3 V and 2.4 V, respectively, to the pixel modules. With this new power system the losses can be reduced by a factor of around 10. About 1200 DC-DC converters have been used in the upgraded pixel detector, with one pair of converters powering up to four modules. A custom DC-DC buck converter has been developed, as radiation-hard DC-DC converters are not available commercially. This device is based on the FEAST2 ASIC, which was designed at CERN, and features an air core coil to allow the operation inside the magnetic field of CMS. Typical efficiencies for an output power of 7 W are around 80% to 85%.

The data acquisition (DAQ) back-end electronics was also upgraded to be compatible with the new detector. The VME-based system was replaced by a new MicroTCA-based system, requiring all back-end boards to be redesigned.

3 Pixel Modules

The basic design of the pixel modules remained unchanged. A module is made of a $285\text{ }\mu\text{m}$ thick $\text{n}^+\text{-in-n}$ type silicon sensor that comprises 66560 pixels, each with a size of $100\text{ }\mu\text{m} \times 150\text{ }\mu\text{m}$. The sensor is bump bonded to 16 readout chips (ROCs). The readout is controlled by the Token Bit Manager chip (TBM), which also aggregates and formats the data and sends it to the detector back-end with a rate of 400 Mbit/s. The particle fluence increases with decreasing radii of the layers, so a special version of the TBM with two data streams is used for layers 1 and 2 in the barrel, with the layer 1 modules actually using two TBMs. The TBM is glued to the High Density Interconnect (HDI), a low mass flex board that distributes the voltages and signals across the module. The HDI is glued onto the backside of the sensor and is connected to the readout chips with wire bonds. Figure 3 shows a schematic view of the modules. For BPIX layers 2-4 and all FPIX layers the modules differ only at the level of minor details. As an example, for the layers 2-4 in the barrel detector there are two $250\text{ }\mu\text{m}$ thick base strips made of Si_3N_4 glued to the long edges of each module to allow it to be fixed to the support structure, whereas in the forward detector a holder is glued onto the short ends.

The ROC used for BPIX layers 2-4 and the FPIX is the `psi46dig` [4], an evolutionary upgrade of the `psi46` chip [5] that was developed for the Phase-0 detector. It was produced with the same 250 nm CMOS process and uses the same column drain architecture to read out pixel hits. The pixels are organized in 26 double columns, each with 80 pixels. Each double column has data and time stamp buffers to store the hits for the trigger latency. To reduce data losses, the number of hit buffer cells has been increased from 32 to 80, the time stamp buffers have been increased from 12 to 24, and an additional global readout buffer has been added. The bandwidth has been doubled by moving from a 40 MHz analog readout with 6 discrete levels to a 160 Mbit/s digital readout. The `psi46dig` has an on-chip ADC to maintain the functionality of reading out the signal height.

Figure 3. Schematic view of the Phase-1 pixel modules [2]. Left: exploded view of a layer 2-4 module. The components shown are (from top to bottom) the cable, HDI with TBM, sensor, ROCs and base strips. Right: Module for BPIX layer 1 with two TBMs (top) and FPIX module (bottom).

Charge sharing between neighboring pixels can be used to improve the single hit resolution, which is around $5\text{--}7\ \mu\text{m}$ [6]. This effect was even improved by operating the new ROC with a minimal threshold of around 1500 electrons instead of the previous value of 3500 electrons, due to changes in the comparator and reduced chip-internal crosstalk.

These changes are still not sufficient to cope with the increased hit rates in the first layer of the barrel detector, so a readout chip known as the PROC600 was developed for these modules. The main new design feature of this chip is a Dynamic Cluster Column Drain architecture that reads out clusters of 2×2 instead of single pixels. The buffers were redesigned so that they no longer have to be reset after a readout and the chip allows up to seven pending column readouts instead of three. The efficiency of this chip was measured in a test beam and is around 98% for a pixel hit rate of $580\ \text{MHz}/\text{cm}^2$ [7], which is expected for layer 1 at an instantaneous luminosity of $2\times 10^{34}\ \text{cm}^{-2}\text{s}^{-1}$.

4 Module Production and Qualification

The pixel modules were produced at a number of different institutes, each taking responsibility for specific parts of the detector. Institutes in Finland, Germany, Italy, Switzerland, Taiwan and CERN (BPIX) were involved, along with a US consortium (FPIX). In total 1856 modules have been installed in the new detector. The general construction procedure for the modules is described below, although it differs slightly between institutes and a variety of vendors have been used. The sensors were produced, tested and diced in industry. The ROC wafers were also produced in industry, but were tested by CMS before further processing took place. The under bump metallization and solder ball deposition on either the sensors or the ROCs was mainly performed by industry, with the exception of one center that carried out the solder ball deposition in-house. The ROCs were then flip-chip mounted to the sensor, either in-house or by external companies. After assembly a

bare module test was done and in some institutes the faulty ROCs were replaced. If applicable, base strips were glued to the bare module. The HDIs, which were produced by an external company, were tested by CMS before they were glued to the modules. The final production step included the wire bonding of the TBM and ROCs to the HDI, followed by another electrical test. In the BPIX detector a protection cap made of Kapton was then glued to components on the HDI in order to protect the wire bonds from any damage during installation. This was necessary because in the BPIX the detector cables are routed such that they pass over neighboring modules. The mass production of pixel modules started in summer 2014 and was finished around summer 2016.

Every pixel module was extensively tested to ensure its usability for the detector. A grading scheme with three different grades was introduced and the necessary test setups were developed for the qualification procedure. The modules were thermally cycled for 10 times between -25°C and $+17^{\circ}\text{C}$ in a setup using a cold box. Electrical tests were carried out at the foreseen operating temperature of -20°C before and after cycling, and also at room temperature after cycling. During these tests the sensor IV curves were measured and the number of defective pixels was counted. Various DAC settings were optimized and stored in a database to be used during detector operation. An X-ray setup was used to carry out high rate tests to find defective pixels and to measure hit efficiencies. In addition, the fluorescence lines of different targets were used to perform an energy calibration of the chip internal charge injection mechanism. In this context the concept of using didactic X-ray tubes for testing silicon detectors has been established. These tubes are much cheaper than the ones used in industry but still offer large enough hit rates to allow the BPIX modules in layers 2-4 to be tested. These modules were tested up to 150 MHz/cm^2 .

Results from the final testing of the modules in BPIX layers 2-4 are shown in Figure 4. In the X-ray tests the efficiency is above 99% for a hit rate of 120 MHz/cm^2 , as expected for layer 2. The bump bonding quality was found to be good, with a mean value of the number of defective pixels per module of 24 out of 66560 pixels (0.036%). The overall production yield from a working sensor to a fully functioning complete module is around 80%. The main reason why modules did not meet the required quality criteria was because of a failure in the X-ray tests.

Figure 4. X-ray hit efficiency for modules in BPIX layers 2-4, interpolated to 120 MHz/cm^2 (left), and number of defective pixels per module (right).

5 Integration and Commissioning

The integration of the sub-detectors was done in Switzerland (BPIX) and in the USA (FPIX). The integration procedure included placing the components of the power system, the optical links and the modules onto the support structures. Figure 5 shows an assembled half shell of the barrel detector as well as one quarter of the forward detector.

In the final checkout procedure at CERN about 98% of all channels were found to be functional. This procedure included the verification of the module programmability and readout as well as current measurements. In addition to that, several more advanced functionality tests and calibrations were carried out for FPIX. Every test was performed twice, at room temperature and again with the CO₂ cooling temperature set to -15°C (-20°C for FPIX). The detector was afterwards successfully installed into CMS in March 2017. The final calibration and fine-tuning of the operation parameters as well as the integration of the detector into the global CMS DAQ is ongoing, with the expectation that the detector will be ready for physics data taking by the time the first LHC beam injections take place in May 2017.

Figure 5. Left: Photograph of three fully integrated half disks, corresponding to one quarter of the FPIX detector [8]. Right: Photograph of a completed BPIX half-shell as seen from the interaction point.

6 Summary

A new pixel detector for the CMS experiment has been developed. It has almost twice the number of channels, and features upgraded readout chips that will ensure that high tracking efficiency is maintained until Long Shutdown 3 takes place in 2024. The detector comprises an evaporative CO₂ cooling system and a novel DC-DC conversion-based power system. More than 2000 pixel modules have been built and tested. The detector was installed in CMS during the extended year-end technical stop 2016/2017.

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