Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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Abstract: The LHC high-luminosity upgrade in 2024-2026 requires the associated detectors to operate at luminosities about 5-7 times larger than assumed in their original design. The pile-up is expected to increase to up to 200 events per proton bunch-crossing. To be able to retain interesting physics events at electroweak energy scales, increased trigger rates are foreseen for the ATLAS detector. At the hardware selection stage acceptance rates of up to 1 MHz are planned, combined with longer latencies up to 40 micro-seconds in order to read out the necessary data from all detector channels. The current readout of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities. For these reasons a replacement of the LAr front-end and off-detector readout systems is foreseen for all 182,500 readout channels, with the exception of the cold pre-amplifier and summing devices of the hadronic LAr Calorimeter. The new low-power electronics must be able to capture the triangular detector pulses of about 400-600 nano-seconds length with signal currents up to 10 mA and a dynamic range of 16 bits. Results from performance simulation of the calorimeter readout system for different options and results from first tests of the components are presented.
1 Introduction

The ATLAS experiment [1] uses fine-grained lead, copper and tungsten – liquid argon sampling calorimeters for central and forward electromagnetic and forward hadronic calorimetry. At electromagnetic shower maximum, the “middle layer”, the cell size is \( \Delta \eta \times \Delta \phi = 0.025 \times 0.025 \). The liquid argon calorimeters (LAr) consist of approximately 180,000 cells.

Since the drift time in the liquid argon is 400–600 ns, much longer than the 25 ns bunch-crossing time, an RC-CR\(^2\) shaping with time constant of approximately 20 ns is applied to the analog signals to minimize sensitivity to both pile-up and electronics noise. This results in a \( \sim \) 100 ns positive pulse followed by a \( \sim \) 400 ns negative lobe.

The current LAr readout architecture is built of front-end boards [2], installed on the cryostats to minimize noise pick-up, that implement three-gain analog amplification and signal shaping followed by an analog pipeline sampling the signal every 25 ns. For every bunch-crossing selected by the Level-1 trigger, four samples around the bunch-crossing are digitized, and the data are transmitted over a 1.6 Gbps optical link. Off-detector, the digitized waveform is processed [3] in DSPs using an optimal filtering technique to determine each cell’s energy and timing for the selected bunch-crossing.

\(^{1}\)ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upward. Cylindrical coordinates \((r, \phi)\) are used in the transverse plane, \(\phi\) being the azimuthal angle around the z-axis. The pseudorapidity is defined in terms of the polar angle \(\theta\) as \(\eta = -\ln \tan(\theta/2)\). The rapidity is also defined relative to the beam axis as \(y = \frac{1}{2} \ln \left( \frac{E+p_z}{E-p_z} \right) \).
The current front-end boards are incompatible with ATLAS’ trigger upgrade plans: they limit the first trigger level to 2.5 $\mu$s latency and 100 kHz readout rate, whereas maintaining trigger thresholds compatible with electroweak and Higgs physics requires $\sim$ 40 $\mu$s latency and 1 MHz readout rate. Since a component-level FEB upgrade is not possible, all 1524 front-end boards (FEB) need to be replaced. This implies replacing the on-detector calibration boards [4] and off-detector electronics.

2 Front-End Electronics

2.1 Key Front-End Specifications

Specifications for the readout electronics are driven by the calorimeter performance requirements. The dynamic range must be large enough to measure MIPS ($\sim$ 50 MeV in a cell) at the lower end for intercalibration, as well as the highest possible energy deposited by an electron or jet without saturating ($\sim$ 3 TeV), i.e. approximately 16 bits. The linearity must be better than 0.1% up to 10% of the dynamic range, but can be somewhat worse at higher energies. The electronics noise must remain well below the intrinsic calorimeter resolution, which implies $\sim$ 11-bit precision at high energy. To allow for future trigger evolution beyond the initial HL-LHC specifications, the pipelines are moved off-detector. Assuming the dynamic range is realized using two gain scales of 14-bit dynamic range each, $\sim$ 1.3 Gbps need to be transmitted off-detector for each channel, or $\sim$ 180 Gbps for each FEB, or $\sim$ 275 Tbps for the full LAr system.

2.2 ASIC Development

2.2.1 Preamplifier-Shaper

Two architectures are being pursued. The first one, called LAUROC, consists of a new line terminating preamp with dual range output and an electronically cooled resistor, as shown in Fig. 1. A test chip, implemented in TSMC 130 nm CMOS and containing various transistor sizes, capacitor types and protection diodes is undergoing first tests. Its linearity meets the specifications: better than 0.1% at high gain and within 1% up to 7 mA current (larger than the maximal physics signal), and its input impedance has little dependence on the input current and is programmable as designed. A second approach, dubbed HLC1, uses a fully differential amplifier with passive feedback, and is also shown in Fig. 1. A complete test chip, which includes programmable peaking time, ADC driving capability, summed outputs for the trigger path, a programmable pulse generator and a shaping stage, is implemented in TSMC 65 nm CMOS and was submitted for fabrication in April 2017. Both architectures will be tested using the same test benches, and the choice of architecture and technology is planned for late 2017.

2.2.2 Analog to Digital Conversion

For a two gain architecture, to ensure 11-bit precision at high energy each ADC channel needs to have 14-bit dynamic range. Its power consumption must be less than 100 mW per detector channel and its latency as small as possible, preferably within 40 MHz clock cycles. An ADC is being developed in TSMC 65 nm CMOS. The core ADC block is built from a Dynamic Range Enhancer (DRE) followed by a 12-bit Successive Approximation Register (SAR) ADC. The DRE block is
similar to a $4 \times$ amplifier, but with its baseline at $-V_{fs}/2$, where $V_{fs}$ is the ADC’s maximum input voltage. The SAR is implemented in two stages, one resolving 5 bits and the next 8, with an $8 \times$ residue gain between the two. A single channel test chip containing the DRE, SAR and radiation-tolerant output drivers will be submitted for fabrication in May 2017. After that, yearly submissions are expected, gradually including additional functionality blocks (PLL, Vref drivers, etc.), until the final prototype submission with $4 \times 2$ ADC channels in 2020.

In parallel with the ASIC development, a market survey has identified twenty 14-bit and seven 16-bit commercial ADCs that satisfy the power consumption and cost requirements. The devices are made by different vendors and in some cases have higher sampling rates than 40 MSPS. For those, analog multiplexing would be necessary. Irradiation tests of a subset of these devices is planned for 2017 to see if one or more satisfies the LAr radiation tolerance requirements. For commercial devices this means no loss in performance after a total ionizing dose of 3.3 kGy and non-ionizing energy loss dose of $2.7 \times 10^{13} \text{n}_{eq}/\text{cm}^2$, combined with sensitivity to single event effects such that no upsets are observed in exposure to $5.1 \times 10^{12} \text{h}/\text{cm}^2$. For ASICs, the corresponding requirements are 1.0 kGy, $2.7 \times 10^{13} \text{n}_{eq}/\text{cm}^2$ and $5.1 \times 10^{12} \text{h}/\text{cm}^2$.

### 2.2.3 Data Transmission

To minimize loss of accuracy due to intercalibration between analog gain scales, data from both gains will be transmitted off-detector for digital processing. This implies transmitting $\sim 180$ Gbps from each FEB, which will be achieved using the CERN-developed lpGBT serializer in combination with the Versatile Link+ transmitter. The lpGBT offers 8.96 Gbps data bandwidth out of 10.24 Gbps total bandwidth (in FEC-5 mode), with encoding allowing forward error correction. Twenty lpGBT chips are needed on each FEB for data transmission. The LAr group contributes to the development of the VCSEL array driver ASIC, and a first prototype shows excellent performance and radiation tolerance. An iteration is underway to address a few small issues.
2.3 Front-End Boards

The architecture of the FEBs themselves will largely be modeled on the current FEBs, with clear analog/digital separation and extensive attention to grounding and shielding. As opposed to the current FEBs, the number of single points of failure will be minimized by having multiple independent sections with only power shared. The boards will also each have direct clock and slow control links to off-detector electronics, removing the need for a local control bus as well as a control board, which is a full crate single point of failure. This means that in addition to the twenty lpGBT chips for data transmission, each FEB will have two or four lpGBTs for clocks and slow controls. There will thus be $\sim 35,000$ fibers from the front-end system to off-detector ATCA-based electronics.

3 Low Voltage Power Distribution

In the current system, the front-end electronics are powered using high-to-low voltage DC-DC converters located near the front-end crates, in an inaccessible location. These power supplies convert 280V to 11V and lower voltages, providing $\sim 2.5$ kW to each crate. For the HL-LHC upgrade, operating voltages for the FEB components under consideration are in the 1 – 2.5V range. The final down-conversion, from 12, 24 or 48V, is expected to be done on the FEBs themselves using point-of-load converters. In this case, it may be possible to move the main DC-DC converters to a more accessible, lower radiation location by converting the 280V to this intermediate voltage.

Also here, two approaches are pursued: R&D on a custom solution focuses on developments based on Si power MOSFETs and GaN transistors, which are now able to handle high voltages and high currents. In parallel, some newer commercial components are very promising. A VICOR module has passed neutron radiation test, and while it does not have sufficient tolerance to total ionizing dose, at a location further removed from the calorimeter itself its tolerance could be sufficient.

4 Off-Detector Electronics

The off-detector electronics must receive and decode the data, calculate each cell’s energy and time from the digitized waveform, suppressing electronics and pile-up noise, while taking into account each bunch crossing’s position in the accelerator train structure. The system will rely on modern communications and FPGA technology and will be modeled on the Phase-I digital processing system [5]. That uses ATCA Advanced Mezzanine Cards (AMC), each with an ARRIA10 FPGA and 96 optical links connected using micropods. In the Phase-I case, half the links are used for inputs from the front-end electronics (at 5 Gbps) and half for outputs (at 11.2 Gbps) to the Level-1 trigger system. For HL-LHC a higher input link density is needed to achieve at least 3 Tbps input bandwidth per ATCA blade, and a smaller fraction of the input data will need to be sent to the first trigger level.

Since the waveform’s full history will be available off-detector, more advanced filtering techniques will be possible to suppress noise. Fully simulated waveforms with up to 200 interactions per bunch crossing and configurable bunch pattern are used in filtering studies. These include
realistic noise and digitization and are used to study shaping and sampling rate options, the performance of different digital filtering schemes, etc.

5 Summary

For operation in the HL-LHC phase, all LAr electronics will need to be replaced as the current version cannot meet trigger latency and rate requirements, which would have a very negative impact on ATLAS’ HL-LHC physics reach. Front-end electronics R&D is focused on crucial ASICs: for the preamplifier-shape, test chips for multiple architectures have been fabricated; an ADC ASIC will be submitted for fabrication in May 2017; the CERN-developed lpgbt will be used for data serialization and transmission. Off-detector electronics will be modeled on developments from the Phase-I upgrades, but scaled for technological progress.

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References


