**Large Hadron Collider and the ATLAS detector**

- The Large Hadron Collider (LHC) is a proton-proton collider with 14 TeV center of mass energy and design luminosity of $10^{34} cm^{-2} s^{-1}$.
- A series of upgrades have been planned which will have an increased average luminosity 5-7 times larger than the nominal Run-2 value.
- The ATLAS detector is one of the two general purpose particle detectors at the LHC, and it consists of multiple sub-detectors which are designed to detect interesting particle physics events in 40 million bunch-crossings per second.

**ATLAS Tile Calorimeter**

- It is the central section (1.7 < eta < 1.7) of the ATLAS hadronic calorimeter.
- Its purpose is to measure energies and directions of hadrons, $\tau$ jets and leptons.
- It is comprised of two Extended Barrels and a central Long Barrel divided in two sections each divided into 64 slices. Made out of alternating the steel plates and scintillator tiles. Wavelength shifting fibers coupled to the tiles collect the produced light and are read out by photomultiplier tubes (PMTs).

**Upgrade of the ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC**

Ignacio Asensi Tortajada on behalf of the ATLAS Tile Calorimeter System

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### Upgrade of the Phase II

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**Status**

The three test-beam campaigns in 2015 and 2016 tested the performance of the upgrade electronics with very good results.

- Radiation tests are underway without failures so far.
- Calibration of the redesigned 3-in-1 board shows a strong performance for the upgrade system.
- Achieved linearity is 0.3% and equivalent energy resolution is less than 0.1%.
- It is the baseline for the Demonstrator project. The unique option that provides analog output to Trigger towers.

### Main Board - Specific for each FEB

- Interface between FEB and Daughter Board
- Control of CS and Cesium calibrations
- Includes LV levels with POL regulators

### Demonstrator Minidrawer

- Housing for PMT blocks
- Redesigned chassis and cable carrier for easy repair
- Water cooled body with modular design
- Legacy Trigger board for backwards compatibility

### Tile PreProcessor (PPr)

- Provides communication from Back to Front End
- Each PPr operates one TileCal module with 48 PMTs
- Saves data in pipelines waiting for trigger decision
- After acceptance the events are buffered, packed and sent to the Read Out Drivers for backwards compatibility
- Signal reconstruction and Interface with Atlas Data Acquisition System
- Trigger, timing and control signals to PEB
- Data flow and control implemented over Ethernet using IPBus protocol

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**New Front End electronics**

- 2 units for 48 PMTs
- 1 unit for 45 PMTs
- 1 + 1 links for 48 PMTs

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**Front End Boards (FEB) – Three options**

- Processes PMT signals
- Slow integration for Cesium calibration
- Charge Injection System (CIS) calibration

### Upgraded 3-in-1

- Pulse Shaping with discrete components
- Bi-gain amplification (1x, 32x)
- Analog trigger output

### QIE: Charge conveyor in ASIC chip

- No pulse shaping
- Signal digitization

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**FATALIC in ASIC design**

- Dedicated poster in ANIMMA 2017
- Active pulse shaping
- Tri-gain (1x, 8x, 64x)
- Signal digitization

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**Main board**

- Low Voltage Power Supply (LVPS)
  - 10V feeder to each half Main Board
  - More modular redundancies
- High Voltage Regulation (HV)
  - Two options
  - Remote HV
    - Off-detector
    - External HV for each PMT
  - Local HV/ HV Opto
    - In-detector radiation resistant HVopto board
    - HV supplied to 6 PMTs

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**Daughter Board – Same design for all FEB options**

- Control and Configuration of the minidrawers
- Data serialization and transfer
- Reduction (2x, 4x, 8x)
- Dual QIEP + links to PEB
- Clock synchronization

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**Upgrade System**

- Energy distribution for 100 GeV electrons
- Electron signal response

**Remote HV**

- 100 GeV electron beam
- Main board signal response

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**ANIMMA 2017**

**Liege, Belgium**