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Characterisation of capacitively coupled HV/HR-CMOS sensor chips for the CLIC vertex detector

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Abstract

The capacitive coupling between an active sensor and a readout ASIC has been considered in the framework of the CLIC vertex detector study. The CLICpix Capacitively Coupled Pixel Detector (C3PD) is a High-Voltage CMOS sensor chip produced in a commercial 180 nm HV-CMOS process for this purpose. The sensor was designed to be connected to the CLICpix2 readout chip. It therefore matches the dimensions of the readout chip, featuring a matrix of 128×128 square pixels with $25 \mu\text{m}$ pitch. The sensor chip has been produced with the standard value for the substrate resistivity ($\sim 20 \Omega\text{cm}$) and it has been characterised in standalone testing mode, before receiving and testing capacitively coupled assemblies. The standalone measurement results show a rise time of $\sim 20 \text{ ns}$ for a power consumption of $5 \mu\text{W/pixel}$. Production of the C3PD HV-CMOS sensor chip with higher substrate resistivity wafers ($\sim 20, 80, 200$ and $1000 \Omega\text{cm}$) is foreseen. The expected benefits of the higher substrate resistivity will be studied using future assemblies with the readout chip.

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1 Introduction

The concept of capacitive coupling between an active sensor and a readout ASIC has been considered in view of a system suitable for the vertex detector at the Compact Linear Collider (CLIC) [1]. The vertex detector is the innermost active component of the CLIC detector, and given its location close to the interaction point, the requirements are highly demanding in terms of spatial resolution, material budget and power consumption. In particular, these requirements include a spatial resolution of $\sim 3 \mu\text{m}$, a material budget of $0.2\% X_0$ per detection layer and a power consumption limited to 50 mW/cm^2 . A time-stamping resolution of 10 ns is required for the readout chip. The requirement for material budget indicates that both the sensor and the readout chip need to be thinned down to $50 \mu\text{m}$ each. In order to achieve the required power consumption, the system can exploit the low duty cycle of the CLIC beam. By implementing a power pulsing scheme, where the most power consuming nodes of the front-end are powered down between subsequent bunch trains, the average power consumption over the 50 Hz cycle can be minimised.

In a High Voltage CMOS (HV-CMOS) device [2], all circuitry is placed within a deep N-well such that it is isolated from the P-type substrate. This allows the application of a relatively high (several tens of Volts) reverse bias voltage to the substrate, without affecting the operation of the circuitry. Biasing the junction between the substrate and the deep N-well with a high reverse bias voltage results in the formation of a relatively thick ($\sim 10 \mu\text{m}$) depleted region. The charge in the depleted region is collected by drift, as opposed to diffusion which is the case for standard CMOS sensors [3]. The detector can thus benefit from the fact that the drift component is collected quickly due to the strong electric field in the depleted region. In addition, since most of the charge is collected in the depleted region, the substrate can be thinned down to a few tens of microns without affecting the sensor performance.

While in monolithic detector applications [2] all analogue and digital circuitry can be implemented inside the deep N-well, in a capacitively coupled HV-CMOS sensor the charge is amplified by a Charge Sensitive Amplifier (CSA) and is then transferred through a thin layer of glue to the readout chip for further processing [4]. The two chips are precisely aligned and glued together by applying a thin layer of epoxy glue between them. A capacitance is therefore formed between the coupling pads of the sensor and readout chips, allowing for the voltage pulse at the output of the HV-CMOS sensor to be detected and processed by the readout chip. The benefit of this approach compared to a monolithic detector is that the digital circuitry can be decoupled from the sensor by means of placing all the (fast-switching) digital logic in the readout chip. Thus, noise injection to the sensor due to the digital circuitry can be avoided. Compared to hybrid pixel detectors with planar sensors, the complications and cost of bump-bonding the sensor to the readout chip are overcome by glueing the two chips together. However, the trade-off is that complications are added at readout system level, as both chips need to be controlled at the same time.

The HV-CMOS sensor chip presented in this document, the CLICpix Capacitively Coupled Pixel Detector (C3PD), was designed to match the footprint of the CLICpix2 readout chip [5]. It therefore features a matrix of 128×128 square pixels with $25 \mu\text{m}$ pitch. Both the sensor and the readout chips are the successors of a first generation of chips that have been designed and tested in capacitively coupled assemblies in the framework of the CLIC vertex detector studies [6, 7].

2 The C3PD chip

2.1 Overview of the C3PD chip

The C3PD chip [8] has been produced in a commercial 180 nm HV-CMOS process. For this process, the depleted depth is expected to be $\sim 10 \mu\text{m}$, with the standard resistivity ($\sim 20 \Omega\text{cm}$) for the bulk silicon substrate and the nominal applied bias of -60 V . As shown in Figure 1, all transistors are placed in a deep N-well which shields the electronics from the high voltage bias of the substrate, and also acts as the collecting electrode. When designing in such a process, it is important to take into account that placing

the PMOS devices in the deep N-well can result in a parasitic coupling between every P+ diffusion and the deep N-well. In order to avoid this undesired coupling, the area occupied by PMOS transistors has been minimised for the design of the C3PD pixel.

Figure 1: Schematic cross-section of a capacitively coupled assembly. Reproduced from [8]. © IOP Publishing Ltd. All rights reserved.

In view of the CLIC vertex detector requirements, the C3PD chip features a power pulsing scheme, a fast rise time (~ 20 ns) to ensure that the charge transferred through the coupling capacitance will be fully integrated within the CLICpix2 shaping time, and a sufficiently high charge gain. A gain above 120 mV/ ke^- was targeted to provide an amplified charge well above the minimum threshold of the readout chip such that the detector efficiency is not compromised.

The collected charge is integrated in the C3PD front-end and then capacitively coupled to the readout chip through the capacitance formed by the glue layer that is applied between the two chips (C_{out} in Figure 1). As shown in Figure 2, the front-end in the HV-CMOS sensor consists of a charge sensitive amplifier (CSA) followed by a unity gain buffer. An NMOS transistor is used as the resistive feedback (R_{fb} in Figure 2), forcing the output node to return to the baseline after the hit (continuous reset). In the layout, the pixel is surrounded by a metal guardring which is used for biasing the substrate.

The pixels are grouped in double columns, where the two rightmost double columns of the pixel matrix feature variations of the regular pixel. A pixel with a simplified biasing scheme, and another with a metal-to-metal coupling capacitance instead of the regular CMOS gate capacitance (C_{coup} in Figure 2) have been implemented and will be tested in capacitively coupled assemblies with the readout chip.

For the C3PD digital interface, the configuration of internal registers is realised using a standard I^2C protocol [9, 10]. Several features were added to provide maximum testability for the prototype, such as the option to monitor or overwrite internal biasing voltages, test pulse injection to individual pixels, and a 3×3 cluster of pixels that can be monitored directly in the analogue signal domain. The monitored pixels are placed in the bottom-right corner of the regular pixel matrix and have their outputs multiplexed and driven to the wire-bond pads using unity gain buffers placed in the analogue periphery. One of the pixels has the test pulse signal connected to its output, bypassing the front-end, allowing for a direct monitoring of the injected test pulse. A power pulsing scheme has been implemented, such that the front-end can be set to a "power-off" state between subsequent bunch trains in order to minimise the average power consumption over the 50 Hz cycle. The block diagram and a microscope photo of the C3PD chip are presented in Figures 3(a) and 3(b) respectively.

Figure 2: C3PD pixel block diagram. Reproduced from [8]. © IOP Publishing Ltd. All rights reserved.

Figure 3: (a) Block diagram (Reproduced from [8]. © IOP Publishing Ltd. All rights reserved.) and (b) microscope photo of the C3PD chip.

2.2 Submission with higher resistivity wafers

Following the first C3PD submission, a second one took place with higher values for the substrate resistivity. The C3PD sensor chip will be produced on wafers with $\sim 20, 80, 200$ and $1000 \Omega\text{cm}$ resistivity. The effects of using the higher substrate resistivity are expected to be beneficial for the sensor, as the depleted volume will increase. This will subsequently lead to a larger amount of charge collected quickly, due to the increased drift component, along with a decreased sensor capacitance [11]. In addition to the higher resistivity, a layout modification took place, in order to achieve a higher breakdown voltage. The metal contact of the HV-guardring surrounding the pixel was shrunk from $4.8 \mu\text{m}$ to $2.6 \mu\text{m}$ width. According to TCAD simulations, this modification is expected to contribute to increasing the breakdown voltage and thus allowing a higher sensor bias. The higher applied bias along with the increased substrate resistivity will result in a larger depleted volume.

The expected benefits of using higher resistivity wafers will be confirmed with beam tests, once the chips are fabricated and capacitively coupled assemblies are produced.

3 Measurements with bare C3PD chips

Before receiving assemblies with the CLICpix2 readout chip, a standalone characterisation was performed for the C3PD chip using a lab setup with bare C3PD chips wire-bonded on a PCB. The results of the standalone characterisation using bare chips have been reported in [8]. Apart from the internal test pulse injection, the bare chips have been measured using a ^{55}Fe source. The results have shown an average charge gain of 190 mV/ke^- , an RMS noise of 40 e^- and a rise time of 20 ns for a power consumption of $\sim 5 \text{ } \mu\text{W}$ per pixel. After enabling the power pulsing scheme, the average power consumption is reduced to $\sim 16 \text{ mW/cm}^2$. Apart from the standard thickness of $250 \text{ } \mu\text{m}$, a few samples have been thinned down to $50 \text{ } \mu\text{m}$. Testing the $50 \text{ } \mu\text{m}$ thick samples confirmed that thinning down the chips does not impact on their performance. This result is promising considering the required material budget at the CLIC vertex detector.

4 Measurements with C3PD in a capacitively coupled assembly

Following the first results using bare chips, C3PD was tested using a capacitively coupled assembly with the readout chip such that the effects of coupling the two chips together can be studied. Before acquiring data from the readout chip, a test of the C3PD analogue performance took place in order to compare with the results observed in the bare sensor chip. An assembly with the C3PD chip capacitively coupled to the CLICpix2 readout chip was used for this set of measurements. The chips were wire-bonded on a custom designed PCB, which was then connected to the data acquisition system [12]. Figure 4 presents the capacitively coupled assembly wire bonded on the PCB. The measurements were performed with both chips operating in continuous power mode (without power pulsing).

In the following paragraphs, results from lab measurements using the C3PD internal test pulse injection are presented. Testing the chip using the ^{55}Fe source was not possible for this setup due to the fact that the C3PD is glued to the readout chip. A standard thickness ($250 \text{ } \mu\text{m}$) sensor chip was used for this assembly and, as mentioned in section 2.1, the depleted depth is expected to be about $10 \text{ } \mu\text{m}$. Consequently, more than $200 \text{ } \mu\text{m}$ of silicon would stop the photons from the ^{55}Fe source from penetrating through the backside of the sensor into the depleted region, making it difficult to illuminate the pixels.

Figure 4: Capacitively coupled assembly of C3PD (top) and CLICpix2 (bottom), wire bonded on the PCB.

4.1 I-V characteristic

As a first step, the I-V characteristic of the sensor was studied scanning the applied reverse bias and measuring the leakage current for the full chip. In Figure 5, the leakage current is plotted as a function of the applied high voltage bias, for the measured capacitively coupled assembly compared with two bare

chips (one with the standard thickness and one thinned down to 50 μm). The breakdown voltage occurs close to an applied bias of -70 V, while the leakage current for the nominal bias of -60 V is ~ 40 nA (measured for the full chip, at room temperature, corresponding to ~ 300 nA/cm²). This value is within the expected variations observed during the measurements performed for bare chips, thus showing that connecting the two chips together does not affect the sensor characteristic.

Figure 5: I-V curve of the measured C3PD chip.

In addition to the leakage current, the noise at the output of the C3PD amplifier was measured as a function of the high voltage bias using one of the monitored pixels. As expected, the noise is suppressed when applying a higher reverse bias since the depletion depth becomes larger and therefore the sensor capacitance is decreased. Figure 6 shows the measured output noise as a function of the applied bias.

Figure 6: Noise at the amplifier output as a function of the high voltage bias.

4.2 Test pulse injection

In order to study the response of the amplifier to injected test pulses of different amplitude, two of the monitored pixels were used. The first measurement was performed using the pixel with direct monitoring of the test pulse. Figure ?? shows the measured amplitude for the injected test pulse as a function of the injected test pulse DAC code. As confirmed with simulations, the non-linearity observed for the lower DAC codes is an effect of the buffer in the analogue periphery that is used to drive this signal to the wire-bond pad. Following this measurement, the amplitude at the preamplifier output was measured as a function of the injected test pulse, as shown in Figure ?. The injected charge presented on the x-axis was extracted based on the design value of 0.8 fF for the test pulse injection capacitance (C_{test} in Figure 2).

In Figure 7, the output pulse is presented for different charges injected using the internal test pulse injection. The signal rise time is fast (of order 20 ns) such that the transferred charge will be fully integrated by the CLICpix2 front-end amplifier. The slow return to baseline helps to ensure that the transferred charge will not be removed before being integrated.

Figure 7: Output pulses (averaged over 16 samples) for different charge injected using test pulse.

4.3 Calibration using test pulses

The performance of the front-end was studied as a function of the biasing voltage for different nodes (preamplifier, unity gain buffer, feedback) in order to find the operating point where the Signal-to-Noise ratio (SNR) is maximised. In addition, the rise time has to be fast enough to ensure that the charge will be fully integrated by the CLICpix2 preamplifier, and the power consumption needs to be kept at a reasonably low level. This calibration is similar to the one performed for the bare C3PD chip [8], this time taking into account the additional load resulting from having the sensor chip capacitively coupled to the readout ASIC. Figure 8 presents some example plots of the DAC scans that were performed in order to optimise the C3PD operating point for the capacitively coupled assembly. The feedback bias was overwritten by an externally provided voltage, so that a bias voltage higher than the one of the internal circuit would be reached. The maximum voltage that can be provided by the the internal feedback biasing circuit has been increased for the version of the chip submitted with higher resistivity wafers (targeting for a maximum voltage of ~ 730 mV, instead of the 550 mV of the current version).

The measured output amplitude, noise and rise time are presented in Table 1. The output amplitude and the rise time were measured as the mean value of 16 samples, while the RMS noise is the mean RMS value over 10 seconds of sampling with the oscilloscope. When the chip is operated in continuous power mode, the power consumption was estimated to be approximately $5 \mu\text{W}$ per pixel. During power pulsing, the front-end can be switched off, reducing the power consumption down to 95 nW per pixel. The resulting power consumption averaged over the 50 Hz duty cycle of the CLIC collider is $\sim 16 \text{ mW/cm}^2$ (assuming a $30 \mu\text{s}/20 \text{ ms}$ duty cycle). Compared to the bare chips, the main difference observed was in the noise performance of the front-end. Additional load is added at the output of the C3PD front-end due to the coupling capacitance between the two chips in series with the input capacitance of the CLICpix2 front-end. As expected, this results in a higher noise at the output of the preamplifier. However, after optimising the operating point, the output noise can be adjusted to comparable levels to those observed for bare chips. Other characteristics of the front-end, such as gain, rise time and power consumption are within the variations observed during the characterisation of bare C3PD chips. Measured, as well as simulated, values from the standalone characterisation of bare chips (before receiving assemblies with CLICpix2) are presented in [8].

Figure 8: (a) Output noise of the preamplifier as a function of the feedback bias, (b) rise time as a function of the unity gain buffer bias, (c) output amplitude and (d) noise as a function of the charge sensitive amplifier bias for the measured C3PD chip.

Table 1: Pixel characteristics, averaged for all monitored pixels of the measured assembly, measured with test pulses of 1.63 ke^- (charge equivalent to the most probable energy of the photons from an ^{55}Fe source).

Parameter	Average	Standard deviation
Amplitude [mV]	278	6.44
Noise RMS [mV]	7	1.4
SNR	42	7.4
Gain [mV/ ke^-]	170	3.9
Rise time [ns]	17.6	0.8

5 Summary and further testing with the readout chip

The CLICpix Capacitively Coupled Pixel Detector (C3PD) has been tested in standalone mode, first using bare chips and subsequently using capacitively coupled assemblies. Laboratory measurements on the C3PD chip capacitively coupled to the CLICpix2 readout chip have shown an average charge gain of 170 mV/ke^- and an RMS noise of 7 mV , while the measured rise time is 17.6 ns . By enabling a power pulsing scheme, the average power consumption for the pixel matrix is limited to $\sim 16 \text{ mW/cm}^2$ over the 50 Hz cycle of the CLIC beam. Both capacitively coupled and bare chips have been measured to be within the requirements for the CLIC vertex detector.

Assemblies with the readout chip have been produced and the performance of both chips (sensor

and readout) will be characterised over laboratory measurements and beam tests. By connecting to the readout chip, testing of the C3PD HV-CMOS sensor will not be restricted to monitoring the analogue front-end for a limited number of pixels and therefore further characterisation can be performed. Pixel-to-pixel mismatch, top-down effects and homogeneity across the pixel matrix will be studied using capacitively coupled assemblies.

A version of the C3PD chip is currently under production with higher resistivity wafers ($\sim 20, 80, 200$ and $1000 \Omega\text{cm}$). Once the chips have been fabricated and capacitively coupled assemblies have been produced, further tests will be carried out towards a study of the expected benefits on the charge collection and sensor efficiency.

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