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Module and electronics developments for the ATLAS ITk pixel system

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ABSTRACT: The ATLAS experiment is preparing for an extensive modification of its detectors in the course of the planned HL-LHC accelerator upgrade around 2025. The ATLAS upgrade includes the replacement of the entire tracking system by an all-silicon detector (Inner Tracker, ITk). The five innermost layers of ITk will be a pixel detector built of new sensor and readout electronics technologies to improve the tracking performance and cope with the severe HL-LHC environment in terms of occupancy and radiation. The total area of the new pixel system could measure up to 14 m², depending on the final layout choice, which is expected to take place in 2017.

In this paper an overview of the ongoing R&D activities on modules and electronics for the ATLAS ITk is given including the main developments and achievements in silicon planar and 3D sensor technologies, readout and power challenges.

KEYWORDS: Large detector systems for particle and astroparticle physics, Radiation-hard detectors, Particle tracking detectors

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1 Introduction

The LHC will be upgraded around 2025 to the High Luminosity LHC (HL-LHC) raising the integrated luminosity from 300 fb^{-1} to 4000 fb^{-1} [1] in 10 years of operation. This upgrade is motivated by the need for more accurate measurements in the Higgs sector, searches for new particles and to open the sensitivity window to rare events that can point to new physics beyond the Standard Model. To achieve this, the accelerator is facing exceptional technological challenges like the use of 13 Tesla superconducting magnets, ultra-precise cavities for beam rotation and 300m-long lines with the lowest possible dissipation [1].

Experiments like ATLAS [2] and CMS [3] must be upgraded together with the LHC to cope with the significant increment of the peak luminosity $\mathcal{L}_{HL-LHC} = 7.5 \times \mathcal{L}_{LHC} = 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, the expected average pile up (interactions on a single crossing) of 200 and the radiation fluences around $2 \times 10^{16} \text{ neq cm}^{-2}$ expected in the innermost pixel layer. To be able to cope with the new conditions, the ATLAS tracking system will be replaced by an all-silicon detector (Inner Tracker, ITk), the five innermost layers of which will be made of pixel detectors.

In this work, the ongoing activities within the ATLAS ITk project towards the new pixel modules and the off-detector electronics will be presented. The R&D activities within the collaboration are currently focusing on producing promising results to be included in the ITk pixel system Technical Design Report (TDR) due at the end of this year.

2 Pixel Module R & D

The baseline pixel module for the ITk is a hybrid device where the sensor is interconnected to the ASIC readout chip. Extensive R&D campaigns are currently ongoing covering readout chip, sensor technologies, interconnection challenges and CMOS detectors. In this section a brief overview of these activities is given, highlighting a few of the most relevant results achieved to date.

2.1 Readout Chip

The last pixel front-end development within the ATLAS collaboration was the FEI4 chip [4], which is now used as the readout chip for the Insertable B-layer (IBL) included in the ATLAS inner detector in 2015 [5]. However the FEI4 doesn't fulfill the requirements for the ITk pixel system, therefore a new on-detector readout chip is being developed in the context of the RD53 collaboration [6].

Some of the requirements for the new front end electronics to work in the ITk conditions are that it needs to be designed in the 65nm CMOS technology to cope with the expected radiation doses and for the correct operation under the expected high peak luminosity and data rate. The pixel granularity needs to be increased reducing the pixel unit size. A low in-time threshold ($1000e^-$) operation is also required since thinner sensors and high radiation damage are foreseen. The data rate per ASIC can reach up to 5 Gbps and the new readout chip will operate in serial powering, so a shunt LDO regulator [7] needs to be implemented on it.

There are several small demonstrators already under test implementing some of these characteristics while a big demonstrator is expected by the end of this year. Together with the readout chip also planar and 3D sensors are being re-designed and produced with reduced thicknesses and cell sizes of 50×50 or $25 \times 100 \mu m^2$, compatible with the RD53 chip layout.

2.2 Sensors

The main technological challenge faced on the sensors sector, especially for the innermost pixel layers, is the high radiation dose expected and its implications on power dissipation and hit efficiency. A hit efficiency of 97% is requested at the end of the experiment life and the power dissipation must be kept low enough to avoid thermal runaway during operation.

To decrease the power dissipated per module, the current consumption and the operational bias voltage of the sensor must be minimized. Several sensor prototyping productions are being carried out at the moment in collaboration with commercial vendors to identify the best technologies for the different pixel layers.

3D Technologies. 3D silicon sensor technology [8] is the prime candidate for the innermost pixel layer of the ATLAS ITk where the expected fluences will reach $1.4 \times 10^{16} n_{eq} cm^{-2}$ considering the foreseen replacement of the two innermost layers around half the lifetime of the detector. In Figure 1 a cross-section of a planar (left) and a 3D (right) pixel sensor are shown [9]. The working principle is the same for both technologies [10] and the only differences are in the geometry and manufacturing technology.

The geometry of a 3D sensor makes the inter-electrode distance independent of the sensor thickness and it can be one order of magnitude smaller than the device thickness. In this way, lower depletion voltages are required to operate the sensors which translates to lower power consumption, and the charge collection is faster providing less trapping. Another advantage of this technology is that the field in the sensor edges is very well defined due to the electrode geometry having by design slim edges that reduce gaps between sensors in the final modules. There are also some disadvantages to this technology, namely longer production times and lower production yields compared to planar technologies, both of which increase the final sensor cost.

Figure 1. Transverse section schematics of silicon p-in-n pixel sensors. Left: Planar technology where electrodes are separated by the sensor thickness. Right: 3D technology, where the electrodes are embedded in the silicon bulk and the inter-electrode space is decoupled from the sensor thickness [9].

3D silicon pixel sensors were for the first time included in a collider experiment in 2015, when 20 % of the detectors of the IBL were made on 3D technologies [11], thereby showing their feasibility. Since then, they have been included in ATLAS-AFP [12] and in CMS-TOTEM [13].

The HL-LHC will require 3D sensors with reduced pixel size, decreased inter-electrode space and smaller-diameter electrodes. For the ITk the technology is moving from a cell size of $50 \times 250 \mu\text{m}^2$ to either 50×50 or $25 \times 100 \mu\text{m}^2$ [14].

Small pitch 3D sensors have been investigated before and after irradiation up to $1.4 \times 10^{16} n_{eq} \text{cm}^{-2}$ showing excellent detection efficiency [15] and power dissipation in comparison with IBL like 3D sensors (see Figure 2). On the left graph it is shown that 3D sensors with the RD53 layout can achieve a hit efficiency of 97% when operated with bias voltages lower than 120V. On the right graph results of the power dissipation are shown where an improvement can be appreciated with respect to the IBL-like 3D sensors.

All these results on 3D pixel sensors look very promising but more characterization will be requested once we have the next generation frontend chip (RD53), which will allow testing of full modules and irradiation campaigns up to $2 \times 10^{16} n_{eq} \text{cm}^{-2}$.

Planar Technologies The planar silicon technology (see Figure 1 left) used in the ATLAS-IBL is a prime candidate for the ATLAS ITk pixel. A major difference with respect to the n-in-n planar pixel sensors implemented in the present ATLAS tracker is the n-in-p technology that allows for a single sided processing and it is more cost-effective. To decrease the operational bias voltage and hence the power consumption in planar silicon technologies, a sensor thickness equal to or less than $150\text{-}200 \mu\text{m}$ is foreseen for the outer layers, where high yield and low costs are required, and $100\text{-}150 \mu\text{m}$ in the inner layers ones where radiation hardness is the major concern.

The main challenges in this technology are making multi-chip modules with thin sensors and thin

Figure 2. This graphs [15] show how the new 3D sensors with RD53 chip layout reach a 97% hit efficiency (left) after a fluence of $1.4 \times 10^{16} n_{eq} cm^{-2}$ with bias voltages below 120 V. In the right plot, the power dissipation is also lower for the new generation of 3D pixel sensors compared to IBL-like sensors.

ASICs; at the moment modules are formed by four FE-I4 chips and one sensor where the sensor layout is either compatible with the FE-I4 or adapted to the next-generation frontend chip (RD53) with 50x50 or 25x100 μm^2 pixel cell sizes.

An extensive characterization campaign is ongoing within the pixel ITk collaboration to study different bias structures, bias ring configuration, high incidence angle and radiation hardness. In this work only two results are highlighted and shown in Figure 3. On the left plot, the hit efficiency for thin n-in-p planar pixel sensors after being irradiated nearly up to HL-LHC fluences ($\phi = 1 \times 10^{16} n_{eq} cm^{-2}$) has been measured for two different sensor thicknesses of 100 μm and 150 μm ; the required voltages to achieve a 97% hit efficiency are about 500 and 800 V respectively. The right plot shows the impact of the biasing structures on the hit efficiency after irradiation up to $3 \times 10^{15} n_{eq} cm^{-2}$. Depending on the bias structure the hit efficiency can locally drop as low as 50% after irradiation even applying 1000 V for biasing. These results show the importance of doing this R&D studies prior to starting the final module production.

Interconnection A particularly challenging aspect of the ITk pixel module assembly is the sensor-chip interconnection given the large area to be covered and the compressed production schedule. The ITk collaboration have chosen bump-bonding as the chip-sensor connection technique. With this technique, hybrid pixel detectors are manufactured using micron-scale bumps made of metal alloys that solder the ASIC to the pixel sensor via a high temperature reflow process. The metallic layers are deposited in ASIC and sensors in a wafer stage, preferably in the vendors sites, then the wafers are diced and the chip is flipped on top of the sensor. It is foreseen that this flip-chipping could take place in several ITk institutes thereby potentially reducing the final cost of the modules.

To satisfy the yield requirements when using 100-150 μm thin chips with the higher bump density and the larger chip wafer size (12" for the 65 nm CMOS technology compared to 8" for the 130 nm CMOS) several studies are being carried out within the ITk collaboration.

One of the challenges of the bump-bonding technique is that it requires high temperatures

Figure 3. Left: hit efficiency versus bias voltage for thin planar sensors after a fluence of $1 \times 10^{16} n_{eq} cm^{-2}$ [16]. Right: The effect of different bias structures on the hit efficiency [17].

and given the thin ASIC and its composition, including several different internal metal layers, it bows due to the thermal stresses during the process. It has been shown that the use of backside compensation layers can mitigate this effect [18]. In Figure 4 this effect is shown for a 100 μm thick FE-I4 chip (black solid line), without bumps (red dotted line) and with the stress compensation layer (blue dashed line) during three thermal cycles.

Figure 4. ASIC bow as a function of temperature for 100 μm thick FE-I4 chip with and without stress compensation layer [18].

CMOS technologies An alternative module concept under consideration for the ITk is monolithic HV or HR CMOS sensors. The ITk CMOS collaboration is actively investigating this technology, which is a candidate for the outer pixel layers of the ITk and offers a significant cost reduction with respect to traditional hybrid pixel detectors because it can be manufactured in 12" CMOS standard technology, avoiding the hybridization by integrating the readout electronics in the sensitive volume.

The technological advantages of CMOS detectors are that they reduce the material budget and the power consumption and it is a very flexible technology that allows testing many different

126 readouts and pixel schemes at a very low cost. Many prototypes are still in process of qualification
127 for the ITk TDR, more details are given in [19, 20].

128 3 Off detector electronics

129 The pixel off detector readout electronics will be implemented in the framework of the general
130 ATLAS trigger and DAQ system [21]. It will consist of firmware-based components on the
131 receiving end of the FE electronics; a distribution system for timing, trigger and command; and a
132 data handling part connected via a commodity multi-gigabit network. The same system is used to
133 calibrate the detector modules during operation to adjust for radiation-induced changes in sensors
134 and electronics.

135 Because of the very high radiation level inside the detector, the first part of transmission has to be
136 implemented electrically with signals to be converted for optical transmission at larger radii.

137 3.1 Data rate

138 For efficient readout of the data, especially in the innermost layer where the hit occupancy is highest,
139 a readout system serving a data rate of several Gb/s is under development. Simulations based on
140 the expected hit rates and the foreseen performance of the RD53 chip indicate that a readout speed
141 of up to 5 Gb/s per data link (FE-chip) is necessary in the innermost layers decreasing to 640 Mb/s
142 for the outer layers.

The data rate is defined by the chip frequency, the number of chips per cable, the average number of hits and the size of the hit information:

$$DataRate = \frac{1}{< RO >} * ChipFreq * 1.05(32bit * < NHits >)$$

143 where the factor 1.05 is the current estimation of the header size and $< RO >$ corresponds to
144 the average expected occupancy of a region of interest for a given trigger.

145 The data rate per link will scale with the frequency and with the number of chips per cable.
146 In order to handle the expected data rates, it is crucial for material budget estimations to calculate
147 the number of cables needed per pixel layer. Simulations are currently taking place considering the
148 expected occupancy in the HL-LHC and the new pixel size.

149 3.2 Serial Powering

150 To save material in the servicing cables, serial powering is the baseline option for the ITk pixel
151 system and extensive tests are being carried out with FE-I4 modules. Serial powering is made
152 possible by the dedicated shunt-regulators (Shunt-LDO) implemented already in the IBL chip that
153 enables operation with a constant current as needed for serial powering. To avoid losing a whole
154 chain in case of a single module failing, a special protection chip is being developed to switch on/off
155 individual modules; this protection chip will be placed on or near the module.

156 Significant progress has been made in manufacturing a first mini-stave prototype implementing
157 the serial powering. Figure 5 shows the first full-size prototype of the bus tape to carry six serially
158 powered quad modules has been fabricated. A test beam was carried out at CERN SPS facilities
159 where one module made of four FE-I4 chips (a quad module) was read out while three more in

the chain were fully powered and operational, the used DAQ system was the HSIO2-cosmic. Data analysis is currently ongoing to study the effect of serial powering on the data lines.

Figure 5. A picture of a mini stave prototype. The ATLAS-Pixel collaboration has manufactured the first full-size prototype of the bus tape to carry 6 serially-powered quad modules. The tape is a 25mm wide double-sided PCB.

4 Summary

The HL-LHC requires a challenging upgrade to the current ATLAS Inner Detector due to higher peak and integrated luminosity, pile up and data rate. The ATLAS inner detector will be upgraded to the so-called ATLAS Inner Tracker (ITk), whose Technical Design Report (TDR) is due at the end of this year.

In this paper, module and electronics challenges facing the ITk have been described as well as some of the extensive R &D activities being carried out within the collaboration to deal with the foreseen conditions in the HL-LHC.

Acknowledgments

This paper would never have been possible without the contributions of all the colleagues and institutes who form the ATLAS ITk collaboration. I would like to specially acknowledge all the colleagues who provided material and are working on the various topics discussed here.

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