The upgraded Trigger and Data Acquisition (TDAQ) system of the ATLAS experiment at the LHC will improve the capability of the detector to select the events with the greatest scientific potential. The Fast Traktor (FTK) is one of the ATLAS TDAQ upgrades that is presently under commissioning. FTK is a custom hardware system that feeds the High Level Trigger (HLT) with charged particle tracks reconstructed from hits in silicon detectors at the rate of 10^6 events per second. The main processing element of FTK is the Associative Memory (AM) system that is used to perform pattern matching with a high degree of parallelism. Its implementation is called the AM Board Serial Link Processor (AMBSLP) and it is a very efficient pattern matching machine that handles massively parallel data.

The AMBSLP consists of two types of boards: the Little Associative Memory Board (LAMB), a mezzanine where the AM chips are mounted, and the Associative Memory Board (AMB), a 9U VME motherboard that hosts four LAMB daughter-boards. We report on the complex FPGA firmware design that has been implemented to operate the high degree of parallelism of the board. We also report on the commissioning status of the AMBSLP and on the performance of the Processor during early data taking.

**FTK in ATLAS TDAQ**

The Fast Traktor (FTK) [1] will receive data from ATLAS silicon tracking detectors via a dedicated board at 2Gb/s, with an expected data rate of 6400Mbits/sec per chip. The data distribution is controlled by an Artix-7 XC7A200T Xilinx FPGA (blue square). The patterns are collected and sent to the AMBSLP output by another Artix-7 XC7A200T FPGA (red square and red arrows). Both the FPGAs execute monitoring and error detection functions. Monitor data and error flags are also added to the output stream.

The AMBSLP has 850 serial links, with ~1 Tbit of global data traffic.

- The AM system will perform 120 Petabits of compression per second
- Typical high usage power consumption is 250 W per AMBSLP

**AM Boards**

The AM system [2, 3] is made up of 128 AM Serial Link Processors (AMBSLPs). The AMBSLP is composed of a motherboard (VME 9U) with 4 daughterboards, that each holds 64 AMChips. The main purpose of the AMBSLP is to distribute inputs to all the 64 AMChips (blue arrows). This data distribution is controlled by an Artix-7 XC7A200T Xilinx FPGA (blue square). The patterns are collected and sent to the AMBSLP output by another Artix-7 XC7A200T FPGA (red square and red arrows). Both the FPGAs execute monitoring and error detection functions. Monitor data and error flags are also added to the output stream.

Input and output data are transmitted on 2 Gb/s serial links. The AMBSLP has ~850 serial links, with ~1 Tbit of data traffic.

- The AM system will perform 120 Petabits of compression per second
- Typical high usage power consumption is 250 W per AMBSLP

**Integration Status**

The AMBSLP is currently being integrated at CERN. Testing procedure applied before each new component is included in the system. Firmware first tested in Pisa, then in a full FTK slice (1 board per type for a complete processing chain) as part of an integrated TDAQ test system at CERN. Once tested, firmware is then deployed to the primary system in the ATLAS service cavern. Stringent and rigid testing procedure in Pisa and/or CERN for all boards before they are deemed suitable for use. Full FTK slice processing up to 12 layer tracks is under commissioning. A partial FTK slice including the AMBSLP (IM-9-AMB) can process real data for hours. Further commissioning is ongoing.

**FTK Processing Units**

The FTK core is made of 128 Processing Units composed of an Associative Memory board (AM) and an Auxiliary Card where the functions of the second step are executed: the Track Finding (TF), the Data Organiser (DO), the interface between ATLAS FTK and the Hit Warrior (HW) able to remove duplicate tracks found by the TF.

**Advanced Monitoring Functions**

In order to monitor and debug such a complex system several advanced monitoring functions have been implemented on the AMBoard FPGAs:

- Synchronization of the 12 parallel input data streams
- Event number (Level-1 Identifier) monitoring
- Error checks of the input data streams
- Backpressure controls for board to board communication
- Real time temperature monitoring
- Real-time error monitoring of the system
- Timing measurements (latency in data distribution and processing)

Block diagram of the input-output interface for the data distribution FPGA firmware.

**Production Status**

Currently there are ~200 LAMBS at CERN and ~70 AMBs. The target for Run 2 is 64 AMBs available with 256 LAMBS and spare boards for back up. This will cover the full ATLAS detector for Run 2 with half of the full FTK computing potential.

Assembly of the remaining LAMBS is now starting.

**FTK System Goals**

2017:

- Primary Goal: Establish stable full slice processing
- Validate 8-layer (pattern recognition) output with data and simulation

2018:

- Integration with ATLAS for 50% of computing potential

**Results**

We designed a massive pattern matching computing system, the AM-BLP for the main processing unit of the ATLAS Fast Traktor. This complex system requires advanced monitoring functions that are continuously developed through firmware and software. The first production for enough system components to cover the whole ATLAS detector at half the computing potential is already complete, with the boards being integrated at CERN. We have achieved stable event running for hours using prescaled events and we are ready for the next integration target.

**References**


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