An Updated Front-End Data Link Design for the Phase-2 Upgrade of the ATLAS Tile Calorimeter

Samuel Silverstein, Eduardo Valdes Santurio, and Christian Bohm for the ATLAS Tile Calorimeter System

Abstract—We present a new design for the advanced Link Daughter Board (DB) for the front-end electronics upgrade of the ATLAS hadronic Tile Calorimeter. The DB provides control, configuration and continuous ADC readout for the front-end through bi-directional multi-GB/s optical links with the off-detector readout system. The DB will operate in high luminosity LHC conditions with limited detector access, so the design is fault tolerant with a high level of redundancy to avoid single-point failure modes. The new design is based on the new Xilinx Kintex Ultrascale+ FPGA family, which provides improved high-speed link timing performance and radiation tolerance, as well as better signal compatibility with the CERN-developed GBTx link and timing distribution ASICs. Two GBTx ASICs each provide redundant phase-adjusted, LHC synchronous clocks, parallel control buses and remote JTAG configuration access to the two FPGAs on the DB.

I. INTRODUCTION

THE trigger and data acquisition system (TDAQ) architecture of the ATLAS experiment [1] will be upgraded in conjunction with the high-luminosity upgrade of the Large Hadron Collider (LHC) [2]. The upgrade is necessitated by the expected 5-7 fold increase in the number of proton collisions per bunch crossing compared with the original LHC design parameters. Interesting physics events will be overlaid by a correspondingly larger number of minimum-bias collisions, making it more difficult to distinguish them from background. The detector and electronics will also be subjected to corresponding increases in minimum ionizing particle and neutron radiation.

To improve event selection, the first-level calorimeter trigger system (L1Calo) will require calorimeter trigger tower inputs with higher resolution and less sensitive to out-of-time energy deposits and other pile-up effects. To achieve this for the hadronic Tile Calorimeter (TileCal), the current front-end electronics will be replaced by a new system [3] designed to provide continuous readout of all digitized photomultiplier (PMT) data samples to the off-detector Pre-Processor (PPR), where they will be stored in pipeline buffers and digitally summed into trigger towers for transmission to L1Calo. Modern FPGAs and multi-Gb/s optical transceivers provide the increased readout link bandwidth required.

Because of limited accessibility and extended operation in a radiation environment, the new system is designed for improved reliability and fault tolerance. Radiation tolerant

components are used, and redundancy is implemented throughout the system to avoid data corruption and single-point failure modes.

II. TILECAL FRONT-END ELECTRONICS UPGRADE

TileCal is segmented into 5182 calorimeter cells that are read out by two PMTs each, one for each side of the scintillator tiles. For the upgraded system design, the PMTs will be installed in 1024 so-called “mini-drawers” (MD), largely independent mechanical blocks inserted into the rear girders of the 256 wedge-shaped calorimeter modules (Fig. 1). Each MD hosts up to 12 PMTs as well as the associated electronics for HV distribution, calibration, digitization and readout.

The PMT block outputs in each MD are received by a 12-channel front-end Main Board (MB). A control and readout link Daughter Board (DB) receives digitized ADC samples from the MB at approximately 40 Msamples/s through a 400-pin FMC connector. The MB and DB are both electrically and functionally divided lengthwise, with each half responsible for control, calibration and readout of the PMTs on its respective side of the calorimeter module. The sides are independently powered by separate supplies, so that a single voltage failure will not remove an entire cell from being read out. Additional redundancy is implemented in the control and data readout data paths to avoid single point failure modes in the front-end system.

Research and development has been ongoing, with three different front-end concepts and two high-voltage distribution options evaluated in parallel. A common DB compatible with all readout and HV options has been developed. The last DB version [4] has been shown to satisfy all functional requirements, however design issues encountered in testing, and the availability of the new Kintex Ultrascale+ family of FPGAs motivate a redesign of the DB.

Fig. 1. The mini-drawer mechanics and electronics, and their placement in the hadronic Tile Calorimeter modules

Manuscript received November 10, 2017.

S. Silverstein, E. Valdes Santurio and C. Bohm are with the Physics Department, Stockholm University, 10691 Stockholm, Sweden (e-mail: silver@fysik.su.se).

Fig. 2. Simplified functional diagram of the DB, showing the main components and functional blocks and the interfaces between them. Red lines indicate GBTx and FPGA signals originating from side A, while side B signals are drawn in blue. The violet dashed line represents the common I2C bus connecting both GBTx and FPGA devices.

III. DAUGHTER BOARD OVERVIEW

The DB is partitioned into redundant sides (Fig. 2), each with an FPGA that provides timing, slow control and readout for the corresponding side of the Main Board (MB) through the common FMC connector. Each side also has a GBTx ASIC for providing redundant LHC-synchronous clocks, 8-bit wide configuration and control buses, remote JTAG access and other control signals to both FPGAs.

The GBTx on each DB side receives a 4.8 Gb/s downlink from the off-detector electronics, and each FPGA transmits two redundant copies of its respective ADC output and status data on separate 9.6 Gb/s uplinks. The six active links per DB are connected through optical fiber cables to the off-detector systems via four SFP+ electro-optic transceiver modules [5]. All six links will be connected and active during nominal operations to allow dynamic correction of transient errors in the redundant uplinks; but only a single functioning downlink and one uplink from each FPGA are necessary for full control and readout functionality.

IV. GBTx TIMING AND LINK ASIC

The CERN-developed radiation-hard GBTx timing and link ASIC [6] is designed for 4.8 GB/s bidirectional serial communications. It includes eight differential clock outputs for distributing LHC-synchronous clocks, with selectable frequency (40/80/160/320 MHz) and individual phase adjustment with 50 ps precision. It also provides multiple banks of differential 1.5 V I/O (eLink groups) for local communication with on-board electronics. The ASIC uses a single 1.5 V supply voltage, and all clocks and ePort I/O banks use a 1.5 V Sub-LVDS signal standard.

The DB uses a pair of GBTx ASICs configured to operate in simplex receiver mode. Each GBTx receives a 4.8 Gb/s serial link from the off-detector system, and drives redundant sets of clocks, configuration/control buses, and JTAG configuration chains to both FPGAs.

Each FPGA automatically selects valid clock/configuration inputs based on two single-ended GBTx status pins: RX_READY and DATA_VALID. RX_READY, when asserted, indicates that the GBTx ASIC is receiving and decoding a valid 4.8 Gb/s data stream, and thus correctly asserting clocks and ePort signals. The DATA_VALID signal is encoded by the user in a 4-bit header of the input link data, and is used by the DB to assert priority of one GBTx source over the other.

A. Clock Distribution

The GBTx has eight differential clock outputs that drive LHC-synchronous clocks with independently selectable frequency (40/80/160/320 MHz) and phase adjustment with 50 ps precision. Both GBTx provide each FPGA with a 40 MHz LHC clock for the FPGA real time data path, a 160/320 MHz reference clock for the multi-Gbit/s transceivers (MGT) and two additional phase-adjusted 40 MHz clocks that are forwarded to the MB for ADC and readout timing.

By default, each FPGA uses the two RX_READY signals to select a valid set of clocks from one GBTx. If both GBTx are asserting RX_READY, then priority is given to the same-side source, but this can be overridden through the configuration/control bus.

B. Configuration/Control Bus

Redundant 8-bit configuration/control buses (ConfigBus) are received by each FPGA from both GBTx ASICs, along with associated clocks. ConfigBus uses a synchronous protocol to write commands and configuration data to register addresses within the FPGA in order to configure and control both the DB and MB. Command responses are sent back to the off-detector electronics by the FPGA, encoded in dedicated data fields of the 9.6GB/s uplinks.

The ConfigBus data signals are driven by a combination of ePorts from both output and bi-directional eLink groups, with associated clocks driven from the separate Clock Out groups of the GBTx. While the nominal use case assumes 40 or 80 MHz data rates, the ConfigBus routing uses only even-numbered ePorts, which will allow the data rate to be increased to 160 MHz if required.

The FPGA uses the two RX_READY signals and a Port-Select function in the ConfigBus protocol to arbitrate control between the two GBTx ASICs, in order to avoid unintentional conflicts.

C. Remote JTAG Access and Reset

Each GBTx is also connected through tri-state buffers to the TMS, TCK and TDI signal ports of each FPGAs JTAG chain, and can also assert a RESET signal to trigger an FPGA reconfiguration from the local configuration PROM. Using discrete logic, the two GBTx DATA_VALID are used to arbitrate control of the JTAG bus, with the same-side (local) GBTx given precedence. If neither GBTx asserts

DATA_VALID, the buffers remain at high impedance, allowing local cable access to the JTAG chain.

A copy of the TDO signal is transmitted to the opposite-side (remote) FPGA, where it is sent off-detector through that FPGA's uplinks. If the remote-side FPGA is not operating, the FPGA and PROM may still be configured remotely through "blind" playback of a serial vector file (SVF) without TDO readback and verification.

V. KINTEX ULTRASCALE+ FPGA

The most significant change in the new DB design is the transition from the Kintex 7 FPGA in earlier versions to the new Kintex Ultrascale+ family. The final DB design is based on XCKU3P FPGAs with FFVB676 BGA packages, although the initial prototypes use pin-compatible XCKU5P devices.

A. Transceiver performance

One of the most important motivations for migrating to Ultrascale+ was the Multi-Gb/s serial link timing. The Kintex 7 FPGAs used in earlier DB revisions were capable of stable 9.6 Gb/s data transmission, but the timing limitations of the GTX transceivers did not allow operation with a GBTx-supplied 160 MHz reference clock. Instead, the FPGA acted as a GBT receiver, extracting a 120 MHz LHC clock from a serial input link, and converting it for use in the FPGA logic fabric and the GTX transmitter timing reference. The GTY transceivers in the Kintex Ultrascale+ family do not have this limitation, so in the new DB all input data and timing extraction are migrated from the FPGA to the GBTx ASICs. This is in line with good timing practices as recommended by Xilinx, and reduces the logic size and complexity in the FPGA firmware.

As described earlier, the FPGA receives two MGT reference clocks, one from each GBTx. Based on the RX_READY signals, a state machine driven by a local crystal oscillator clock dynamically switches between reference clock inputs by register value changes, followed by a reset/initialization sequence.

B. Low Voltage Differential Signaling

In the Kintex Ultrascale+ devices used, most of the general-purpose I/O pins are high-performance (HP) banks supporting signal standards up to 1.8 V, including the sub_LVDS standard. As noted above, this provides an ideal match with the 1.5 V GBTx I/O, allowing direct signal connection from the GBTx ePorts and clock outputs to the FPGA, with no level-shifting necessary. The configuration bank is also 1.8 V compatible, allowing the remote JTAG configuration circuitry to be redesigned to run entirely from the 1.8 V supply.

The overall result is a simpler DB design with fewer components and simpler layout, especially in the densely routed area between the GBTx, FPGA and FMC connector.

C. SEU Hardness

Preliminary tests of the earlier Kintex 7 based DB design in proton beam indicated negligible data loss at HL-LHC data taking conditions for a design using Soft Error Mitigation (SEM) as well as triple module redundancy (TMR) for real time data paths. The 20 nm Ultrascale FPGA family has several times higher SEU tolerance with respect to the 28 nm

7-series devices, and the 16 nm Ultrascale+ architecture with FinFET transistors is expected to continue this trend [7][8].

VI. RADIATION TOLERANCE

The DB requirements for 10 years of high-luminosity running are 200 Gy TID, $5.8\text{E}+13$ N/cm² NIEL, and $1.34\text{E}+11$ cm⁻²/yr SEE [9]. Most of the COTS components have already been qualified on other systems; for instance the LTM4619 dual 4A DC/DC regulator has been tested to more than 10 times the TileCal requirement, with abrupt voltage loss (as opposed to overvoltage) as the primary failure mode. We have also successfully tested 65 nm serial NOR flash configuration memories in gamma radiation, with suspected charge pump failures first appearing between 200 and 300 Gy TID.

Radiation tests of the new DB are planned in early 2018, in parallel with beam tests and commissioning at CERN.

VII. OUTLOOK

The updated DB design solves several outstanding issues from earlier board versions, not least of which are the serial link timing and clock distribution. In addition to improved radiation tolerance, we expect the simplified board design and migration to Kintex Ultrascale+ to reduce overall power consumption and make the DB more reliable. Barring unforeseen issues, this new design can be considered a near-final prototype.

Beam tests and radiation qualification of the new DB will be performed in 2018, with final production scheduled to begin in 2020.

REFERENCES

- [1] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider," JINST vol 3, S08003, 2008.
- [2] ATLAS Collaboration, "Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System," Tech. Report ATLAS TDAQ Collaboration, CERN, Geneva, 2015.
- [3] F. Tang *et al.*, "Design of the Front End Readout Electronics for ATLAS Tile Calorimeter at the sLHC," IEEE Trans. Nucl. Sci., vol 60, Issue 2, pp. 1255-1259, 2013.
- [4] S. Muschter *et al.*, "Development of a Readout Link Board for the Demonstrator of the ATLAS Tile Calorimeter Upgrade," JINST vol 8, C03025, 2013.
- [5] SFF Committee, Specifications for Enhanced Small Form Factor Pluggable Module SFP+," Multi source agreement SFF_8431. <http://www.sfplustransceiver.com/pdf/MSA-SFF-8431.pdf>
- [6] P. Moreira *et al.*, "The GBT SerDes ASIC Prototype, JINST vol 5(11), C11022, 2010.
- [7] Xilinx Inc., "Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits," White paper WP286 (v2.0), 2016. <https://www.xilinx.com>
- [8] Xilinx Inc., "Device Reliability Report," User guide UG116 Chapter 1, v10.6.1, 2017. <https://www.xilinx.com>
- [9] H. Åkerstedt *et al.*, "Reliable and Redundant FPGA Based Read-Out Design in the ATLAS TileCal Demonstrator," IEEE Trans. Nucl. Sci., vol 62, Issue 5, pp. 2129-2133, 2015.