1) Introduction

ATLAS is a particle physics experiment at the Large Hadron Collider (LHC) at CERN. The online trigger system of ATLAS is structured in 2 levels to reduce the rate from a bunch crossing (BC) rate of 40 MHz down to 1 kHz written to permanent storage. The Level-1 trigger which reduces the event rate to a maximum of 100 MHz is implemented with custom electronics, while the High-Level Trigger (HLT) is built from commercial computers, network components, and custom software.

2) Level-1 trigger system

The Level-1 trigger system performs fast event selection based on reduced-granularity information from the calorimeters and muon detectors. Information from both calorimeter (L1Calo) and muon (L1Muon) triggers consists of multiplicities, energy flags and position of trigger candidate objects. The level-1 trigger data transfer is based on source-synchronous clocking technique with the clock being distributed on a separate network. This network is implemented by the Timing, Trigger and Control system (TTC). The Muon to Central Trigger Processor Interface (MUCTPI) combines the information from the muon trigger selector logic (SL) through the L1Muon trigger which selects the most promising muons. The L1Muon trigger contains all the required information, such as the most likely momentum, the starting and stopping position of the track, the multiplicity, and the number of counts consistent with the trigger.

3) MUCTPI prototype

The prototype of the upgraded MUCTPI has been tested successfully. All the features including power supply, clock circuitry, FPGA configuration, hardware monitoring, inter-FPGA communication, and the Control SoC were tested without problems or difficulties thanks to extensive preparatory work using development boards. The prototype was tested on a test rig with 28 links running at 6.4 Gbps. The power consumption of the prototype was measured to be 0.5 W.

4) MUCTPI implementation

The new system is based on a highly-integrated generation of FPGAs (Xilinx 20 nm Ultrascale devices), featuring a large number of on-chip multi-gigabit transceivers (47x4G) as well as 12-channel RoI optical fiber optics receiver and transmitter modules (MiniPOD) for the data transfer. The functionality of 8 existing modules, i.e. one half of the detector, has been merged into a single large Virtex UltraScale FPGA (UL100), the Muon Sector Processor (MSP). The two FPGAs together receive and process muon trigger data from 208 sector logic modules connected through high-speed serial optical links using MiniPOD receiver modules. The MSP FPGAs also carry any information on muon trigger objects to several LiTops modules using four 12-channel fiber optic transmitter modules in total. The third FPGA, Kintex UltraScale device (KU903), merges the information received from the two MSP FPGAs through UOS and MCT links, and send the results to the CTP. In addition, it can be used to implement multi-sector topological trigger algorithms. Some FPGA receives, decodes and distributes the TTC information. It sends the muon trigger information to the data acquisition system when it receives a Level-1 accept decision. A smaller Xilinx Zynq UltraScale SoC (ZCU102) is used for configuration, control and monitoring of the module through a Gigabit Ethernet (GbE) interface.

5) SL synchronization & alignment

In order to synchronize data from different muon sectors, the MUCTPI has to compensate the input phase-skew and align the signals in multiples of the bunch-crossing period of 25 ns. First, the bunch crossing clock, trigger, and timing data has to be recovered and locked from the TTC. Second, the SL data is sent to be synchronized and aligned. The following block diagram shows the SL synchronization and alignment firmware. A write control logic block is used to select the SL frame boundary, and dual port memories are used to transfer all the 286 inputs from their respective clock domaining into a single clock domain for combined data processing. This circuit can cope with phase variation of the received data and non-deterministic data latency from FPGA transceivers by monitoring received data timing and setting delay logic in the write control logic. A reduced version of this firmware implemented in a prototype module has tested successfully with the muon SL prototype modules. Currently, the complete version of this firmware has been tested with 72 optical links coming from two different sources will be also tested with the muon SL modules during the next integration tests.

9) Summary

The prototype of the upgraded MUCTPI has been tested successfully. All the features including power supply, clock circuitry, FPGA configuration, hardware monitoring, inter-FPGA communication, and the Control SoC were tested without problems or difficulties thanks to extensive preparatory work using development boards. The prototype was tested on a test rig with 28 links running at 6.4 Gbps. Comparison of the prototype with the 9.6 & 12.8 Gbps was also confirmed. The TTC recovery has been tested and fixed-latency was measured. The muon SL data synchronization & alignment was tested with success using 72 optical inputs from two different sources. Integration tests with the muon trigger sector logic modules will take more time to take into account and optimize latency and resources.