The Phase-2 Electronics Upgrade of the ATLAS Liquid Argon Calorimeter System

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ABSTRACT: The LHC high-luminosity upgrade in 2024-2026 requires the associated detectors to operate at luminosities about 5-7 times larger than assumed in their original design. The pile-up is expected to increase to up to 200 events per proton bunch-crossing. The current readout of the ATLAS liquid argon calorimeters does not provide sufficient buffering and bandwidth capabilities to accommodate the hardware triggers requirements imposed by these harsh conditions. Furthermore, the expected total radiation doses are beyond the qualification range of the current front-end electronics. For these reasons an almost complete replacement of the front-end and off-detector readout system is foreseen for the 182,468 readout channels. The new readout system will be based on a free-running architecture, where calorimeter signals are amplified, shaped and digitized by on-detector electronics, then sent at 40 MHz to the off-detector electronics for further processing. Results from the design studies on the performance of the components of the readout system are presented, as well as the results of the tests of the first prototypes.

KEYWORDS: Calorimeters, Electronic detector readout concepts (liquid), Front-end electronics for detector readout, Radiation-hard electronics.

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1 The ATLAS liquid argon calorimeter system

The ATLAS detector [1] liquid argon (LAr) calorimeter system [2–5] consists of several different fine-grained sampling calorimeters of different geometry and that use different absorbing material. The LAr calorimeter system covers the pseudo-rapidity region $|\eta| < 4.9$. The calorimeters are segmented both laterally and longitudinally and are used to provide a measurement of the energy of particles such as electrons, photons and hadrons. The LAr calorimeter system has a total of 182,468 individual readout channels.

The high luminosity LHC [6] (HL-LHC) data taking period is scheduled to begin in 2026, after a two years shutdown period during which both the LHC and detectors, such as ATLAS and CMS, will undergo major upgrades. During HL-LHC operation, peak instantaneous luminosity of up to $7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ are expected, resulting in approximately 200 inelastic proton-proton collisions every 25 ns. A total data sample of approximately $4,000 \text{ fb}^{-1}$ will be recorded over a period of about 10 years.

In order to take advantage of the physics opportunities under these challenging experimental conditions, major upgrades [7] to the ATLAS detector are foreseen. While the LAr calorimeters are expected to continue to operate reliably for the entire HL-LHC data-taking period, both the front-end and off-detector readout electronics will need to be replaced for two primary reasons. First, the current LAr calorimeter readout electronics is incompatible with the planned upgrade to the trigger system which is necessary to meet the physics goals of the ATLAS experiment at HL-LHC. The current readout is limited to a $2.5 \mu\text{s}$ level-1 trigger latency and maximum readout rate of 100 kHz, while the new system must be compatible with a level-0 (level-1) trigger latency of 10 (35) μs and a maximum readout rate of 4 (0.8) MHz. Secondly, the existing LAr calorimeter front-end electronics components are not qualified for operation at the high radiation doses expected at the HL-LHC and would simply not survive. For these reasons both the front-end on-detector as well as the back-end off-detector electronics need to be replaced.

2 Electronics readout at HL-LHC

The new LAr calorimeter readout electronics must satisfy the following requirements. First, the readout electronics must provide the ability to measure a wide dynamic range of energies, driven by the physics needs of the experiment. The ability to measure the energy of minimum ionizing particles (MIP) for calibration purposes defines the low end of the dynamic range, while the high end is defined by the maximum cell energy that would be expected in the search for a hypothetical high mass particle. This corresponds to the ability to measure cell energies in the range of a few tens of MeV all the way up to a few TeV. The high end of the dynamic range sets the requirement on the maximum input current that the pre-amplifiers will need to be able to cope with. The energy scale of the ATLAS LAr calorimeter is set using collisions producing Z bosons and events containing J/ψ particles. Since the energy scale is extrapolated to lower/higher energies based on these measurements, stringent requirements are set on the linearity of the electronics readout. More specifically, the readout electronics is required to achieve linearity at the per mille level for up to approximately 10% of the dynamic range (i.e. up to approximately 300 GeV), and achieve a linearity at the level of a few percent at higher energies. In addition, front-end components, which are mounted on the rim of the cryostats, must be radiation hard ¹. Finally, although pile-up noise will dominate at high luminosity, the electronics noise must be kept smaller than signals from MIPs for calibration purposes and to achieve the best possible performance during possible occasional low luminosity physics runs.

Preliminary studies have been performed to optimize the analog shaper characteristics in order to minimize the total noise after digital filtering. The current baseline design is to use a bipolar $CR - (RC)^2$ shaper with a programmable shaping time around the default value of 13 ns.

A new readout architecture has been designed based on these requirements and characteristics. Figure 1 shows a schematic diagram of the new LAr readout electronics for HL-LHC. Raw signals from the LAr calorimeters enter the readout system on the top left of the schematic diagram, and will get processed first by the on-detector front-end electronics, and then by the back-end system located off-detector. The key difference of this design with the current readout electronics is the new free-running scheme where all the data is sent off detector to the back-end system. The back-end system will then integrate sufficient digital buffer space for holding the data while waiting for a trigger decision.

The following sections briefly describe the different main components of this readout architecture and provide the status of ongoing R&D.

2.1 Front-end electronics

The “FEB2” front-end boards will provide input line termination, amplification, pulse shaping, digitization and data transmission to the off-detector electronics. The design of the FEB2 is based on the current front-end board design [8]. The entire LAr calorimeter readout will have a total of 1524 FEB2 boards, each handling 128 channels. The three key ASICs on this board are the pre-amplifier-shaper, the analog-to-digital converter (ADC) and the serializer.

¹For example, the application-specific integrated circuits (ASIC) are required to be radiation hard, including a safety factor, for a integrated total ionizing dose (TID) of 1.24 kGy, a non-ionizing energy loss (NIEL) dose of up to $3.4 \times 10^{13} \text{ neq/cm}^2$, and for up to 1 single event effect (SEE) for $4.6 \times 10^{12} \text{ protons/cm}^2$

Figure 1: Schematic diagram of the LAr calorimeter readout architecture for the Phase-2 upgrade. The LAr Trigger Digitizer Board (LTDB) and LAr Digital Processing System (LDPS) will be installed in the Phase-1 upgrade.

2.1.1 Analog signal processing

The signal pre-amplification and analog shaping will be integrated into one ASIC. There are two parallel R&D projects currently being pursued.

One design, shown in Figure 2a, is implemented in 130 nm CMOS technology. It is a low power low noise line terminating pre-amplifier with dual range output and electronically cooled resistor. A test chip with only the pre-amplifier functionality implemented was received in 2016 and is undergoing tests. The input impedance of a few ohms was demonstrated to be easily tunable by changing the capacitance of the C_2 capacitor. The linearity of the pre-amplifier was measured to be better than 0.5% up to 7 mA² (25 Ω , low gain). The equivalent noise current (ENI) was measured to be about 300 nA, a factor of two larger than expected. This larger noise was identified to be due to additional resistance in the input transistor. A new transistor was designed and successfully tested in November 2017. The next chip submission will include the shaper stage.

The second design is implemented in 65 nm CMOS and includes a fully differential amplifier with passive feedback as shown in Figure 2b. A pre-prototype chip was received in July 2017 which includes both pre-amplifier and shaper stages, programmable termination, two gains and programmable peaking time. A linearity better than 0.2% up to approximately 9.7 mA (25 Ω , low gain) was measured.

Finally, in order to evaluate both ASIC options, a common test system has also been designed and produced. The current plan is to choose the architecture and technology for the pre-amplifier

²A current comparable to the maximum current expected from a new high mass 5 TeV resonance decaying to a pair of electrons.

Figure 2: Schematic diagrams of the design of (a) the line terminating pre-amplifier implemented in 130 nm CMOS process and (b) the fully differential pre-amplifier implemented in 65 nm CMOS process.

and shaper ASIC in 2018.

2.1.2 Digitization

The next step in the electronic readout is the digitization of the shaped analog signals. The digitization scheme adopted consists in digitizing the waveform at 40 MHz using a 14-bit radiation hard ADC. To cover the full 16-bit dynamic range required by the physics needs of the experiment, a two-gain system will be used where each ADC digitizes only part of the range and both outputs are sent to the off-detector electronics. One of the requirements of this analog to digital conversion is that the quantization noise remains smaller than the intrinsic LAr calorimeter resolution in order not to degrade the total energy resolution by more than 5%. This two-gain digitization scheme is shown in Figure 3. The energy at which the gain switching occurs is chosen such that photons from $H \rightarrow \gamma\gamma$ decays have their cell energy falls in the same gain as electrons from Z boson decays used to set the energy scale. This will result in a reduction in one of the dominant uncertainties on the precise measurement of the Higgs boson mass. Additional requirements on the ADC are that it be low power (less than 100 mW/channel at 40 MSPS) and have an integral (INL) and differential (DNL) non-linearities of both less than 1 least significant bit (LSB).

Three options are being explored: a custom ADC ASIC design in 65 nm CMOS, an ADC design based on a commercial IP block, and a commercial off-the-shelf ADC chip.

The advantage of a custom ADC ASIC is to provide a design that can be fully customized for the specific needs of the LAr readout, and that it is the cheaper option. The current design of the custom ADC is based on a dynamic range enhancer (DRE) followed by a 12-bit successive-approximation-register (SAR) converter. Figure 4 shows a schematic diagram of this design. The dynamic range enhancer block is similar to a 4x amplifier. It determines the most significant two bits of the 14-bit digital code. The two-stage SAR architecture provides a 12-bit conversion. ADC

Figure 3: Estimated quantization noise as function of energy in the LAr electromagnetic middle layer in the endcap outer wheel with the proposed two-gain system. The quantization noise curves assume the use of 12-bit SAR with a dynamic range enhancer in order to obtain 14-bit ADCs with 12-bit precision.

test chips were received in August 2017 and are being tested.

Figure 4: (a) Schematic diagram of analog signal processing and digitization of one readout channel. The 14-bit digitization is achieved using (b) a dynamic range enhancer (DRE) block followed by (c) a two-stage SAR ADC.

An ADC design based on a commercial IP block would provide an intermediate approach in the ability to customize the ASIC for the LAr readout needs. The idea would be to use commercially available block(s) with proven analog performance for the critical functionalities of the ASIC and customize the digital interface as needed. This solution would be more costly than a custom ASIC design.

Finally, the most expensive solution would be to purchase a commercial off-the-shelf ADC. This solution would also require additional development to integrate this ADC into the FEB2 architecture. One promising ADC candidate, identified in a market survey, is the Texas Instruments

ADS5294, octal 14-bit ADC, fabricated in 180 nm process and consuming 60 mW per channel at 40 MSPS.

2.1.3 Data transmission

After having digitized the shaped analog signal, all the ADC data need to be serialized and transmitted to the off-detector back-end processor. The data will be serialized at a bit rate of 640 Mbps per channel, which adds up to a total data rate of over 160 Gbps per FEB2. To achieve this, the plan is to use the CERN-based lpGBT [9] chips with the Versatile Link+ optical assemblies [10]. The lpGBT is designed in 65 nm CMOS and is a lower power higher bandwidth version of the GBT [11] chip.

2.2 Off-detector electronics

As mentioned earlier, the full data stream will be sent to the off-detector LAr signal processor (LASP). The general functionalities of the LASP system are to receive digitized waveforms, perform gain selection, apply digital filtering to calculate energy/time of LAr signal pulses, buffer data until a trigger decision and to transmit relevant data to both the trigger and data acquisition systems.

2.2.1 Digital signal processing

The baseline hardware implementation of the LASP system is based on a full-size Advanced Telecommunications Computing Architecture (ATCA) format. A single monolithic ATCA blade will contain two processing units. Each LASP processing unit will receive data from 2 to 4 FEB2 boards and will be equipped with a high-performance FPGA, electro-optical receiver/transceiver arrays operating at different link speeds, and additional memory and clock distribution devices. Given the timescale of the project, the choice of the FPGA is premature, however some FPGA models currently on the market already fulfill the LASP resource requirements.

3 Summary

The readout electronics for the ATLAS LAr calorimeter needs to be replaced in time for the HL-LHC data-taking period. A new readout architecture based on a free-running scheme where all data are sent off-detector to a digital back-end system has been designed. The status and ongoing developments of critical components of this new readout system have been presented. The project is progressing well.

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