The Compact Muon Solenoid Experiment

Conference Report

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Performance of the CMS Phase 1 Pixel Detector

Bora Akgun for the CMS Collaboration

Abstract

It is anticipated that the LHC accelerator will reach and exceed the luminosity of $L = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ during the LHC Run 2 period until 2023. At this higher luminosity and increased hit occupancies the CMS phase-0 pixel detector would have been subjected to severe dead time and inefficiencies introduced by limited buffers in the analog read-out chip and effects of radiation damage in the sensors. Therefore a new pixel detector has been built and replaced the phase-0 detector in the 2016/17 LHC extended year-end technical stop. The CMS phase-1 pixel detector features four central barrel layers and three end-cap disks in forward and backward direction for robust tracking performance, and a significantly reduced overall material budget including new cooling and powering schemes. The design of the new front-end readout chip comprises larger data buffers, an increased transmission bandwidth, and low-threshold comparators. These improvements allow the new pixel detector to sustain and improve the efficiency of the current pixel tracker at the increased requirements imposed by high luminosities and pile-up. A new DAQ system has been developed based on a combination of custom and standard microTCA parts. This contribution gives an overview of the design and performance of the CMS phase-1 pixel detector.

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It is anticipated that the LHC accelerator will reach and exceed the luminosity of $L = 2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ during the LHC Run 2 period until 2023. At this higher luminosity and increased hit occupancies the CMS phase-0 pixel detector would have been subjected to severe dead time and inefficiencies introduced by limited buffers in the analog read-out chip and effects of radiation damage in the sensors. Therefore a new pixel detector has been built and replaced the phase-0 detector in the 2016/17 LHC extended year-end technical stop. The CMS phase-1 pixel detector features four central barrel layers and three end-cap disks in forward and backward direction for robust tracking performance, and a significantly reduced overall material budget including new cooling and powering schemes. The design of the new front-end readout chip comprises larger data buffers, an increased transmission bandwidth, and low-threshold comparators. These improvements allow the new pixel detector to sustain and improve the efficiency of the current pixel tracker at the increased requirements imposed by high luminosities and pile-up. A new DAQ system has been developed based on a combination of custom and standard microTCA parts. This contribution gives an overview of the design and performance of the CMS phase-1 pixel detector.

Keywords: Silicon Sensors, Tracker, Detector Control Systems, Data Acquisition Concepts, Optical Detector Readout Concepts, Modular Electronics

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1. Introduction

The phase-0 pixel detector of the CMS experiment (1) which operated until 2016 was designed to record efficiently and with high precision the first three space-points near the interaction region up to an instantaneous luminosity of $1.0 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ with 25 ns colliding bunch spacing. The main

goal of the phase-1 pixel project (2) is to have an evolutionary upgrade with minimal disruption of data taking by keeping the pixel size and sensor the same, meanwhile improving the performance by higher hit rate capability of readout chips and data transmission and optimized material budget. The phase-1 pixel detector was designed to maintain a high tracking performance at luminosities up to $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The phase-1 pixel detector with modified data acquisition (DAQ) (3), two-phase CO₂ cooling and detector control systems (DCS) was installed during an extended year-end technical stop in the beginning of 2017 and it is expected to contribute to high performance tracking in the high luminosity environment of the LHC up to Long Shutdown 3 (LS3).

2. Phase-1 Pixel Detector Upgrade Overview

Figure 1: The layouts for phase-1 and phase-0 pixel detectors.

The CMS phase-1 pixel detector has 4 layers in the barrel and 3 disks in the forward region on either side of the interaction point. Figure 1 shows the layouts for phase-1 and phase-0 pixel detectors. An overview of the system architecture including auxiliary components required to interface with the CMS Central DAQ is shown in Fig. 2. The phase-1 pixel detector features a fully digital readout system with new backend electronics. The new readout chips (ROC)s (4) perform zero-suppression on the chip and operate on a 40 MHz clock and have a 160 Mbps serial output data stream. Two

streams of eight ROCs each are multiplexed into a 320 Mbps stream by the token-bit manager chip (TBM). This stream is then encoded using a 4b/5b bit scheme, leading to a 400 Mbps output, to reduce the impact of bit-errors during transmission (5). The output signal of the TBM is converted to an optical signal off the module and transmitted on a fiber to a microTCA Front-End Driver (FED) board located in the counting room which does decoding, deserialization, building of event fragments which are sent to CMS Central DAQ. There are 24 input channels per FED card. The control part of the system requires two different flavors of Front-End Controllers (FEC): the Pixel FEC and the Tracker FEC. The Pixel FEC distributes clock, trigger and fast signals to the pixel modules and in addition is responsible for programming the Digital-to-Analog-Converter registers of the ROCs and the TBM. The Tracker FEC is used to program the registers of the auxiliary electronic components, namely opto-hybrids and DC-DC converters (6) via the Inter-Integrated Circuit (I²C) interface and Parallel Interface Adapter (PIA) port of a Control & Communication Unit (CCU) (7).

Figure 2: Overview of the system architecture of the phase-1 pixel detector. Modules are connected to the port cards via flex or twisted pair cables. There are two different types of optical hybrids on the port cards: a Pixel-Opto-Hybrid, which converts an electrical signal from the modules to an optical signal and delivers it to the FED, and a Digital-Opto-Hybrid, which converts an optical signal from the Pixel FEC to an optical signal to the modules. Registers on the port cards and DC-DC converters, used for powering, are programmed by Tracker FEC via CCUs. The numbers in the parentheses indicate the installed electronics for the forward and barrel parts, respectively.

3. Detector Construction, Commissioning and Calibration

Pixel modules were produced in several centers with a single set of qualification criteria. The barrel pixel detector (BPIX) was assembled in Switzerland (Paul Scherrer Institute and University of Zurich) and the forward pixel detector (FPIX) was assembled in the United States (Fermilab). After the transportation to CERN system tests for both BPIX and FPIX were performed on the surface before installation. After the installation, in order to check the physical connection between the detector and the counting room the light level of the opto-links is varied. Next, clock, data and trigger delays are adjusted. In the checkout, both the 160 Mbps and 400 Mbps phases have been adjusted until a complete data word consisting of the TBM header, a number of ROC headers, and TBM trailer could be decoded in the FED. Finally, test pulses have been injected in individual pixels and read out in order to test the signal path down to the level of the readout chip. Once the full signal path has been established down to the single pixel hit level, ROC parameters such as V_{ana} , CalDel, etc. have been adjusted. See Ref. (8) for details. The threshold of the ROCs for barrel layer 2-4 and the forward disks have been optimized to around 1750 electrons, while for barrel layer 1 the threshold was set to around 3000 electrons due to the higher noise level of the barrel layer 1 ROCs.

The main task after installation was to adjust the relative delays of the barrel layers and forward disks. Relative delays for barrel layer 2-4 and forward disks were adjusted. A new readout chip, PROC600, is designed for barrel layer 1. The PROC600 can handle higher instantaneous luminosities than PSI46dig that is used on barrel layer 2-4 and forward disks. The PROC600 is 12 ns faster than PSI46dig but layer 1 and layer 2 share the same delay chip in a single ϕ -sector which made it difficult to adjust the relative delay. In the end a working point was chosen where the hit efficiency for layer 1 was 98% after increasing the layer 2 HV from 100 V to 250 V.

4. Detector Performance

The CMS phase-1 pixel detector has collected data with 95.7% fully functional channels. During LHC collision running the phase-1 pixel detector has experienced communication losses with port cards and single event upsets on TBMs and ROCs. Communication losses with port cards and single event upsets on ROCs are fixable by reprogramming whereas single event upsets on

TBMs require a power cycle. In order to reduce the dead-time an automatic procedure was implemented for power-cycling and reprogramming.

One of the main motivations for the replacement of the CMS phase-0 pixel detector was the diminishing hit detection performance with the continuous increase of instantaneous luminosity of the LHC accelerator. Hence an important performance benchmark for the new pixel detector is the hit efficiency, here defined as the probability to find a cluster within a 1 mm distance around the expected hit from a track reconstructed in all other layers of the CMS Tracker and a transverse momentum of $p_T > 1.0$ GeV. As shown in Fig. 3, the hit efficiency for layer 2-4 of BPIX and all FPIX disks equipped with the PSI46dig ROC is well above 99% for a large range of instantaneous luminosity. Layer 1 of BPIX, equipped with the PROC600, shows an average efficiency of 99% with a drop at high instantaneous luminosity. Considering the particle rate is up to a factor five higher in this layer, this performance is excellent.

Figure 3: Hit efficiency as a function of instantaneous luminosity for different layers of BPIX and FPIX.

5. Summary and Outlook

During the EYETS 2016/17 the CMS phase-0 pixel detector was replaced with an upgraded detector. The front-end readout chips (PSI46dig) for the outer layers underwent an evolutionary upgrade guaranteeing a consistently high hit efficiency. The fully new developed front-end ASIC (PROC600) for

the innermost layer also performs well with low inefficiencies. The DAQ back-end hardware was completely replaced based on the microTCA standard. The detector shows good performance with high hit efficiency in all layers.

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