STUDY OF RUN TIME ERRORS OF THE ATLAS PIXEL DETECTOR IN THE 2012
DATA TAKING PERIOD

by
Reddy Pratap Gandrajula

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Thesis Supervisor: Professor Usha Mallik

To my Parents

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ABSTRACT

The high resolution silicon Pixel detector is critical in event vertex reconstruction and in particle track reconstruction in the ATLAS detector. During the pixel data taking operation, some modules (Silicon Pixel sensor +Front End Chip+ Module Control Chip (MCC)) go to an auto-disable state, where the Modules don't send the data for storage. Modules become operational again after reconfiguration. The source of the problem is not fully understood. One possible source of the problem is traced to the occurrence of single event upset (SEU) in the MCC. Such a module goes to either a Timeout or Busy state. This report is the study of different types and rates of errors occurring in the Pixel data taking operation. Also, the study includes the error rate dependency on Pixel detector geometry.

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CHAPTER 1

INTRODUCTION TO PIXEL SENSOR AND SEMICONDUCTOR THEORY

1.1. Introduction:

Silicon pixel detectors are used to measure the position of charged particles. Each pixel is a small segmented square on a silicon wafer which is a thin slice of Semiconductor material. The pixel detector in the ATLAS experiment is designed to collect information on particles coming from a point of interest, in our case it is the interaction point where the two proton beams collide, so it's built to surround that point as completely as possible. In the following sections, a basic working principle of a pixel sensor and semiconductor physics theory is briefly discussed. A brief description of the ATLAS pixel detector [1] is given in Chapter 2. A study of the SEU rate in the ATLAS Pixel detector is presented in Chapter 3. The summary of results and conclusions based on the SEU rate study is presented in Chapter 4.

1.2. Basic working principle of a Pixel detector:

An energetic charged particle passing through a pixel detector creates many (thousands or tens of thousands) electron-hole pairs via the electromagnetic interaction. The electron thus created is pulled to one direction (towards the anode) by the applied electric field, while the hole (the empty space where the electron should be) is pulled to the other direction (towards the cathode) as shown in Figure 1. The charge built up on these contacts produces a current which is registered via the electronic readout into the data acquisition system and recorded into the data stream. By studying the data streams

to identify the patterns of pixels that have charge recorded, we can reconstruct the paths of the particles that passed through them. This gives us a very precise measurement of the point at which the particle passed through the detector.

LHC collisions had highest peak instantaneous luminosity around $7.61 \times 10^{33} \text{cm}^{-2} \text{sec}^{-1}$ [2] in 2012 operation. Pixel sensors are designed to withstand intense radiation found right next to the collision region, which can damage the silicon structure. Studies of Single Event Upset (SEU) in pixel readout electronics [3] were performed before LHC operation began. An SEU is the phenomenon of producing an electrical signal with in a micro-electronic device, such as a transistor, when an energetic particle passes directly through it.

Figure 1. Basic working principle of a pixel detector: electrons flow clockwise and holes anti-clock wise. **Source:** [4].

1.3. Brief introduction to semiconductors:

This section discusses the basic properties of semiconductors. A semiconductor is a material which has electrical conductivity between that of a conductor such as copper and an insulator such as glass. In semiconductor production, doping intentionally introduces impurities into an extremely pure semiconductor (also referred to as intrinsic). Adding small quantities of impurity atoms to an intrinsic semiconductor significantly changes the electrical conductivity of a semiconductor. The energy levels of different types of semiconductor materials are shown in Figure 2, where E^p is the energy of a single-electron quantum state drawn along the vertical axis. The number of quantum states per unit energy (Energy density of states “D”) is drawn along the horizontal axis. The valence band is the highest range of electron energies in which electrons are normally present at absolute temperature. The conduction band is the range of electron energy that is high enough to free an electron from binding with its atom to move freely within the atomic lattice of the material. The difference between the valence band and conduction band is the band gap. The minimum energy required for an electron in the valence band to jump into the conduction band is the band gap energy given by E_{gap}^p . States occupied by electrons are shown as states filled with small black circles. At room temperature, due to thermal excitation, some electrons jump to the conduction band leaving “holes” (absence of an electron) in the valence band. Electrical conductivity is possible with either electrons in the conduction band or holes in the valence band.

Figure 2. Band gap spectra of intrinsic and doped semiconductors at room temperature.

Source: [5]

The number of electrons per quantum state is given by the Fermi-Dirac distribution.

$$n_e = \frac{1}{e^{(E^p - \mu)/k_B T} + 1}$$

n_e depends on the energy of the single-electron quantum state, the absolute temperature T , the Boltzmann constant $k_B = 1.38 \times 10^{-23} \text{ J/K}$, and μ is the chemical potential, also known as the Fermi level. The Fermi level is shown by a red tick mark in Figure 2.

Because the number of electrons in the conduction band is small, the average number of quantum states in the conduction band may be simplified to the Maxwell-Boltzmann distribution given by:

$$n_e = e^{-(E^p - \mu)/k_B T} \ll 1$$

Here T is the absolute temperature, k_B is the Boltzmann constant, and μ is the chemical potential. For an intrinsic semiconductor, the Fermi level is about in the middle of the band gap. Therefore with $\mu = \frac{E_{gap}^p}{2}$, the average number of electrons per quantum state at the bottom of the conduction band is

$$n_e = e^{-E_{gap}^p/2k_BT}$$

At room temperature ($T = 293$ K), k_BT is about 0.025 eV and for silicon, the band gap energy is about 1.12 eV. Then the fraction of electrons in the bottom of the conduction band is about 2×10^{-10} . In other words, only one in 5 billion quantum states in the lower part of the conduction band has an electron in it. This is why pure silicon conducts poorly.

Holes are the absence of electrons, so the states that are not filled with electrons in the valance band are given by:

$$n_h = 1 - n_e$$

Plugging the Fermi-Dirac distribution into n_e , we have the expression for n_h .

$$\begin{aligned} n_h &= 1 - \frac{1}{e^{(E^p - \mu)/k_BT} + 1} \\ &= \frac{e^{-(\mu - E^p)/k_BT}}{e^{(E^p - \mu)/k_BT} + 1} \end{aligned}$$

In the valence band, the energy of the single-electron (or hole) is less than the Fermi level μ . Therefore $(E^p - \mu)/k_B T$ tends to $-\infty$ making the exponential $e^{(E^p - \mu)/k_B T}$ go to zero. Thus the average number of holes in the valence band is given by

$$n_h = e^{-(\mu - E^p)/k_B T}$$

Note that when the Fermi level is exactly at the middle of the band gap, the number of the electrons per quantum state n_e in the bottom of the conduction band is the same as the number of holes per quantum state n_h at the top of the valence band. This is what one expects, since the electrons in the conduction band came from the valence band by creating holes in it.

The bottom line here is that pure semiconductors have too few current carriers to have good conductivity. This can be greatly improved by doping the material. Silicon with 4 valence electrons per atom can be doped with an impurity atom with 5 valence electrons. The additional free electron can then easily go to the conduction band and allows additional conduction to occur. Since the valence-5 impurity atoms add electrons to the conduction band, they are called “donors” and the doped semiconductor is called “n-type” as shown in Figure 2. Likewise the semiconductor can be doped with 3 valence electron atoms. Using a bit of thermal energy, holes are created to accept valence band electrons. Therefore the impurity atoms are called “acceptors” and the doped semiconductor is called p-type.

Expressions for the total number of conduction electrons per unit volume and the total number of holes per unit volume are:

$$i_e = 2 \left(\frac{m_{eff,e} k_B T}{2\pi\hbar^2} \right)^{\frac{3}{2}} e^{-(E_c^p - \mu)/k_B T}, \quad i_h = 2 \left(\frac{m_{eff,h} k_B T}{2\pi\hbar^2} \right)^{\frac{3}{2}} e^{-(\mu - E_v^p)/k_B T}$$

Where E_c^p is the bottom of the conduction band energy and E_v^p is the top of the conduction band energy. $m_{eff,e}$, $m_{eff,h}$ are electron and hole effective masses in silicon crystal comparable to true electron mass (0.511 Mev / c^2). The expressions $\left(\frac{m_{eff,e} k_B T}{2\pi\hbar^2} \right)^{\frac{3}{2}}$ and $\left(\frac{m_{eff,h} k_B T}{2\pi\hbar^2} \right)^{\frac{3}{2}}$ are the number of single-electron quantum states per unit energy range per unit volume (density of states) and the number of single-hole quantum states per unit energy range per unit volume respectively.

Equating i_e and i_h , one can compute the Fermi level given by:

$$\mu = \frac{E_c^p + E_v^p}{2} + \frac{3k_B T}{4} \ln \left(\frac{m_{eff,h}}{m_{eff,e}} \right)$$

In an *n-type* semiconductor donor atoms add more energy states just below the conduction band. At room temperature the Fermi level moves up compared to intrinsic semiconductor but stays below the donor states as shown in Figure 2. An increase in Fermi level μ increases the number of electrons per quantum state; in the conduction band thus the combined number of electrons in the conduction band and the donor states is a bit more than the donor electrons. Adding more donors move up the Fermi level. Light doping is of the order of 1 impurity atom in 100 million intrinsic atoms. While heavy doping is 1 in 10,000. If the donor atoms get too close together, their electrons start to interact and donor states broadens into a band, to form a metallic “degenerate” semiconductor.

The upward shift in the Fermi level in *n-type* material makes the number of conduction electrons provided by the valence band smaller still than it was already for the intrinsic semiconductor. Due to this, all conduction band electrons are provided by the donors and almost all electrical conduction is performed by electrons, not holes. The electrons in *n-type* material are therefore called the “majority carriers” and the holes the “minority carriers”. Similarly a *p-type* material with a high number of holes will have very few conduction electrons as shown in Figure 3.

Figure 3. Electron density versus hole density in pure semiconductors have neither conduction electrons nor holes. Source: [5]

CHAPTER 2

THE ATLAS PIXEL DETECTOR

2.1. Introduction:

ATLAS is one of the general purpose high energy particle detectors located in the Large Hadron Collider (LHC) ring at CERN [1]. The high energetic proton beams and luminosity delivered by the LHC collider will produce collisions in the ATLAS detector at high interaction rates, with very high radiation doses, in particular in the proximity of the interaction region, where processes with high particle multiplicities and energies will be produced. The nominal interaction point is defined as the origin of a right - handed coordinate system; where the beam direction defines the z-axis and the x-y plane is transverse to the beam axis as shown in Figure 4. The azimuthal angle Φ is measured around the beam axis, while the polar angle θ_{cm} is the angle from the beam axis.

Figure 4. LHC coordinates.

Usually the angle θ_{cm} is more conveniently expressed in terms of the pseudo-rapidity defined $\eta = -\ln\left(\tan\frac{\theta_{cm}}{2}\right)$.

2.2. The ATLAS Pixel Detector:

The innermost detector, immediately outside the LHC beam pipe, is the silicon pixel detector. As shown in Figure 5, the ATLAS Pixel detector has three concentric cylindrical layers and six end cap disks of detectors inside a magnetic field provided by a superconducting solenoid.

Figure 5. ATLAS Pixel detector geometry with 3 barrel layers and 3 end cap disk layers.

Dimensions are in mm. **Source:** [6]

Figure 6. A schematic view of the active region of the pixel detector consisting of barrel and end cap layers. **Source:** [3]

The Pixel detector is capable of measuring the charged particle positions in spite of the high particle densities, radiation doses, and interaction rates provided by the LHC collisions.

The schematic view of the active region of the pixel detector is shown in Figure 6.

The principle components of the pixel tracking system are given below:

- The active region (3 barrel + 6 end cap disks)
- optical readout systems, power monitoring systems, cooling and mechanical support structures
- pixel support tube
- An external data acquisition systems connected to pixel detector

Figure 7. Block diagram of the pixel detector system. Source: [3]

The basic unit of the pixel detector is the module, composed of silicon sensors, front-end electronics and flex-hybrids with control circuits. All modules are identical to each other. Figure 7 shows the block diagram of the pixel detector system. Each module is connected to the off-detector Read-Out-Drivers through optical- fiber links (opto-links). Figure 8 shows the architecture of the opto-links. The two main components in the opto-link system are the Opto-board, on the detector side, and the Back of Crate Card (BOC), on the off-detector end.

Figure 8. optical link system architecture. Source: [3]

The transmission of the signals from the detector modules to the opto-boards uses Low Voltage Differential Signalling (LVDS) serial links. These electrical connections link the MCC with the VCSEL (Vertical-Cavity Surface-Emitting Laser) Driver Chip (VDC) and the Digital Optical Receiver IC (DORIC) are located on the opto-boards. The communication with each detector module uses individual fibers: one for down-link and one or two for up-links. Trigger, clock, commands and configuration data travel on the down-link, while the event data and configuration read-back data travel in up-link(s). The data transmitted in the up-links are encoded in non-return-to-zero (NRZ) format. Electrical-to-optical conversion occurs in the opto-boards on the detector side and in the optical-receiver (RX) and optical-transmitter (TX) plug-ins in the BOC. In the off-detector part of the links, one BOC serves each ROD. ROD is the next level up in the event readout chain. An overview of the ROD functionality is given in Chapter 3.

The nominal pixel size is 50 microns in the ϕ direction and 400 microns in z (barrel region, along the beam axis) or r (disk region). There are 46,080 pixel electronics channels in a module. The summary of the number of modules, number of channels and active area for pixel barrel layer is shown in Table 1 and for Disks is shown in Table 2.

Table 1. Basic parameters for the barrel region of the ATLAS pixel detector system

Layer Number	Mean Radius [mm]	Number of Staves	Number of Modules	Number of Channels	Active Area [m^2]
0	50.5	22	286	13,178,880	0.28
1	88.5	38	494	22,763,520	0.49
2	122.5	52	676	31,150,080	0.67
Total		112	1456	67,092,480	1.45

Table 2. Basic parameters for the end cap region of the ATLAS pixel detector system

Disk Number	Mean z [mm]	Number of Sectors	Number of Modules	Number of Channels	Active Area [m^2]
0	495	8	48	22,11,840	0.0475
1	580	8	48	22,11,840	0.0475
2	650	8	48	22,11,840	0.0475
Total one end cap		24	144	6,635,520	0.14
Total both end caps		48	288	13,271,040	0.28

As shown in Figure 6, there are 1456 barrel modules and 288 disk modules covering pseudorapidity $-2.5 < \eta < 2.5$, in the radial distance between 5 cm and 12 cm from the collision point. A total of 80 million channels provide data transmission for track recognition capability at LHC design luminosity of $\mathcal{L} = 10^{34} cm^{-2} sec^{-1}$. It is the most important detector used in the identification and reconstruction of secondary vertices from the decay of, for example, particles containing b-quarks, or b-tagging of jets. In addition it provides the spatial resolution for reconstructing primary vertices coming from the proton – proton collisions even in the presence of multiple interactions at the LHC design luminosity.

CHAPTER 3

INTRODUCTION TO ATLAS PIXEL OPERATIONAL ERRORS

3.1. Introduction to Pixel Operational Issues:

The ATLAS Pixel detector has a robust Data Acquisition system (DAQ) to provide high energy particle tracking information. The pixel detector consists of three Barrel layers and three end cap disks on either side of the collision point. The basic component of the Pixel detector is the Pixel Module consisting of silicon sensors bump bonded to Front End (FE) chips. An energetic particle passing through these sensors triggers a hit, and its position information is sent to the Readout-driver (ROD) system, which is the next level of the DAQ chain, via optical links to the off-detector side. A brief description of the Pixel data path is shown in Figure 9.

Figure 9. Readout driver overview. Source: [7]

Each Pixel module contains 16 FE chips connected to a Module Controller Chip (MCC). Hit position information is exported to a Formatter (FMT) which is a Field Programmable Gate Array (FPGA) in the ROD via optical communication links. FMTs perform serial - to - parallel data conversion and derandomize the event fragments. There are 8 FMTs per ROD and each FMT has 4 links connected to Modules operating 40 Mbit/sec, 80 Mbit/sec and 160 Mbit/sec depending on their position in layers and disks. Each link has a First-in-First-Out link (FIFO) buffer that holds the formatted 32 - bit data before sending it to the Event Fragment Builder (EFB). The ROD Controller FPGA (RCF) passes the trigger token to a group of four formatters to initiate data flow to EFB. These FMT link FIFOs expect the data from modules within the trigger set time limit and if the data are not received in the set time window then the corresponding module goes to a “Timeout” state. When the FMT is waiting for data from a certain link, data coming from other links pileup in the FMT FIFO buffer making it overflow, which results a “ROD Busy” error state. The EFB looks for any mismatches between the Level1ID generated from the hits in different modules and the ATLAS Level1ID from the Trigger, Timing & Control (TTC) system and if a mismatch is found it results in a “Module level synchronization error”. Similarly if a mismatch between TTC Level1 ID with bunch crossing ID (BCID) is found a “Rod level synchronization” error results.

Module reconfiguration has proved to be a corrective action for Timeout, Busy and module level Synchronization error states. An automatic mechanism to detect these error states at ROD level and reconfigure that specific problematic module to recover it into data-taking mode is implemented. In the following sections, we present the

performance of this module auto-recovery tool and quantify the rate of occurrences of these error states and their dependency on layer and end cap disk geometry.

3.2. Analysis of the QuickStatus performance:

The following section contains several studies aiming to evaluate the performance of the ROD-level auto recovery system during the 2012 LHC proton-proton collisions run. Section 3.2.1 describes the runs considered in this analysis. Each section from 3.2.2 to 3.2.4 concentrates on studying the rate for a particular type of error; namely, Timeout (3.2.2), Busy (3.2.3), Module level synchronization (3.2.4.1) and ROD level synchronization (3.2.4.2). The results of these studies are then summarized in Section 3.2.5.

3.2.1. Data collection:

The Module Timeout and Busy recovery logic of QuickStatus was deployed in the Pixel Detector during the May 2012 technical stop. The QuickStatus module auto-recovery actions information on Module Timeout and Rod Busy errors was stored in a log file created at the end of each run, in the DSPBuffer directory. One log file is created per run per problematic ROD. The analysis results presented in the following sections were from studying these log files during the three phases of data taking. The 2012 data-taking period can be separated into three phases, each corresponding to an increased functionality of the ROD level recovery system. Phase1 was from May 7th, 2012 to June 18th, 2012; Phase2 was from July 1st, 2012 to August 31st, 2012 and Phase3 was from September 27th, 2012 to November 5th, 2012. During the Phase2 runs, the QuickStatus algorithm was modified to take corrective actions on Module - level Synchronization

(ModSync) errors in addition to Module Timeout and Rod Busy errors, and the corrective actions information was saved in the same log file. During Phase3 runs, QuickStatus was updated to take corrective actions on Rod level Synchronization (RodSync) errors and this actions information was also written to the same log file. The number of runs, the average time per run and the total run time for each Phase can be found in Table 3. Approximately 22% of the log files were lost due to automatic clean up.

Table 3. Run information in the three Phases

Parameters of Interest	Phase1 runs (69)	Phase2 runs (75)	Phase3 runs (42)
Total # runs considered	61	75	42
Total run time in hours	380.95	453.32	223.73
Average run time in hours	6.24	6.04	5.33
Average Peak.Inst.Lumi. in $\text{cm}^{-2}\text{sec}^{-1}$	5.6×10^{33}	5.8×10^{33}	6.35×10^{33}

3.2.2. Module Timeout errors study:

The average Timeout error rate can be computed by counting the total number of Timeout errors in the given Phase of runs and dividing it by the total run time of that Phase. Table 4 shows the summary of Timeout error rates in a given Pixel Layer Module in all three Phases of the run. Here $\#e$ is the total number of Timeout errors occurred in the given Phase of the run in the Pixel detector; $\sum T_n$ is the total run time in hours for the given Phase of the run. The Timeout error rate then is the ratio of $\#e$ and $\sum T_n$. The average Timeout error rate in BLayer for Phase1 runs was 0.19; i.e., approximately one Timeout error in every 5 hours of data taking in BLayer Modules. Whereas in Phase2 and Phase3 runs were 4 hours and 3 hours of data taking respectively; this observation clearly

indicates the increase in Timeout error rate from Phase1 to Phase3. This increase in Timeout error rate was due to the increase of Timeout error contributions from known problematic Modules (Modules connected to the Rods: ROD_B1_S18 and ROD_B1_S9) in BLayer. Also, Table 4 shows the number of Timeout errors per run in each Pixel Barrel Layer and All End cap Disks Modules. Here, $\sum n$ is the total number of runs in the given Phase; i.e., $\sum n = 61, 75$ and 42 for the Phases 1, 2, and 3 respectively. The number of Timeout errors per run is the ratio of $\#e$ and $\sum n$. There was an average of one Timeout error per run in Pixel BLayer Modules for all three Phases of runs.

Table 4. Total Timeout errors in a given Pixel Layer in all the three Phases of runs.

Pixel	Timeouts in Phase1 runs (61)			Timeouts in Phase2 runs (75)			Timeouts in Phase3 runs (42)			Total Runs (178)		
Layers /Disks	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$
BLayer	71	0.19	1.16	110	0.24	1.47	70	0.31	1.67	251	0.24	1.41
Layer1	32	0.08	0.52	43	0.09	0.57	20	0.09	0.48	95	0.09	0.53
Layer2	15	0.04	0.25	24	0.05	0.32	29	0.13	0.69	78	0.07	0.44
Disks	14	0.04	0.23	19	0.04	0.25	9	0.04	0.21	42	0.04	0.24

Figure 10. Timeout errors distribution in a given Pixel Layer in all the three Phases.
Source: [2]

Figure 10 shows the percentage of total Timeout errors in all the three Phases occurred in a given Pixel Layer Modules. A total of 466 Timeout errors were cured by the QuickStatus algorithm during the three Phases (a total of 178 runs); among these 466 Timeout errors, 251 Timeout errors (53.9% of total Timeouts) were in BLayer Modules as expected. Since BLayer Modules are closer to the bunch crossing point, the probability of a single event upset occurring is greater. Next, dominant total Timeout errors were in the Layer1 Modules in which 95 Timeout errors (20.4% of total Timeouts) occurred in all the three Phases of the run.

To make the Timeout error rate independent with respect to the number of Modules in a given Pixel Layer Modules, we normalize the Timeout error rate by taking the ratio of Timeout error rate in a given pixel layer Module and the number of Modules in the respective Layer. The Timeout error rate can be scaled with respect to Layer 2 Modules for better comparison in the given Pixel Layer.

Table 5. Timeout error rate in a given Layer per Module, scaled w.r.t Layer2 Module rate.

Pixel Geometry Layer\Disks	Timeouts rate in all the three Phases	Total number of Modules	Timeouts rate in all the three Phases per Module	scaling w.r.t Layer2 Module
BLayer	0.24 ± 0.0166	286	0.0008	8.1
Layer1	0.09 ± 0.0096	494	0.0002	1.8
Layer2	0.07 ± 0.0086	676	0.0001	1.0
Disks	0.04 ± 0.0062	288	0.0001	1.3

Table 5 shows that for every one Timeout error in the Layer2 Module, there were eight Timeout errors in the BLayer Module, approximately two Timeout errors in the Layer1 Module and one Timeout error in the Disk Module.

3.2.3. ROD Busy errors study:

Similar to the previous Timeout Study, the Busy rate is the ratio of the total number of Busy errors in the given Phase of the run and the total run time of that Phase. Table 6 shows the summary of Busy rates in the given Pixel Layer in all of the three Phases of the run. The average Busy error rate in the BLayer for Phase1 runs was 0.50; i.e., approximately one Busy error in every two hours of data taking in the BLayer Modules. Whereas, in Phase2 and Phase3 runs were 1.6 hours and 1 hour of data taking respectively, clearly indicating the increase in the Busy error rate from Phase1 to Phase3. This increase in Busy rate was due to the increase of Busy errors contribution from known problematic Modules (Modules connected to the Rods: ROD_B1_S12, ROD_B1_S18, ROD_B1_S9 and ROD_B3_S8) in BLayer [2]. There was on average three Busies in every run in Pixel BLayer Modules in Phase1 and Phase2 runs and on an average of five Busies per run in Phase3 runs.

Table 6. Total Busies in a given Layer in all the three Phases.

Pixel	Timeouts in Phase1 runs (61)			Timeouts in Phase2 runs (75)			Timeouts in Phase3 runs (42)			Total Runs (178)		
Layers /Disks	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$
BLayer	191	0.50	3.13	275	0.61	3.67	220	0.98	5.24	686	0.65	3.85
Layer1	92	0.24	1.51	128	0.28	1.71	49	0.22	1.17	269	0.25	1.51
Layer2	76	0.20	1.25	97	0.21	1.29	40	0.18	0.95	213	0.20	1.20
Disks	40	0.10	0.66	52	0.11	0.69	27	0.12	0.64	119	0.11	0.67

Figure 11. Rod Busy in Pixel Layers and All Disks in all the three Phases. Source: [2]

Figure 11 shows the percentage of total Busy errors in all the three Phases occurred in Pixel Layers. A total of 1287 Busies occurred in the three Phases, among them, 686 Busies (53.3% of total Busies) were in BLayer Modules and 269 Busies (20.9% of total Busies) in Layer1 Modules.

Table 7 shows the rate after normalization with respect to Module number per Layer. For every one Busy error in Layer2 Module there were eight Busies in BLayer Module, approximately two Busies in Layer1 Module and one Busy in Disks Modules.

Table 7. Busy rate in a given Pixel Layer per Module scaled w.r.t Layer2 Module rate.

Pixel Geometry Layer\Disks	Busy rate in all the three Phases	Total number of Modules	Busy rate in all the three Phases per Module	scaling w.r.t Layer2 Module
BLayer	0.65 ± 0.0318	286	0.0023	7.7
Layer1	0.25 ± 0.0277	494	0.0005	1.7
Layer2	0.20 ± 0.0151	676	0.0003	1.0
Disks	0.11 ± 0.0109	288	0.0004	1.3

3.2.4. Results from Synchronization study:

The Synchronization study includes the Module level synchronizations errors and Rod level synchronization errors.

3.2.4.1. Module level Synchronization errors study:

Similar to previous error analyses, Module Synchronization error rate analysis was studied. The average ModSync error rate in BLayer for Phase2 runs was 4.48; i.e., approximately 4.5 ModSyncs in every one hour of data taking in BLayer Modules. Whereas, in Phase3 runs ModSync rate was 4.88 ModSync errors per hour of data taking. There were on average of 27 ModSyncs in every run in Pixel BLayer Modules in Phase2 and on average of 26 ModSyncs per run in Phase3 runs.

Table 8. Total ModSync in a given Pixel Layer in the Phase2 and Phase3 runs.

Pixel	Timeouts in Phase2 runs (75)			Timeouts in Phase3 runs (42)			Total Runs (117)		
Layers /Disks	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$
BLayer	2032	4.48	27.09	1093	4.88	26.02	3125	4.62	26.71
Layer1	1008	2.22	13.44	406	1.81	9.67	1414	2.09	12.08
Layer2	575	1.27	7.67	318	1.42	7.57	893	1.32	7.63
Disks	609	1.34	8.12	344	1.54	8.19	953	1.41	8.14

Figure 12. ModSync errors in Pixel Layers and All Disks in Phase2 runs and Phase3 runs. Source: [2]

As shown in Figure 12, a total of 6385 ModSyncs occurred in 117 runs; among them 3125 ModSyncs (48.9% of total ModSyncs) were in BLayer Modules as we expected to be the case, since BLayer modules are closer to the bunch crossing point, the probability of Single Event upset occurring is greater. Next ModSync error rate dominant

was in the Layer1 Modules in which 1414 ModSyncs (22.1% of total ModSyncs) occurred in total Phase2 and Phase3 runs.

Table 9 shows the ModSync rate after normalizing, for the respective Layer Module number. For every one ModSync action in Layer2 Module there were 8 ModSyncs in BLayer Module, approximately two ModSyncs in Layer1 Module and two ModSyncs in All End cap Disks Modules.

Table 9. ModSync rate in a given Pixel Layer per Module scaled w.r.t Layer2 Module rate.

Pixel Geometry Layer\Disks	ModSync rate in Phase2 and Phase3 runs	Total number of Modules	ModSync rate in Phase2 and Phase3 runs per Module	scaling w.r.t Layer2 Module
BLayer	4.62 ± 0.196	286	0.016	8.3
Layer1	2.09 ± 0.098	494	0.004	2.2
Layer2	1.32 ± 0.067	676	0.002	1.0
Disks	1.41 ± 0.071	288	0.005	2.5

3.2.4.2. Rod level Synchronization errors study

A similar study is done for the RodSync error rate. The average RodSync rate in BLayer for Phase3 runs was 1.64; i.e., approximately 2 RodSyncs in every one hour of data taking in BLayer Rods, and approximately 18.42 RodSyncs in every one hour of data taking in the Layer2 Rods. The high rate of RodSync in Layer2 Rods may be due to known bandwidth problems in the Layer2 Rods. There was on average 98 RodSyncs in every run in Pixel Layer2 Rods in Phase3 and on an average 8 RodSyncs per run in Pixel BLayer Rods in Phase3 runs.

Table 10. Total RodSync in a given Pixel Layer Rod for Phase3 runs

Pixel	Timeouts in Phase3 runs (42)		
Layers / Disks	#e	$\frac{\#e}{\sum T_n}$	$\frac{\#e}{\sum n}$
BLayer	368	1.64 ± 0.14	8.76 ± 2.96
Layer1	213	0.95 ± 0.09	5.07 ± 2.25
Layer2	4122	18.42 ± 1.26	98.14 ± 9.91
Disks	241	1.08 ± 0.10	5.74 ± 2.39

Figure 13. RodSync in Pixel Layer Rods in Phase3 runs. **Source:** [2]

Figure 13 shows the percentage of total RodSync errors in the Phase3 runs occurred in Pixel Layer. A total of 4944 RodSyncs were cured by the QuickStatus algorithm during these 42 runs; Among these 4944 RodSyncs, 4122 RodSyncs (83.4% of total RodSyncs) were in Layer2 Rods. In the Disks, almost all the RodSyncs were occurred in the Rod: ROD_D1_S17 [2]. This ROD is known for its bandwidth problem.

Table 11 shows the results after normalizing the RodSync error rate by taking the ratio of RodSync rate in a given pixel Layer Rods and the number of Modules in the respective Layer and scaling it with respect to the Disk Module. For every one RodSync action in the Disk Rod, there were 7 RodSyncs in the Layer2 Rods, and approximately two RodSyncs in the BLayer Rods.

Table 11. RodSync rate in a given Pixel Layer per Module scaled w.r.t Disks Module rate.

Pixel Geometry Layer\Disks	RodSync rate in Phase2 and Phase3 runs	Total number of Modules	RodSync rate in Phase2 and Phase3 runs per Module	Scaling w.r.t Layer2 Module
BLayer	1.64 ± 0.14	286	0.006	1.5
Layer1	0.95 ± 0.09	494	0.002	0.51
Layer2	18.42 ± 1.26	676	0.027	7.3
Disks	1.08 ± 0.10	288	0.004	1.0

3.2.5. Summary and discussion from the above errors study:

In general BLayer modules are sensitive to Timeout, Busy and ModSync errors, because the source of these errors is SEU, whereas the Layer2 Rods are sensitive to Rod level Synchronization errors. The Busy rate in BLayer is more than double the Timeout rate in all the three Phases of runs. The ModSync rate is 7.5 times higher than the Busy rate in BLayer Modules. The RodSync rate is 2.6 times higher than the Busy rate in BLayer.

CHAPTER 4

SUMMARY OF RESULTS AND CONCLUSIONS

Before the QuickStatus program was deployed to take the recovery actions on Timeout, Busy and Module Synchronization errors, at the beginning of each run a few of known problematic Modules were persistently showing Timeout or Busy states and with the run time the number of Bad (error state) modules increased as shown in black point curve in Figure 15, As a result the Good Module fraction goes down which directly affects the Pixel data taking efficiency. Figure 14 shows the Good Module Fraction for a set of data taking runs in the week before (up to run 202609) and after (after run 202609) implementing Quick Status logic.

Figure 14. Good Module Fraction after deployment of QuickStatus Timeout and Busy error recovery Logic.

Figure 15. Data-2012 Module error rate per luminosity block. **Source:** [8]

It is clearly noticeable that the QuickStatus logic recovers the problematic modules efficiently so that the Enabled module fraction is increased after run 202609, shown in Figure 14.

Figure 15 shows the average number of modules with readout errors per event per luminosity block in the Pixel BLayer for the data taken from a run before (black points) and after (blue points) the recovery procedure was introduced.

Because of single event upset a module may get stuck in a permanent error state. After the automatic recovery, the number of modules in error state has decreased significantly.

Thus we conclude that the Module auto-recovery algorithm recovered many problematic Modules a significant number of times in a given run. It will be interesting to study the above errors (SEU) rate at higher energies when the LHC restarts after a long shutdown, in 2014.

APPENDIX A. THRESHOLDS FOR TIMEOUT AND BUSY ERROR STATES

The QuickStatus is a Formatter link monitoring program tuned to take recovery actions on Module Timeout, Rod Busy, ModSync and RodSync errors. PixDspMonitorTask is a tool that monitors the Formatter status in the off - detector side for every 5 sec. QuickStatus also monitors the Formatter status on the detector at a faster rate of every 0.4 millisecond. It resets the Formatter link to a given number of times (Threshold set=3) before reconfiguring once the modules with Busy error as shown Figure 16. If the Busy still persists, the Module is temporarily taken out of data taking mode. For a Timeout error, the logic tries a maximum three recovery attempts to reconfigure the problematic module within the time interval of 5 sec. A brief description of module recovery action logic is shown in Figure 17. For Module synchronization also the tool reconfigures the problematic module.

Figure 16. QuickStaus Timeout and Busy recovery logic

Figure 17. Quick Status auto recovery logic for Timeout, Busy, ModSync and RodSync errors

Figure 18. Anomalous busies

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