Development of pixel front-end electronics using advanced deep submicron CMOS technologies

Miroslav Havránek

The content of this thesis is oriented on the R&D of microelectronic integrated circuits for processing the signal from particle sensors and partially on the sensors themselves. This work is motivated by ongoing upgrades of the ATLAS Pixel Detector at CERN laboratory and by exploration of new technologies for the future experiments in particle physics. Evolution of technologies for the fabrication of microelectronic circuits follows Moore’s laws. Transistors become smaller and electronic chips reach higher complexity. Apart from this, silicon foundries become more open to smaller customers and often provide non-standard process options. Two new directions in pixel technologies are explored in this thesis: design of pixel electronics using ultra deep submicron (65 nm) CMOS technology and Depleted Monolithic Active Pixel Sensors (DMAPS). An independent project concerning the measurement of pixel capacitance with a dedicated measurement chip is a part of this thesis. Pixel capacitance is one of the key parameters for design of the pixel front-end electronics and thus it is closely related to the content of the thesis. The theoretical background, aspects of chip design, performance of chip prototypes and prospect for design of large pixel chips are comprehensively described in five chapters of the thesis.
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Miroslav Havránek
aus
Prostějov, Czech Republic
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Chapter 1

Introduction

The invention of the cloud chamber in 1911 by the Scottish physicist C. T. R. Wilson [1] opened the door to the new world - the world of elementary particles. Wilson’s cloud chamber allowed visualization of the particle tracks coming from the natural radioactivity and from the cosmic rays. The type of the particle could be easily identified by a visual analysis of the particle tracks in the real time. During this exciting time of exploring the unknown domain of the reality, many new particles like for example the muon, pion and positron have been discovered by analyzing the "pictures" recorded from the cloud chambers. C. T. R. Wilson received the Nobel Prize in Physics in 1927 for his invention.

In the early experiments (1960s) at particle accelerators, a modified version of the cloud chamber, a bubble chamber [2], has been extensively used. The bubble chamber is filled with a superheated liquid and contains a piston which allows to make a fast change of the pressure inside the chamber, thus bringing the liquid into a superheated state. As the particles traverse the superheated medium, they vaporize the liquid along their paths. These trails of bubbles were photographed and the films were analyzed manually (see Figure 1.1 (a-c)). Bubble chambers provide good spatial resolution (several µm). One of the greatest discoveries made by a bubble chamber was the discovery of the neutral currents in 1973 at the Gargamelle bubble chamber installed at CERN [3]. The inventor of the bubble chamber, D. A. Glaser, was awarded the Nobel Prize in physics in 1960.

Figure 1.1: Photographs of the particle tracks (a) were analyzed manually by human "scanners" (b). Nowadays, the films capturing the "physics data" from 60s-70s are stored in metallic cans in the CERN underground (c) [4].

The path of evolution of the tracking detectors was further oriented towards gaseous detectors like for example spark chambers which allowed triggered operation or Multi Wire Proportional Chambers (MWPC) surpassing the previous generations of the detectors by high detection rates and electronic read-out. History of particle detectors is rich and well beyond the scope of this overview. More com-
Chapter 1 Introduction

A comprehensive overview of historical development of the particle detectors is shown for example in [5].

Nowadays, much more complicated experiments are undertaken in the field of particle physics. The experiments are extremely complex, particle collision rate counts in billions collisions per second and the patterns of the particle tracks are so complicated that even the best human “scanner” would never figure out what happened during the particle collisions (see Figure 1.2 (a-c)). Large experiments in contemporary high energy physics contain many sub-detectors with an electronic readout, automatically digitizing the particle collision events and storing the data with the rates of gigabytes per second for further analysis. This process is fully computerized.

Figure 1.2: Large particle experiments like the ATLAS experiment at CERN (a) are built to study the physical processes occurring in the microscopic scales. Complex patterns of the particle tracks (b) are analyzed by computers and the data are stored on magnetic tapes in data storage centers (c) [6], [7].

This thesis is dedicated to the development of pixel detectors, which play a role of tracking and vertexing devices in the modern experiments in High Energy Physics (HEP). The core of the research work presented in this thesis is a design of Integrated Circuits (IC) in the advanced CMOS technologies and evaluation of their performance for applications in experiments in HEP. The IC design involves conceptual studies of the future integrated circuit and translation of the concept to the electrical schematic. Extensive simulations and optimizations of the schematic parameters are made before the layout - physical placement of the transistors and the metallic interconnection can be made. Integrated circuits are fabricated in silicon foundries located only in several places in the world.

Design of several integrated circuits of pixel related electronics, research results and the necessary theoretical background are presented in the following five chapters of this thesis and summarized in the last chapter.

The second chapter (the first chapter is this introduction) gives a theoretical background about pixel detectors with the emphasis on the analog parameters of the pixel front-end electronics. The third chapter discusses the influence of the pixel capacitance on the noise performance of the pixel detector. The main part of this chapter is dedicated to the design of a pixel capacitance measurement chip PixCap and results obtained with this chip. The fourth chapter introduces new technologies in pixel detectors and prepares the ground for the next two chapters. The fifth chapter describes author’s work on a design of the pixel front-end electronics in a 65 nm CMOS technology and discusses the lessons learned with this technology during the design and testing phase of the chip. The sixth chapter is devoted to design and measurements of a new generation of monolithic pixel sensor chip. The thesis finalizes with conclusions.
Chapter 2

Pixel detectors for experimental high energy physics

2.1 Role of pixel detectors in high energy physics

Experiments in High Energy Physics (HEP) allow to study the composition of matter at the smallest possible scales and examine the laws governing the interactions between the elementary particles. In order to approach distances of the order of $10^{-19}$ m, particles are collided at TeV energy scales. Not only energy but also luminosity (a quantity related to the particle collision rate) is an important quantity, particularly in case of studying rare physical processes occurring with a small probability.

The energy frontier particle collider is the Large Hadron Collider (LHC) (see Figure 2.1) [8] at CERN particle laboratory near Geneva in Switzerland. LHC was designed to collide protons at center of mass energy of 14 TeV and luminosity of $10^{34}$ cm$^{-2}$ s$^{-1}$. Protons are accelerated in bunches of $10^{11}$ protons. These bunches collide at the collision points every 25 ns, producing about one billion proton-proton collisions every second. More details about the LHC can be found in [8].

![Overall view of the LHC experiments.](image)

Figure 2.1: The Large Hadron Collider has four large experiments: ALICE, ATLAS, CMS and LHCb [9].
Chapter 2  Pixel detectors for experimental high energy physics

Four large experiments are installed at the collision points of LHC: two general purpose experiments ATLAS [9] and CMS [10], an experiment dedicated to studies of heavy ion collisions - ALICE [11], and an experiment optimized for studying the b-physics - LHCb [12]. These experiments measure parameters of secondary particles produced in the collisions of the high energetic primary particles. In order to precisely measure trajectories and origins (vertices) of these secondary particles, the tracking detectors are situated very close to the collision point. Tracking and vertexing detectors are finely segmented silicon pixel or strip detector systems with short recovery time and high data throughput. All large experiments (except ALICE, which uses Time Projection Chamber) use silicon tracking systems. Technological progress in the past 20 years allowed design of silicon detectors with the size of sensitive cells of the order of tens of microns, which outperform the older generation of gas detectors in terms of speed and spatial resolution.

Currently, two large pixel detectors operate in the experiments ATLAS [6] and CMS [13]. In spite of operation in a hostile radiation environment, the pixel detectors provide data allowing the reconstruction of events with multiple vertices (see Figure 2.2) with unprecedented precision. The technology of pixel detectors significantly improved the precision measurements in particle physics and finally played a crucial role in the discovery of the Higgs boson at these experiments in 2012 [14], [15].

![Example of a candidate event of Z boson decaying into $\mu^+\mu^-$ recorded by the ATLAS experiment [16]. This event contains 25 reconstructed vertices.](image)

2.2 Tracking systems

The tracking system (tracker) is an essential component of a large HEP experiment. The tracker performs a precise measurement of particle trajectories. Electrically charged particles are detected in sensitive layers of the tracker. Throughout this thesis we will often refer to the coordinates of the coordinate system in which the tracker is placed. Definition of the coordinates $x, y, z, \phi, \theta$ and $\eta$ is identical with the ATLAS experiment and can be found in [6].

The sensitive layers of a tracker are usually arranged as coaxial (with respect to $z$ axis) barrel layers and several end-cap disks to provide a broad angular coverage. Trackers operate in a strong magnetic oriented along $z$ axis. The magnetic field curves the particle trajectories proportionally to their momentum as shown in Figure 2.3 (a). By measuring the curvature of the trajectory, the momentum of the particle is determined.
In case of a tracker consisting of three sensitive tracking layers placed inside a solenoidal magnetic field, we can express the transverse momentum $p_T$ of the particle in terms of two geometrical quantities $L$ and $s$ (sagitta) as described in Figure 2.3 (b) and the strength of the magnetic field along $z$ axis $B_z$ (more detailed derivation can be found in [17]):

$$p_T = \frac{0.3B_zL^2}{8s} \quad (2.1)$$

Momentum resolution is then given by formula:

$$\frac{\sigma(p_T)}{p_T} = \sqrt{\frac{3}{2}} \sigma_x \frac{8p_T}{0.3B_zL^2} \quad (2.2)$$

Momentum resolution improves quadratically with the radius of the tracker and linearly with the magnetic field and degrades with increasing transverse momentum and uncertainty of the spacepoint measurement $\sigma_x$ of the sensitive elements. The spacepoint resolution of the tracking layers is directly related to the geometry of the sensitive elements and cluster size. In order to find the optimum parameters of a tracker providing the best momentum resolution, additional quantities must be taken into account, for example the granularity of the sensitive layers, the inserted material causing multiple scattering and the financial budget.

![Figure 2.3](image)

**Figure 2.3:** (a): Trajectories of the charged particles are curved due to the magnetic field. By measuring the curvature radius of the trajectory, transversal momentum of the particle can be determined. (b): Transversal momentum is often expressed in terms of sagitta ($s$) and distance between spacepoints ($L$).

Although a large radius tracker is useful for the momentum measurement, some experimental methods require the determination of a decay point (vertex) of short lived particles as for example B mesons, D mesons or $\Lambda$ baryons which fly only a few $\mu$m before they decay. The position of the vertex is measured by a vertex detector. The vertex detector contains finely segmented pixellated layers closely surrounding the collision point, thus allowing a precise measurement of the vertex position and the impact parameters of the tracks (see Figure 2.4).
Chapter 2 Pixel detectors for experimental high energy physics

Figure 2.4: Short lived particles travel just a few tens of µm and decay before they reach the detector. In this case a displaced (secondary) vertex is observed in the detector. The tracks, originating at the secondary vertex, are described by transversal ($d_0$) and longitudinal ($z_0$) impact parameters.

The vertex resolution can be derived from a simple model described in [18]. If we assume a two layer vertex detector with a geometry described in Figure 2.5 having the spatial resolution $\sigma_1$ in layer 1 and $\sigma_2$ in layer 2, the resolution of the vertex position is a quadratic sum of terms arising from spacepoint uncertainties $\sigma_1$ and $\sigma_2$ as follows:

$$\sigma_{\text{VX}} = \sqrt{\sigma_{\text{VX1}}^2 + \sigma_{\text{VX2}}^2}$$  \hspace{1cm} (2.3)

where $\sigma_{\text{VX1}}$ and $\sigma_{\text{VX2}}$ are functions of the vertex detector geometry and the spatial resolution of the detector elements:

$$\sigma_{\text{VX1}} = \frac{R_2}{R_2 - R_1} \sigma_1 \quad \sigma_{\text{VX2}} = \frac{R_1}{R_2 - R_1} \sigma_2$$  \hspace{1cm} (2.4)

The quantities $R_0$ and $R_1$ and $R_2$ are radii of the beam pipe and the sensitive layers. The particles passing the beam pipe are scattered and thus deflected by an angle $\theta$ with uncertainty $\sigma_\theta$. Correction for multiple scattering enters the formula for vertex resolution in the following way:

$$\sigma_1^2 \rightarrow \sigma_1^2 + (R_1 - R_0)^2 \sigma_\theta^2$$  \hspace{1cm} (2.5)

$$\sigma_2^2 \rightarrow \sigma_1^2 + (R_2 - R_0)^2 \sigma_\theta^2$$  \hspace{1cm} (2.6)

The multiple scattering terms entering $\sigma_1$ and $\sigma_2$ are correlated. Assuming 100% correlation, we obtain following formula for the vertex resolution:

$$\sigma_{\text{VX}} = \frac{\sigma_1^2 R_2^2}{(R_2 - R_1)^2} + \frac{\sigma_2^2}{(R_2 - R_1)^2} + \sigma_\theta^2 (R_2(R_1 - R_0) + R_1(R_2 - R_0))^2$$  \hspace{1cm} (2.7)

Multiple scattering occurs also in the tracking layers and the model becomes more complicated. An alternative way to determine the vertex resolution is by performing a Monte Carlo simulation.
2.3 Hybrid pixel detectors

Using this simplistic model we can see that a good vertex resolution will be achieved if the distance between layer 1 and layer 2 is large, layer 1 is as close to the interaction point as possible, the beam pipe is as thin as possible and the spacepoint resolution of the sensitive layers is as high as possible.

![Geometrical model of a vertex detector](image1)

Figure 2.5: Geometrical model of a vertex detector for determination of the vertex resolution.

2.3 Hybrid pixel detectors

Hybrid pixel detectors are widely used in HEP for tracking and vertexing. Vertex detectors using this technology have been successfully implemented in experiments at the LHC: ATLAS [19], CMS [13] and ALICE [20]. Hybrid pixel detectors are distinguished by their excellent spatial resolution (fine segmentation), low noise, radiation hardness, fast read-out and small inserted mass in the detector.

A hybrid pixel detector is a composition of sensor and read-out chip interconnected by a suitable technology (see Figure 2.6). This approach allows an independent development of these components and more freedom in design and fabrication. On the other hand, the interconnection process represents a significant portion of a financial budget for the detector production. In the following sub-sections we will describe sensor and front-end electronics in more detail.

![A hybrid pixel detector consists of a sensor and a front-end electronic chip interconnected by the bump and flip-chip technology.](image2)
2.3.1 Pixel sensor

Pixel sensors for applications in HEP are predominantly made of silicon. Silicon is a favorable material due to its relatively small band-gap of 1.1 eV with respect to the ionisation energy of the older generation of gaseous detectors (typically more than 10 eV), and therefore, silicon sensors provide a relatively large signal. From the technology point of view, silicon is readily available and sensor fabrication process is compatible with the processes for fabrication of microelectronics.

HEP applications typically require detection of highly energetic particles passing the sensors without loosing a significant fraction of their initial kinetic energy. The silicon sensor is sensitive to electrically charged particles as for example electrons, muons, pions, kaons and others. The dominant physical process of interaction of these particles with the sensor is ionisation accompanied by creation of electron-hole (e-h) pairs in the sensor. The energy needed for the creation of a single e-h pair in silicon is on average 3.65 eV.

The mean energy, deposited in the sensor by a heavy relativistic charged particle, is described by Bethe-Bloch formula \[21\]:

\[
-\left(\frac{dE}{dx}\right) = K\frac{\varepsilon^2 Z}{A}\beta^2 \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{\text{max}}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right]
\]  

(2.8)

Ionization energy loss of a charged particle passing the matter depends on parameters of the incident particle (mass, velocity, electric charge) and on the properties of the material. Meaning of the variables used in the Bethe Bloch formula is explained in Table 2.1. \(T_{\text{max}}\) is maximum kinetic energy transfer of the incident particle to the electron during a single collision. The value of \(T_{\text{max}}\) arises from the laws of conservation of energy and momentum and is described here:

\[
T_{\text{max}} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e / M + (m_e / M)^2}
\]  

(2.9)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Units</th>
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<tr>
<td>(K)</td>
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<td>(0.307\ 075 ~\text{MeV \cdot cm}^{-2})</td>
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<tr>
<td>(N_A)</td>
<td>Avogadro’s number</td>
<td>(6.022\ 141\ 29(27)\times 10^{23}\ \text{mol}^{-1})</td>
</tr>
<tr>
<td>(r_e^e)</td>
<td>electron radius (electron radius)</td>
<td>(2.817\ 940\ 3267(27)\ \text{fm})</td>
</tr>
<tr>
<td>(e)</td>
<td>electron charge (abs. value)</td>
<td>(1.602 \times 10^{-19}\ \text{C})</td>
</tr>
<tr>
<td>(\varepsilon_0)</td>
<td>permittivity of vacuum</td>
<td>(8.85 \times 10^{-12}\ \text{F})</td>
</tr>
<tr>
<td>(m_e c^2)</td>
<td>rest energy of electron</td>
<td>(0.5109958918\ (44)\ \text{MeV})</td>
</tr>
<tr>
<td>(M)</td>
<td>mass of the incident particle</td>
<td>(\text{MeV})</td>
</tr>
<tr>
<td>(z)</td>
<td>charge number of incident particle</td>
<td></td>
</tr>
<tr>
<td>(Z)</td>
<td>atomic number of absorber</td>
<td></td>
</tr>
<tr>
<td>(A)</td>
<td>atomic mass number of absorber</td>
<td>(\text{g} \cdot \text{mol}^{-1})</td>
</tr>
<tr>
<td>(I)</td>
<td>mean excitation energy</td>
<td>(\text{eV})</td>
</tr>
<tr>
<td>(\delta(\beta\gamma))</td>
<td>density effect correction to ionization energy loss</td>
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</table>

Table 2.1: Constants and variables used in Bethe-Bloch formula [21].
2.3 Hybrid pixel detectors

As shown in Figure 2.7, the Bethe Bloch formula describes the ionisation energy loss of muons in a broad range of energies. Similar characteristic can be computed for other particle types and energy absorbing materials. The energy, deposited by the process of ionisation is a subject of large fluctuations with a characteristic long tail towards high energy, described by the Landau distribution.

Three conditions must be satisfied in order a piece of silicon can be used as a particle sensor:

1. silicon must be free of impurities which can eventually become charge generation or recombination centers
2. the bulk of the sensor must be free of charge carriers (must be either depleted or intrinsically free (diamond))
3. a drift field must be present in the sensor

The first condition is met by using high resistivity (several k\(\Omega\)-cm) silicon often doped with oxygen atoms to increase radiation hardness. The second and third conditions are met in an array of PN junctions (diodes) technologically processed on the high resistivity silicon and biased with high voltage oriented in the reverse direction of the PN junctions.

A PN junction forms at the p-n boundary in the semiconductor material separating the two regions of different types of conductivity: p-type (positive) conductivity is accomplished by holes originating from a non-saturated atomic bonds of acceptor atoms (B, Al); n-type (negative) conductivity is accomplished by electrons due to doping by donor atoms (P, As). A schematic cross section of a PN junction is shown in Figure 2.8. In the vicinity of the PN junction a depletion region forms due to diffusion of holes from the p-doped region into the n-doped region and diffusion of electrons from n into p.
Chapter 2 Pixel detectors for experimental high energy physics

Figure 2.8: Cross section of a PN junction. Majority charge carriers diffuse across the PN junction and recombine on the other side of the junction and thus a depletion region around the PN junction is formed.

Diffusion current densities $j$ of electrons and holes are proportional to the gradient of the dopant concentration $n$:

$$j_n = -D_n \nabla n_n = \frac{kT}{e} \mu_n \nabla n_n$$  \hspace{1cm} (2.10)$$

$$j_p = D_p \nabla n_p = \frac{kT}{e} \mu_p \nabla n_p$$  \hspace{1cm} (2.11)

where $D$ is the diffusion constant, $k$ the Boltzmann constant, $T$ is an absolute temperature and $\mu$ stands for the mobility of the charge carriers. The charge carriers which already crossed the PN junction recombine and are no-longer free. These trapped charges build up an electric field across the PN junction and create a potential wall between p and n regions. The shape of the electric field and the potential around the PN junction can be obtained by solving the Poisson equation. The electric potential $\phi$ and the electric field $E$ across the PN junction are illustrated in Figure 2.8.

The width of the depletion region $W$ depends on the concentration of charge carriers and also on the bias voltage ($V_{bias}$) of the sensor according to the formula:

$$W = \sqrt{\frac{2\epsilon_0 \epsilon_r}{e} \left( \frac{1}{n_n} + \frac{1}{n_p} \right) (V_{bias} + V_{bi})}$$  \hspace{1cm} (2.12)$$

$\epsilon_0$ is the vacuum permittivity and $\epsilon_r$ is the relative permittivity of silicon. $V_{bi}$ is the built-in voltage which is present across the PN junction due to the diffusion of the charge carriers. In the real sensor
the concentration of the dopants is not equal on both sides of the PN junction. The bulk of the sensor is usually much less doped than the biasing electrodes and collecting electrodes. Bias voltage of the sensor is of the order of 100 V and the build-in voltage about 0.5 V. Hence equation 2.12 can be simplified:

\[
W = \sqrt{\frac{2\varepsilon_0\varepsilon_S}{e} \frac{1}{n_{bulk}} V_{bias}}
\] (2.13)

In this case, the depletion region does not grow to the same depth \( d \) on both sides of the PN junction, but the charge from the highly doped region diffuses further into the low doped region as described by the following formula:

\[
n_n \cdot d_n = n_p \cdot d_p
\] (2.14)

\( d_n \) and \( d_p \) denote the depth of the depleted layer on each side of the PN junction. The depletion region broadens with increasing reverse voltage across the PN junction. After reaching a certain bias voltage, the depletion region extends across the entire sensor bulk and can not grow further. At this point we say that the sensor is fully depleted. Using (2.13), the voltage to achieve full depletion of the sensor is proportional to the concentration of the impurities in the silicon bulk and is quadratically proportional to the sensor thickness:

\[
V_{fullDep} = e \cdot n_{bulk} \cdot d^2
\] (2.15)

Satisfying these the conditions (silicon purity, absence of free charge carriers and presence of electric drift field) the charge, generated by the traversing charged particle, moves under the electric drift field and is collected at the collection electrodes of the sensor. More theoretical details about silicon sensors can be found in [22], [23].

An example of silicon particle sensor used in the ATLAS pixel detector is shown in Figure 2.9. Information about ATLAS pixel sensors are taken from [19]. The pixel sensor was fabricated on the oxygenated n-type FZ (Float Zone) silicon substrate with thickness of 256 \( \mu m \). The pixel size is defined by the pattern of charge collecting \( n^+ \) regions on the front-side of the sensor. This pixel sensor type is \( n^+ \) in \( n \). Pixel dimensions are 400\( \times \)50 \( \mu m \). The \( n^+ \) regions are separated by \( p \)-type regions (p-spray) preventing from ohmic connection between \( n^+ \) regions and thus from radiation induced currents between pixels. Back-side of the sensor contains a \( p^+ \) region forming a PN junction. This region is biased by negative sufficiently high voltage to achieve full depletion. The depletion region of the sensor grows (before irradiation) from the back side towards the front-side. The edge of the sensor often contains a significant damage of the crystal lattice and therefore it is conductive. High voltage from the back side of the sensor can therefore easily appear at the edge of the front side thus building up large a electric field, which can lead to an excessive leakage current or break down of the sensor. The back side of the sensor contains several guard-rings which smoothly adjust the potential from the high voltage \( p^+ \) region down to the ground potential of the sensor front-side.

Another class of silicon sensors are 3D sensors [24]. Unlike the planar sensors, the charge collecting electrodes in 3D sensors penetrate the entire sensor bulk. A schematic cross section of a 3D sensor is shown in Figure 2.10 (a, b). This sensor topology has several advantages with respect to the planar sensor. The biasing and charge collecting electrodes are closely spaced and therefore a lower bias voltage is needed to achieve full depletion (see 2.15). A typical bias voltage of the 3D sensor is only about 20 V and after irradiation no more than 200 V, while for planar sensors it is typically 100 V before
irradiation and 600 V after absorbing a large radiation dose. After charge generation, the signal travels smaller distance to the electrodes (see Figure 2.10) and therefore it has smaller probability to be trapped by radiation induced bulk damage. 3D sensors are therefore potentially radiation harder than planar sensors. Another benefit comes from the small distance between the sensitive area of the sensor and its edge. This is achieved by an active edge implant. A disadvantage of vertically arranged collecting electrodes is large pixel capacitance and large insensitive volume of the sensor due to the charge collecting and biasing electrodes. The fabrication process of 3D sensors is more complicated than of planar sensors because it consists of many successive steps involving Deep Reactive Ion Etching (DRIE). The number of companies able to produce 3D sensors is therefore limited.
2.3 Hybrid pixel detectors

Except silicon, another interesting material for producing sensors for HEP experiments is diamond. Due to the large band-gap (5.5 eV), diamond is a nearly perfect insulator and diamond crystal can therefore work as a sensor without any further doping. To extract the signal charge, only the pattern of metallic electrodes is needed to generate the drift field. The energy needed to create an electron-hole pair is 13.1 eV on average. Therefore, diamond sensor produces smaller signal with respect to the silicon sensor of the same thickness. Stronger crystal lattice of the diamond sensor predetermines this material for fabrication of radiation hard sensors. Energy needed to release a carbon atom from diamond lattice is 43 eV, while in the case of silicon it is only 25 eV. Application potential of diamond sensors is in the fields requiring a large radiation tolerance. A diamond sensor is not just an “academic option”, but is already used for example in the Beam Condition Monitor (BCM) [26] and Diamond Beam Monitor (DBM) [27] in the ATLAS experiment.

2.3.2 Front-end electronics

As we have seen in the previous subsection, silicon sensors provide a typical signal in the range of tens of thousands of electrons within the collection time of a few nanoseconds. Front-end (FE) electronics processes the signal from the sensor. Signal processing starts with the conversion of the signal charge into voltage which is performed by a charge sensitive amplifier (CSA). This voltage is discriminated and digitized. The resulting data are then coded into a comprehensive data format so that information about pixel address, time and amplitude can be disentangled from the data pattern. Then data are transmitted out of the detector.

FE electronics together with the sensor itself define properties of the entire pixel detector as for example: signal to noise ratio, maximum allowable hit-rate, radiation hardness and power consumption. Special requirements for HEP applications do not allow to use commercially available integrated circuits for signal processing and therefore FE electronics is usually implemented by Application Specific Integrated Circuits - ASICs. The design of an ASIC allows to maximally optimize the performance of the circuitry to the particular application. A general scheme of the FE integrated circuit (FE chip) of a hybrid pixel detector is illustrated in Figure 2.11. The core of the chip contains in-pixel FE electronics which is usually identical for every pixel and replicated all over the pixel matrix. The in-pixel electronics contains CSA, shaper, discriminator, digital logic and sometimes also DACs for local tuning of pixel parameters. Circuits responsible for fast data transmission - LVDS drivers, global DACs, clock signal generator (PLL), voltage regulators and digital coders (Hamming code to increase bit error immunity) stand at the chip periphery. The following four sub-sections are devoted to the description of CSA, shaper, discriminator and digital logic.

2.3.3 Charge sensitive amplifier

Charge Sensitive Amplifier (CSA) is an electronic circuit converting the electric charge $Q$ to the voltage $V_{out}$. The core of the CSA is a voltage amplifier (core amplifier) providing high open loop gain $a$. The voltage amplifier has a capacitive feedback $C_f$. In the ideal case, the CSA behaves as an integrator with a closed loop gain (the word gain in the rest of the thesis means always closed loop gain unless otherwise stated) $g$ inversely proportional to the feedback capacitance. The output voltage is related to the input charge as follows:

$$V_{out} = \frac{Q}{C_f}; \quad g_{ideal} = \frac{1}{C_f} \quad (2.16)$$
In the real life, the core amplifier has a finite open loop gain (several hundreds), the capacitance of the sensor \( C_d \) can be several hundreds of fF. Taking these effects into account, the formula for gain of the CSA changes to:

\[
g = \left( \frac{1}{C_f + \frac{C_f + C_d}{a}} \right) \cdot \left( 1 + \frac{1}{a} + \frac{C_d}{C_f a} \right)
\]  

(2.17)

Assuming realistic values of the sensor capacitance of 250 fF, open loop gain of 400 and feedback capacitance of 5 fF, the ideal gain is reduced by a factor of 0.89. Therefore, low detector capacitance and high open loop gain of the core amplifier is desirable.

The core amplifier can be implemented in several ways. The most common amplifiers are described in Figure 2.12 (a-c). The first option is a common source amplifier (Figure 2.12 (a)). An advantage of this amplifier is its simplicity and the fact that the output potential is similar to the input potential at the transistor M1. Therefore, DC feedback can be easily applied. The gain of this amplifier is equal to:

\[
g = g_m \cdot (R_{o1} || R_{o2})
\]  

(2.18)

\( R_{o1} || R_{o2} \) is a parallel combination of output resistances of transistor M1 and M2 and \( g_m \) is the transconductance of the transistor M1. Typically in deep submicron CMOS technology the output resistances of M1 and M2 are in the range of several M\( \Omega \) and transconductance of the input transistor is in the order of 10 \( \mu \)S. The open loop gain of the common source amplifier rarely exceeds 100 which is the main disadvantage of this architecture. The open loop gain can be enhanced by cascoding the input transistor. This amplifier is called the cascode amplifier and is shown in Figure 2.12 (b).

Cascoding of the input transistor increases the output resistance of the amplifier and therefore increases its gain. If we neglect the body effect of the transistor M2 and assume that \( R_{o1} \) and \( R_{o2} \) << \( R_{o3} \):

\[
g = R_{o1} g_m (1 + g_m R_{o2}) \approx g_m g_m R_{o1} R_{o2}
\]

The additional transistor M2 disables large voltage changes at the drain of the transistor M1 and thus
2.3 Hybrid pixel detectors

Figure 2.12: Typical implementations of the core amplifier of the CSA: (a) common source stage, (b) telescopic cascode, (c) folded cascode.

effectively reduces the Miller effect. The cascode amplifier works up to higher frequencies compared to the common source amplifier. On the other hand, the large output resistance only allows loading the amplifier with a high resistance load. The fact that all transistors must operate in saturation limits the maximum output voltage swing of the cascode amplifier.

The input transistor of the amplifier can be also cascoded by a transistor of a different type. In this case we talk about a folded cascode which is shown in Figure 2.12 (c). An advantage of the folded cascode is that a quiescent DC voltage at the input is similar to that at the output. Therefore, this amplifier is more suitable for closing a DC feedback loop. However, folded cascode requires a higher bias current with respect to the telescopic cascode of a similar performance and therefore this amplifier is less suitable for low power applications. Another option is represented by a differential amplifier. Its advantage is a higher Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR) compared to the single-ended architecture. However, the differential amplifier fills a larger silicon area, consumes more power and suffers from a higher noise than the equivalent single-ended amplifier.

Up to now, only the static parameters of the CSA have been discussed. Dynamic parameters of the CSA are crucial in pixel detectors processing large hit rates. Every CSA has a reset circuit to avoid saturation after detection of several particles. The reset can be implemented either by a resistor (resistive reset), a switch (switched reset CSA) or by a current source (continuous reset CSA) connected in the feedback loop of the CSA. These options are shown in Figure 2.13.

Resistive reset provides an exponential discharge of the CSA with a time constant:

$$\tau_f = R_f C_f$$  \hspace{1cm} (2.19)

As we have shown upper in this section, the value of the feedback capacitance ($C_f$) determines gain of the CSA and it can not be chosen arbitrarily. Its value is, depending on the signal charge, in the range from 4 fF to 20 fF. The discharge time constant of the CSA in a pixel detector is usually chosen as a compromise between speed (shorter $\tau_f$, the higher hit-rate the CSA can process) and noise (longer $\tau_f$,
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Figure 2.13: The CSA with different discharge circuits: (a) the CSA with resistive feedback discharges exponentially with time constant $\tau_f = R_f C_f$. (b) the switched feedback CSA discharges within a short reset period when the feedback switch is switched on. (c) the CSA with constant current feedback discharges linearly with time.

...the better noise performance is achieved). Typical value for $\tau_f$ is between 100 ns and 1 $\mu$s. In order to achieve this range of discharge time, the feedback resistor must be very large ($\sim 100$ M$\Omega$) which is difficult to realize in CMOS technology. A MOSFET transistor biased in the linear region can perform this task. The second option is a switched reset which is particularly suitable for applications with emphasis on speed. The amplifier with switched reset has faster risetime, no ballistic deficit (described below) and provides fast return to the baseline. The third option is using a current source as a discharge circuit. In this case, the feedback capacitor discharges linearly and the signal amplitude can therefore be measured by a Time Over Threshold method.

Two major effects influence the dynamic performance of the CSA: risetime and ballistic deficit. The risetime $\tau_r$ of the CSA describes how fast the voltage at the output of the CSA reaches its maximum value after charge collection (charge collection is assumed to be much shorter than $\tau_r$). The ballistic deficit appears in the CSA with feedback circuit implemented either with a resistor or with a current source. During the time $\tau_r$, the CSA already starts being discharged by the feedback circuit limiting the maximum achievable peak voltage of the CSA. The effect is more significant when the $\tau_r$ is of the same order as $\tau_f$ and the CSA charge collection rate becomes comparable with the discharge rate.

To investigate the dynamic performance of the CSA, a simple model has been used. The model and subsequent analysis was inspired by [28] and that document contains a more detailed description of the CSA. A simplified schematic of the CSA is shown in Figure 2.14. The core amplifier with open loop gain $a$ is followed by a unity gain buffer. The capacitor $C_d$ represents sensor capacitance, $R_f$ and $C_f$ are feedback components and $C_{out}$ is the output capacitance of the core amplifier. The $C_{out}$ capacitor has been added after the core amplifier rather than after the buffer, because the core amplifier has usually large output resistance and is more sensitive to the load impedance than the buffer. For small signals, this model can be linearized and expressed in more suitable form for the further analysis as shown in Fig-
2.3 Hybrid pixel detectors

In this model, we assume that the core amplifier is implemented with a single stage amplifier whose gain is given by a product of $g_m$ of the input transistor and output resistance of the amplifying stage $R_o$.

![Diagram of the CSA model](image)

Figure 2.14: Model of the CSA.

![Diagram of the small signal linearized model of the CSA](image)

Figure 2.15: Small signal linearized model of the CSA.

Applying the nodal analysis on the linearized model shown in Figure 2.15, we obtain the following transfer function:

$$H(p) = K \cdot \frac{(p + \text{Zero})}{(p + \text{Pole1}) \cdot (p + \text{Pole2})}$$

(2.20)

The transfer function has one zero (Zero), two poles Pole1 and Pole2 and a constant factor $K$. These parameters were computed in Wolfram Mathematica [29] using the assumptions $a \gg 1$ and $C_{out} \gg C_f$ as follows:

$$K = \frac{a \tau_f}{g_m (\frac{a C_{out} \tau_d}{g_m} + \tau_f \tau_{out})} ; \quad \text{Zero} = \frac{g_m}{C_f}$$

(2.21)

$$\text{Pole1} = \frac{g_m (\tau_d + a \tau_f + \tau_{out})}{a C_{out} \tau_d + g_m \tau_f \tau_{out}} ; \quad \text{Pole2} = \frac{a}{\tau_d + a \tau_f + \tau_{out}}$$

(2.22)

Time constants and gain are defined in a following way:

$$a = g_m \cdot R_o \quad \tau_f = R_f \cdot C_f \quad \tau_d = R_f \cdot C_d \quad \tau_{out} = R_o \cdot C_{out}$$

(2.23)
Typical values for the CSA model from Figure 2.15 are written in Table 2.2 and the corresponding frequency characteristic is shown in Figure 2.16. The poles are located at frequencies of 30 kHz and 13.6 MHz. Each pole bends the frequency characteristic downwards with the rate of 20 dB per decade, while the zero bends the frequency characteristic upward at the frequency of 1.6 GHz by 20 dB per decade.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_d$</td>
<td>150 fF</td>
</tr>
<tr>
<td>$C_f$</td>
<td>5 fF</td>
</tr>
<tr>
<td>$R_f$</td>
<td>1 GΩ</td>
</tr>
<tr>
<td>$g_m$</td>
<td>50 µS</td>
</tr>
<tr>
<td>$R_o$</td>
<td>10 MΩ</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>20 fF</td>
</tr>
</tbody>
</table>

Table 2.2: Typical parameters of the CSA designed in deep sub-micron CMOS technology.

Response of a CSA to a Dirac impulse is given by the inverse Laplace transform of the original transfer function (2.20):

$$V_{out} = K \cdot \left( \frac{Pole1 - Zero}{Pole1 - Pole2} \cdot e^{Pole1 \cdot t} + \frac{Zero - Pole2}{Pole1 - Pole2} \cdot e^{Pole2 \cdot t} \right)$$  (2.24)

$Pole1$ at the frequency of 13.6 MHz is responsible for the rising edge of the output signal of the CSA.
and Pole2 at 30 kHz determines a slow CSA discharge. The risetime of the CSA is then proportional to the inverse value of Pole1 and by keeping the most significant terms only, the risetime $\tau_r$ can be expressed in the following way:

$$
\tau_r \approx \frac{1}{\text{Pole1}} = \frac{aC_{\text{out}}\tau_d + g_m\tau_f\tau_{\text{out}}}{g_m(\tau_d + a\tau_f + \tau_{\text{out}})} \approx \frac{C_{\text{out}} \cdot C_d}{g_m \cdot C_f}
$$

(2.25)

In order to achieve fast risetime, the input transistor must have large transconductance and a large feedback capacitor while the sensor and loading capacitance of the amplifying stage of the CSA must be as small as possible. However, each of these parameters have a direct impact on noise (or rather signal to noise ratio) of the CSA and therefore must be carefully optimized. A very fast CSA is not always the best choice. The charge collection time can be as long as several ns. If the CSA risetime is shorter than the charge collection time, it will not improve the speed of the detector and in addition introduces a higher noise level. The discharge time (or return to baseline) of the CSA is given by Pole2 and is approximately equal to $\tau_f$.

In practice it is desirable that $\tau_f \gg \tau_r$. If $\tau_f$ is too close to $\tau_r$ (Pole2 approaches Pole1), the CSA starts discharging before the voltage amplitude at the output of the CSA develops due to the ballistic deficit effect and thus the gain of the CSA drops. A response of the modelled CSA to various input charges is shown in Figure 2.17 (a) and the effect of the ballistic deficit is shown in Figure 2.17 (b).

![Figure 2.17: (a): Response of the modelled CSA to various input charge amplitudes. Pole2 is set to 30 kHz and Pole1 to 13.6 MHz. The characteristic exponential discharge is apparent. (b): The Pole2 is swept close to the Pole1 while the injected charge is constant (20 ke\textit{e}). Decline of the peak voltage $V_{\text{out}}$ is observed due to the ballistic deficit.](image)

### 2.3.4 Shaper

A shaper is an electronic filter, usually a band-pass, defining the bandwidth of the signal output of the CSA. The shaper helps to suppress the low and high frequency noise component and therefore improves the signal to noise ratio of the pixel detector. The low $f_{\text{cmin}}$ and high $f_{\text{cmax}}$ frequencies of the shaper have to be chosen carefully to optimize Signal to Noise Ratio (SNR). The simplest shaper is the CR-RC filter as shown in Figure 2.18.
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Figure 2.18: A simple realization of the shaper with CR and RC elements.

The transfer function of this circuit has the form:

\[ H(p) = \frac{pC_1R_1}{(1 + pC_1R_1)(1 + pC_2R_2)} \]  

(2.26)

and an example of frequency characteristic with \( f_{\text{cmin}} = f_{\text{cmax}} = 1 \) MHz is shown in Figure 2.19.

Figure 2.19: Frequency characteristic of the CR-RC filter with \( f_{\text{cmin}} = f_{\text{cmax}} = 1 \) MHz

The first order CR-RC filter often does not provide a good band-selectivity and therefore filters of higher orders are applied - for example \( \text{CR}^n-\text{RC}^m \). Although applying a dedicated shaper in a pixel read-out chain may be beneficial to improve the SNR, it is often omitted due to various reasons. In HEP, the useful signal usually lies within a bandwidth around 1 MHz and the filter has to be designed accordingly. In the example described above, the time constant is in the range of \( \mu s \). This corresponds for example to a resistor in the range of M\( \Omega \) and a capacitor of pF range. Such resistors and capacitors are often hard to integrate in a small pixel area. In the current trend of decreasing the pixel size and power consumption, the power saving is the next parameter to be considered. In pixel FE electronics, the constant current feedback acts as a filter and by appropriate choice of the discharge time constant \( \tau_f \) and output capacitance \( C_{\text{out}} \) (see Figure 2.14), the SNR can be optimized.
2.3 Hybrid pixel detectors

2.3.5 Discriminator

The discriminator stands at the end of the analog read-out chain. The discriminator compares the voltage at the output of the shaper (or CSA) with a reference value and sets its output either to HIGH level or LOW level depending on whether the input voltage is above or below the detection threshold, thus providing digitization with a single bit resolution. If the discriminator processes a signal from the CSA with a constant current source feedback, the length of the pulse at the output of the discriminator is directly proportional to the signal charge. The length of the pulse can be used for amplitude measurement. This method is called Time Over Threshold and can be understood from Figure 2.20.

![Figure 2.20: Pulse length at the output of discriminator can be used for measurement of signal charge.](image)

Three figures of merit define the performance of the discriminator. High pixel occupancy is typical for high luminosity hadron colliders. The analog read-out chain has to provide information about a hit within a fraction of a microsecond independently of the signal amplitude. Therefore, a high speed discriminator providing a small time-walk of the pixel analog read-out chain is desirable. The second parameter is the dispersion of a voltage input offset of the discriminator across the pixel matrix. Due to fabrication process variations, an offset of the discriminator can significantly change from pixel to pixel. This effect can be compensated by an in-pixel DAC to achieve uniform threshold of all pixels in the matrix. A last, but not least requirement is a low power consumption which goes against the speed requirements. In the pixel electronics, a power of only few µW is available to power the discriminator. Alternatively, the signal can be digitized by an ADC and discriminated on data level. However, integration of a fast ADC might be challenging and may significantly increase the power budget of the pixel.
2.3.6 Digital logic

A hit of an event is usually stored locally in a pixel waiting for the read-out to be triggered. The event must be assigned with a pixel address and timestamp (bunch crossing ID). An optimal read-out architecture strongly depends upon the hit occupancy and bunch crossing scheme. For example, at the LHC the bunch crossings come with the time spacing of 25 ns. It is not possible (and also not needed) to always read-out all pixels at every bunch crossing. The discriminator in a pixel automatically provides a zero suppression and only pixels with a hit are read-out. Large particle experiments like ATLAS or CMS use sophisticated trigger systems which tells the pixel detector to only read-out data when the event is physically interesting. The trigger system needs a time of 2-3 µs (trigger latency) for the decision whether the event was interesting or not. The information about the hits must be stored in the pixels for that time before it is either read-out or lost.

Layout of a pixel matrix in a large pixel chip is usually organized in double column regions. This topology is advantageous in terms of distribution of digital signals and separation of the sensitive analog part from the digital part. The data from the pixels are transmitted on a data bus which is common for all pixels in the double column. Data from all double columns are processed by a double column logic and read-out by high speed (for example LVDS) interface.

2.3.7 Interconnection

Interconnection of the sensor and FE electronic chip requires a technology able to deal with a small pitch and high density connections. Several techniques can be used for interconnecting the sensor and the FE chip as for example bump bonding [30], gold stud [31], slid [32], etc. A widely used technology in high energy physics is bump bonding using electroplated solder bumps. More details about chip-to-sensor interconnection are written in [22] and about its capabilities in [33].

Figure 2.21: In the process of bump-bonding, the cylinders of solder bumps (a) are galvanically grown on the silicon chip. After reflow, the solder balls (b) are formed [33].

Bump-bonding is performed within several technological steps involving the deposition of an Under Bump Metallization (UBM), typically containing a thin adhesion layer (Ti/W) and a thick wettable Cu layer. On the top of the UBM the solder (PbSn) cylinders are galvanically grown as shown in Figure 2.21 (a). The solder cylinders turn into solder balls under surface tension during reflow at a
temperature of about 250 °C as shown in Figure 2.21 (b). The UBM layer is also grown on the surface of the sensor counterpart. Both parts of the detector are then combined and reflowed again. This process is called flip-chipping. During the reflow, the surface tension of the solder balls perfectly self-aligns the sensor and the FE chip and minimizes the number of imperfectly connected pixels. This interconnection method provides a mechanically stable connection. A disadvantage of this interconnection technology is its complexity and high cost.

2.4 ATLAS Pixel Detector

The pixel detector [19] is an innermost part of the ATLAS tracking system and is schematically shown in Figure 2.22. Three coaxial barrel layers with radii from 50.5 mm to 122.5 mm and three end-cap disks provide full angular coverage in the \( \phi \) direction and in \( \theta \) direction up to \( \eta \leq 2.5 \) (for definition of coordinates see [6]). The pixel size is 400 \( \mu \)m in \( z \) direction and 50 \( \mu \)m in \( \phi \) direction and provides an impact parameter resolution better than 15 \( \mu \)m in \( \phi \) direction and about 1 mm in \( z \) direction. This extraordinary resolution is particularly important for the identification of multiple primary vertices and precision measurement of displaced secondary vertices. A direct consequence of the high resolution is a large number of pixels, about 80 million (67 mil. barrel layers and 13 mil. end-cap disks). The pixel detector was designed to operate in a trigger based data taking mode. Components of the pixel detector have been designed to withstand a radiation dose of about 500 Mrad and a fluence of \( > 10^{15} \) neq/cm\(^2\). The entire detector consists of a mechanical support, power and data cables, cooling systems and pixel modules. All the mechanical components of the detector introduce an unwanted multiple scattering of the particles leaving the collision point. Therefore their mass must be as small as possible.

![Figure 2.22: A schematic view of the ATLAS pixel detector [19].](image)

The pixel detector contains in total 1744 pixel modules (1456 barrel and 288 end-cap modules). One pixel module is shown in Figure 2.23. Each module carries 16 front-end chips FE-I3 [19] bump-bonded to the pixel sensor and one MCC chip [19]. Silicon pixel sensors are type \( n^+ \) on \( n \) with a thickness of 256 \( \mu \)m.
Each front-end chip FE-I3 processes the signal from 2880 pixels of the sensor. The FE-I3 has been fabricated in 250 nm CMOS process. The read-out chain has a typical read-out architecture described in Section 2.3.2. A charge sensitive amplifier implemented with a single-ended folded cascode stands at the beginning of the read-out chain. The chip has been designed to process a negative charge signal obtained from a pixel sensor with a pixel capacitance of up to 400 fF. The amplifier is DC coupled to the sensor. The FE-I3 contains circuits for leakage current suppression operating up to a leakage current of 100 nA per pixel. The CSA has a current source feedback providing a return to the baseline time of 1 µs at the 20 keV input signal. The signal from the CSA is processed by a discriminator with adjustable threshold and supplied to the digital logic. The FE-I3 has a double column architecture beneficial for separating of analog and digital parts of the pixels and sharing a common data bus of two columns. If a hit comes, the digital logic stores a timestamp of the Leading Edge (LE) and Trailing Edge (TE) of the signal from the discriminator and sends them together with a pixel row number to the End Of Column (EoC) logic. Read-out of all 16 FE-I3s within a single pixel module is controlled by a MCC chip. The MCC collects data from FE-I3 chips and performs derandomization of the data. When the data from one event are complete, the event is built and the data are transmitted out of the MCC to the ROD system. Apart from the event building, the MCC chip provides a distribution of the timing signals into the 16 FE-I3s, as for example bunch crossing clock, trigger signal or reset, and also performs a configuration of the FE-I3 chips. Data transmission out of the module is implemented by the LVDS line providing a data rate of 40 Mbit/s. Data lines from several pixel modules are further multiplexed and transmitted outside the detector by an optical link.
2.5 ATLAS upgrade

The physics program at the Large Hadron Collider spans over many years up to about 2030. The long term operation of the LHC including the experiments requires periodic maintenance and continuous upgrades. Major upgrades of detectors are performed during long LHC Shut-Down (LS) periods. The upgrade of the ATLAS pixel detector will be conducted in three phases. During the upgrades, new technologies will be implemented in the tracking systems to enhance the tracking performance and efficiency as required by the increasing luminosity at the LHC. ATLAS pixel upgrade phases are described below. The data and time-lines presented here were taken from [34] and they might change in the future.

Phase 0 - upgrade will be performed during a long LHC shut-down in 2013-2014. Before the shut down, ATLAS has collected the integrated luminosity of 21.3 fb\(^{-1}\) and reached peak luminosity of \(7 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}\), which is 70% of the nominal luminosity of the LHC. In this phase, a new pixel layer (Insertable B-Layer - IBL) will be installed to improve tracking and vertexing performance of the pixel detector.

Phase 1 - before Phase 1 upgrade the peak luminosity reaches the nominal luminosity of the LHC of \(1 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}\) and the total recorded integrated luminosity will be about 50 fb\(^{-1}\). This upgrade is scheduled during a long LHC shut down in 2018.

Phase 2 - in 2022-2023, a long LHC shut down is planned. Before this time, the peak luminosity will reach double of the nominal luminosity of the LHC. The existing pixel detector will be at the end of its lifetime and will be completely replaced. After this upgrade, LHC will further increase the peak luminosity by factor of 5-10. The entire Inner Detector [6] (Pixel Detector, Semiconductor Tracker (SCT) and Transition Radiation Tracker) will be replaced.

2.6 Insertable B-Layer

The Insertable B-Layer (IBL) is a new innermost layer of the ATLAS pixel detector. Motivation for the IBL development is an improvement of the tracking and vertexing performance and compensation of tracking inefficiency of the existing B-Layer due to the radiation damage. The IBL is meant to extend the lifetime of the pixel detector before LHC reaches twice of its nominal peak luminosity. IBL consists of 14 staves carrying 224 pixel modules. In total, IBL has about 4 million pixels arranged in one barrel layer of a small radius of 3.3 cm (sensor radius). The IBL requires installation of a new (smaller) beam-pipe. IBL represents an inserted material budget of 1.5% \(X_0\) (\(X_0\) is the radiation length) at small \(\eta\). The IBL has been installed in ATLAS in May 2014. More detailed information about IBL can be found in the Technical Design Report [35]. The development of this new pixel layer involved development of new sensors, FE electronics, powering scheme and cooling system.

2.6.1 Sensors

Two sensor technologies have been chosen for sensor production for IBL: planar silicon sensors and 3D silicon sensors. The planar sensors cover up to 75% of the central IBL area while the remaining 25% in the high \(\eta\) region is covered by 3D silicon sensors. The 3D sensors located in the high \(\eta\) regions provide better resolution after irradiation than silicon planar sensors would at the same conditions. Pixel size of both sensor types is 250×50 \(\mu\text{m}^2\).
2.6.2 Front-end chip

A new FE chip - FE-I4 - has been developed for ATLAS IBL. Micrograph of the FE-I4 is shown in Figure 2.24. FE-I4 with an area of \(21 \times 19\) mm\(^2\) is the largest FE chip used in the high energy physics. The active area of the chip is almost 90%. FE-I4 has been fabricated using 130 nm CMOS technology and contains about 80 million transistors. FE-I4 processes signal from 26880 pixels arranged in 80 columns and 336 rows and transmits the data with a speed of 160 Mbit/s using differential LVDS data lines. Due to the complexity of FE-I4, only the key aspects of the chip will be discussed in this subsection and more detailed information can be found in design documentation [36].

![Micrograph of the FE-I4 front-end chip](image)

**Analog pixel** - simplified schematic of the analog pixel FE electronics is shown in Figure 2.25. A two stage AC coupled CSA with a current feedback has been designed to amplify the charge of negative polarity. The first stage has been implemented with a regulated telescopic cascode with an NMOS input transistor. The entire amplifier has been optimized for fast rise-time, low noise and low power.

![A schematic of the analog pixel electronics implemented in the FE-I4](image)
2.6 Insertable B-Layer

The sensor is DC coupled to the first amplifying stage and therefore a leakage current compensation circuit has been implemented in the FE-I4. The charge sensitive amplifier provides a good linearity for the ToT charge measurement with a possibility of adjusting the ToT range with a 4-bit Feedback DAC (FDAC) individually in each pixel. Signal is coded by 4-bits using ToT information. The discriminator has a local threshold adjustment DAC (TDAC) providing 5-bit resolution.

**Digital pixel** - FE-I4 follows a double column architecture (see Figure 2.26) in a similar way as its predecessor FE-I3. However, a concrete implementation and data handling is different. The increased hit rate in the close vicinity of the collision point requires a novel approach of data handling. The digital part of FE-I4 pixels is divided to digital regions. One digital region is shared by four pixels (2 × 2). The digital region contains shared memory allowing to store up to 5 events. The time of arrival of each event is registered by a counter with a time resolution of 25 ns. The data are transmitted to the double column bus only when the trigger comes (which is the main difference with respect to FE-I3.)

![Figure 2.26: A simplified schematic of the FE-I4 read-out chip [36].](image)
The trigger selects only 0.25% of all hits to be transmitted and read-out [37]. This solution greatly reduces the digital activity on the double column data bus, thus keeping the power budget of the chip within reasonable limits. More information about FE-I4 is written in [36].

Storing data locally in a pixel has been possible with use of the deep submicron technology (130 nm feature size), allowing high density integration. The pixel digital logic is shared by 2×2 pixel regions as shown in Figure 2.27. As we show in the following chapters, the distributed digital logic and advanced data processing is becoming a popular trend in the design of large pixel chips in deep submicron technologies.

Figure 2.27: Layout of 6 pixels out of 26880 pixels integrated in FE-I4 [38].
Chapter 3

Pixel capacitance and electronic noise

3.1 Noise in the charge sensitive amplifier

Noise is an unwanted component of the electrical signal having an unpredictable character in the time domain and its presence in the pixel detector can have several causes. Noise can come into the pixel electronics from outside, superimposed in the power lines (pickup noise). Another noise contribution can be obtained due to the crosstalk between the electronics in the adjacent pixels or even the crosstalk within a single pixel (typically coupling between noisy digital part and sensitive analog part of the pixel). These kinds of noise can be eliminated by a proper filtering of the power lines and by a careful design of the FE electronics.

Another noise component represents an electronic noise. The electronic noise comes from the electronic components themselves as their physical property. In the CMOS electronics, the main sources of noise (from now on, “noise” will always refer to the electronic noise, unless stated otherwise) are MOSFET transistors and resistors. The most significant noise contributor in the pixel detector is the CSA.

Depending on the physical mechanisms of noise generation, we distinguish several types of noise appearing in the CSA: thermal noise, flicker noise and shot noise. A statistical behavior of the noise amplitude and its frequency spectrum is known and therefore noise can be effectively modelled and the CSA can be optimized to achieve an optimum noise performance. More detailed information about noise in electronic circuits can be found in [39] and [40].

3.1.1 Thermal noise

Thermal noise is present in every electronic component involving a current flow. In CMOS electronics, it is limited only to transistors and resistors. Electrical current is a current of charged particles (electrons) propagating through material. The electrons often collide with atoms thermally vibrating in a crystal lattice. Electrons rapidly change velocity thermally. These effects lead to an erratic motion of the electrons causing voltage fluctuations on the terminals of the electrical component. The interaction cross-section of these electron collisions grows with temperature and therefore the noise power also grows with temperature. Frequency spectrum of the thermal noise is flat. Noise is expressed in a form of the Power Spectral Density (PSD), describing the noise power as a function of frequency. In an analysis of electrical circuits, we rather use quantities like voltage V and current I which are related to power with relations $P = R \cdot I^2$ and $P = V^2/R$. Depending on a particular noise model, noise source is often represented by a current source with noise current $I_n$ or by a voltage source with noise voltage of $V_n$. PSD is obtained either by multiplying or dividing this quantity by an appropriate resistance.
Chapter 3 Pixel capacitance and electronic noise

Thermal noise of a resistor is modelled by a voltage source connected serially to the resistor. The thermal noise voltage generated in the resistor is as follows:

\[
\overline{V_{n,th}^2} = 4 \cdot k \cdot T \cdot R \cdot df
\]  

(3.1)

\(\overline{V_{n,th}}\) is the RMS value of the noise voltage. Noise of the MOSFET transistor operating in saturation region is modelled by a current source connected between drain and source. Noise current of the MOSFET transistor is equal to:

\[
\overline{I_{n,th}^2} = 4 \cdot k \cdot T \cdot \gamma \cdot g_m \cdot df
\]  

(3.2)

The coefficient \(\gamma\) is 2/3 for long channel transistors. In case of deep submicron devices, this coefficient is larger. Since the origin of the thermal noise is given by fundamental laws of physics, it can not be reduced in any other way than decreasing the operating temperature of an electronic device.

3.1.2 Flicker noise

Flicker noise in CMOS electronics is caused by the charge carriers propagating close to the Si-SiO\(_2\) boundary in the conductive channels of the MOSFET transistors. This boundary contains a number of dangling bonds, acting like traps for the charge carriers which are randomly trapped and released again. The density of traps depends on the quality of the silicon processing and therefore the flicker noise can not be derived using fundamental laws of physics. The flicker noise of the MOSFET transistor is modelled by a voltage source connected serially to the gate as shown in Figure 3.1.

![Figure 3.1: Flicker noise is modelled by a voltage source connected serially to the transistor gate.](image)

The noise voltage due to the flicker noise is described by the following formula:

\[
\overline{V_{n,fl}^2} = \frac{K_f}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f} \cdot df
\]  

(3.3)

\(W\) and \(L\) are dimensions of the transistor (width and length), \(C_{ox}\) is the gate oxide capacitance and \(K_f\) is a constant depending on the technology. The power spectral density of the flicker noise is inversely proportional to the transistor area. Unlike the thermal noise, the power spectral density of the flicker noise decreases with frequency, which means that low frequency fluctuations have higher amplitude than high frequency fluctuations.
3.1.3 Shot noise

Shot noise originates from a discrete movement of the charge carriers across a potential barrier - for example a PN junction. As the charge carrier crosses the PN junction, the intensity of the electric field across the junction changes appropriately. Noise current due to the shot noise is directly proportional to the electrical current $I$ across the PN junction:

$$I_{n_{-sh}}^2 = 2 \cdot q \cdot I \cdot df$$  \hspace{1cm} (3.4)

The power spectrum of the shot noise is flat. In a pixel detector, shot noise originates from leakage current of the sensor and usually represents a negligible component of the total noise budget. However, the leakage current of the sensor increases as a consequence of the bulk damage caused by radiation and in extreme cases the shot noise can become a dominant noise component of the pixel detector.

3.2 Noise modelling

The most sensitive element of the CSA is the input transistor, which is a subject of thermal and flicker noise. An additional noise component is represented by the shot noise originating from the sensor. These noise mechanisms (thermal, flicker and shot) cause uncorrelated current/voltage fluctuations. The noise level of the CSA is usually expressed in terms of the Equivalent Noise Charge (ENC). The ENC is equal to the charge fluctuation at the input of an ideal (noiseless) CSA causing a noise voltage at the output which is equal to the noise voltage of a real (non-ideal) CSA. A conversion equation between the ENC and noise voltage of an ideal CSA is described by the formula:

$$ENC = \frac{C_f}{q} \cdot \overline{V_{n_{-th}}}$$  \hspace{1cm} (3.5)

$\overline{V_{n_{-th}}}$ is RMS noise voltage at the output of the CSA. The total ENC of the CSA is expressed as a quadratic sum of all noise components:

$$ENC = \sqrt{ENC_{th}^2 + ENC_{fl}^2 + ENC_{sh}^2}$$  \hspace{1cm} (3.6)

We will use the linearized model of the CSA introduced in Chapter 2 in Figure 2.15, extended by a current source $I_{n_{-th}}$ as shown in Figure 3.2 to evaluate the dependence of the thermal noise of the CSA $\overline{V_{n_{-th}}}$ on the parameters of the model.

![Figure 3.2: A linearized model of the CSA used for computation of the thermal component of noise.](image)
The transfer function of the CSA has been extracted by a nodal analysis:

\[ H_{th}(p) = \frac{V_{n,th}(p)}{I_{n,th}(p)} = K \cdot \frac{(p - Zero)}{(p - Pole1) \cdot (p - Pole2)} \]  

\( I_{n,th} \) is the thermal noise current of the input MOSFET transistor described by Equation 3.2. Poles (Pole1 and Pole2), zero (Zero) and constant factor \( K \) have been computed using Wolfram Mathematica [29] under simplifying conditions: \( C_d \gg C_f \), \( C_{out} \gg C_f \), \( a \gg 1 \), \( \tau_d \gg \tau_f \), \( \tau_d \gg \tau_{out} \), \( a \cdot \tau_f \gg \tau_d \):

\[ \text{Pole1} = -\frac{a \tau_f}{\tau_d \tau_{out}} \]  

\[ \text{Pole2} = -\frac{1}{\tau_f} \]  

\[ \text{Zero} = -\frac{1}{\tau_d} \]  

\[ K = -\frac{a}{g_m \cdot \tau_{out}} \]  

Time constants and open loop gain are defined in the following way:

\[ \tau_{out} = R_o \cdot C_{out}; \quad \tau_f = C_f \cdot R_f; \quad \tau_d = C_d \cdot R_f; \quad a = g_m \cdot R_{out} \]  

The RMS noise voltage at the output of the CSA can be obtained from Equations 3.2 and 3.7 by integrating over the entire frequency space:

\[ \overline{V_{n,th}^2} = \int_0^\infty \overline{I_{n,th}^2} \cdot |H_{th}(i \cdot \omega)|^2 d\omega \approx \frac{k \cdot T \cdot \gamma \cdot C_d}{C_f \cdot C_{out}} \]  

The ENC can be extracted in the following way:

\[ \text{ENC}_{th} = \frac{C_f}{q} \cdot \sqrt{\overline{V_{n,th}^2}} = \frac{1}{q} \cdot \sqrt{\frac{k \cdot T \cdot \gamma \cdot C_d}{C_f \cdot C_{out}}} \approx \sqrt{C_d} \]  

To optimize the noise performance of the CSA, capacitances \( C_d \), \( C_f \), \( C_{out} \) are of central importance. \( C_d \) depends on the sensor material and the pixel geometry. An over-reduction of \( C_d \) by adjusting the sensor layout may lead to a loss of charge collection efficiency of the sensor. The capacitance \( C_f \) determines the gain of the CSA. A large \( C_f \) reduces noise, but at the same time the CSA loses its gain and thus reduces the SNR as well. The capacitance \( C_{out} \) has a large impact on the dynamic behavior of the CSA (risetime and ballistic deficit) and can not be arbitrarily high as well.

### 3.3 Noise simulations

Noise performance of the CSA (or any other electronics circuit) can be simulated using the standard IC design tools. The simulation tools often use more sophisticated noise models than models described in the previous section. Parameters of these models are tuned to the particular technology. Simulations therefore represent a more precise way of determination of noise and its scaling with the values circuit parameters (pixel capacitance). Two simulation strategies exist to determine noise levels: AC noise simulation and transient noise simulation.
3.3 Noise simulations

3.3.1 AC noise simulation

An input for the AC noise simulation is a schematic of the circuit. The simulator determines a DC operating point of the circuit and linearizes the circuit around the DC operating point. Linearization of a non-linear circuit introduces an error in the simulation which grows as the circuit departs from its DC operating point.

Each individual component of the circuit is replaced by its noise model with known PSD. The noise sources are not correlated and do not influence each other. Simulation of the response of the circuit to the noise sources is performed in frequency domain.

AC noise simulation is very fast and effective way to determine noise in a broad frequency range. However, the applicability of AC noise analysis is limited to linear circuits where signal and noise can be treated separately or mixed using the superposition principle.

3.3.2 Transient noise simulation

The electronic circuits in real life are not always linear and do not always process only small signals. Transient noise simulation is a general tool for computing noise behavior of non-linear systems. It is particularly suited for the circuits dealing with random signals like for example data transmitters, receivers, converters (ADC/DAC) or PLL.

Transient noise simulation operates in the time domain. At each time step, the noise sources in the circuit generate a random noise signal. The upper limit of the studied noise frequency spectrum is given by the minimum time step. The lower frequency limit is determined by the number of the simulated time steps. Transient noise simulation requires significantly more computation power than AC noise simulation and is therefore used only in applications where the precision of AC simulation is insufficient.

3.3.3 Noise simulation of FE-I4

Noise of the CSA integrated in FE-I4 has been simulated using Cadence Virtuoso Spectre simulation tools [41]. The CSA is not completely linear and is not a time invariant system. AC simulation is not sufficient to simulate the noise performance of the CSA. Noise has been therefore simulated using transient noise analysis. Figure 3.3 (a, b) displays a response of both stages of the CSA to the signal charge of 2 ke− determined by transient noise simulation.

The simulation covered 100 µs of the proper time of the circuit with resolution of 1 ns while the PC ran the simulation for approximately two days. The noise bandwidth was from 10 kHz up to 1 GHz. There are many possible ways to determine noise out of the signal represented in the time domain. We have chosen the one, which is similar to the procedure how the noise is physically measured in FE-I4 by a threshold scan. The maximum signal amplitude from each injection has been identified in the data. Standard deviation of signal amplitude represents noise. This procedure has been repeated for several sensor capacitances $C_d$. The noise dependence on $C_d$ has been expressed in terms of ENC and is shown in Figure 3.4.
The result of the transient noise simulation indicate increase of noise with sensor capacitance. However, the simulated dependency does not absolutely agree with noise scaling $\text{ENC} \approx \sqrt{C_d}$ as predicted by theory, but is something rather linear. In Chapter 5, results of a real measurement of noise performance of the CSA as a function of $C_d$ also indicate rather linear dependence. The discrepancy between noise modeling and transient noise simulation can be caused by the fact that in the noise modeling we neglected many second order terms to be able to perform integration over the entire frequency space (see Equation 3.13).

### 3.4 Determination of the pixel capacitance

As we have shown in the previous section, the noise performance of a pixel detector scales with the pixel capacitance as $\sqrt{C_d}$. To achieve the optimal noise performance of the detector with the existing pixel sensors, the FE electronics has to be carefully optimized to the capacitance of the pixel sensor. The pixel capacitance is usually not well known and hard to determine. Several methods exist to determine...
3.5 PixCap

the pixel capacitance: 1. direct measurement by a RLC meter [42], 2. simulation using TCAD tools [43], or 3. extrapolation from the noise level of the pixel detector using an appropriate noise model [44].

The first method introduces a significant error of the capacitance measurement (about 5 fF), the second method is very sensitive to the geometry and knowledge of the concentration profiles, and the last method has a significant model dependence. Although each method provides certain information about the capacitance, it is not applicable for the design of the pixel FE electronics, where the designer needs to know the capacitance value as a single real number.

To precisely determine the pixel capacitance a dedicated integrated circuit has been developed. This chip is called the PixCap chip. The concept of the capacitance measurement is based on a charge pump integrated in the PixCap chip which is bump-bonded directly on the sensor as shown in Figure 3.5. This on-sensor capacitance measurement provides significantly smaller systematic error than in the case of the direct measurement with the RLC meter.

![Figure 3.5: A concept of an on-sensor capacitance measurement.](image)

Three types of the pixel sensor with dimensions compatible with FE-I4 pixel FE chip have been measured with PixCap.

3.5 PixCap

PixCap is a microelectronic integrated circuit fabricated in a 150 nm CMOS technology. A micrograph of the PixCap chip is shown in Figure 3.6. The dimensions of the chip are 3.3×2.3 mm². The core of the chip consists of an pixel array with a geometry identical with the sensors developed for the ATLAS IBL [25]. The pixel size is 250×50 µm². The pixel matrix integrated on PixCap has 8 columns and 40 rows, covering in total 320 pixels and an area of 2×2 mm². In addition, 6 test-pixels connected to the capacitors of a known capacitance are part of PixCap.

Each pixel of the PixCap contains a charge pump and a configuration logic. The functionality of the charge pump is explained in Figure 3.7 (a). The charge pump is implemented with two switches (MOSFET transistors), which are driven by two independent clock lines (CLK1 and CLK2).
Chapter 3  Pixel capacitance and electronic noise

Figure 3.6: A micrograph of the PixCap chip.

Figure 3.7: A charge-pump in the PixCap (a) periodically charges (Phase 1) and discharges (Phase 2) the pixel which causes the switching current (b) flowing from the $V_{in}$ terminal. The integral of the current pulse is directly proportional to the pixel capacitance.

The charge pump operates in two phases. In the first phase, the switch SW1 is ON and SW2 is OFF, and the pixel charges up to the input voltage $V_{in}$. In the second phase, the switch SW1 is OFF and SW2 is ON and the pixel discharges to the ground voltage. Periodical switching introduces a switching current flowing from the voltage source $V_{in}$, which is directly proportional to the capacitance. By measuring the switching current $I_{av}$, the pixel capacitance can be extracted using the following formula:

$$C = \frac{Q}{V_{in}} = \frac{\int_0^T i(t) \, dt}{V_{in}} = \frac{1}{f} \frac{\int_0^T i(t) \, dt}{f \cdot V_{in}} = \frac{I_{av}}{f \cdot V_{in}}$$  \hspace{1cm} (3.15)

Figure 3.7 (b) shows a simulation of a single current pulse into the $V_{in}$ terminal as a function of meas-
ured capacitance. An integral of the current pulse is directly proportional to the measured capacitance with almost perfect linearity as shown in Figures 3.8 (a,b). The sensitivity of the measurement increases with the switching frequency and voltage $V_{in}$. Using the typical operating voltage $V_{in} = 1.8$ V and frequency of $f = 4$ MHz, the sensitivity of 7.2 nA/fF is achieved.

Figure 3.8: Simulated transfer function of the PixCap chip (a) is almost linear. The parasitic capacitance of the switching transistors introduces an error to the capacitance measurement. The graph in Figure (b) shows the error curves in each process corner.

For completeness, a more detailed schematic of the PixCap pixel is shown in Figure 3.9. The charge pump for the pixel capacitance measurement is implemented by two MOSFET transistors M1 and M2. A transistor M3 was added for the possibility of the interpixel capacitance measurement using an additional measurement line MEAS. The functionality of the switches is programmable. Each pixel contains five configuration bits for programming the transistors M1 and M2. They can either follow the logical states at the driving clock lines CLK1 and CLK2, or they can be switched ON or OFF regardless of the state of the clock lines. One bit is used to enable/disable the CLK2 signal driving the transistor M3.

Figure 3.9: A block schematic of the PixCap chip.
A direct measurement of the average value of the pulsed current into the $V_{in}$ terminal is rather difficult and therefore a current to voltage converter with an integrating feedback has been used. A schematic of this measurement circuit is shown in Figure 3.10. A great advantage of this circuit is the possibility to adjust a conversion factor, which is equal to the resistance of the feedback resistor ($R = 100 \, \text{k}\Omega$). This circuit boosts the sensitivity of the capacitance measurement up to $0.72 \, \text{mV/fF}$. The time constant of the integrating feedback is significantly longer than a typical switching period of the charge-pump $\tau = R \cdot C = 10^5 \cdot 10^{-9} = 10^{-4} \, \text{s}$.

![Figure 3.10: A schematic of the current to voltage converters for the measurement of the small switching currents.](image)

### 3.5.1 Capacitance measurement with PixCap

A setup for the capacitance measurement and a detail view of the PixCap assembly is shown in Figure 3.11 (a, b). The measurement setup is based on the MultiIO board [45] with FPGA Xilinx Spartan 3 and on a daughter card carrying the PixCap assembly. The FPGA provides a configuration data pattern and clock signals for the PixCap. The switching current, which is proportional to the pixel capacitance, is converted to voltage and measured by a voltmeter.

The PixCap itself is not completely free of parasitic capacitance. The switching transistors have capacitance between gate and drain of about $2.5 \, \text{fF}$ (simulation), which adds to the measured capacitance. In addition, a significant fraction of the parasitic capacitance is represented by the bump-pad. The parasitic capacitance of the PixCap chip has been studied experimentally by performing a capacitance measurement without a sensor. A map of the parasitic capacitance of the PixCap chip and a capacitance histogram are shown in Figure 3.12 (a,b).

The parasitic capacitance is about $11 \, \text{fF}$. The upper half of the chip is shielded by two top metal layers and therefore the mean parasitic capacitance of the PixCap in the shielded part is slightly higher ($11.6 \pm 0.1 \, \text{fF}$), compared to the non-shielded region ($11.2 \pm 0.1 \, \text{fF}$). The parasitic capacitance is dominated by the bond-pad.
3.5 PixCap

Figure 3.11: A setup for the capacitance measurement (a) includes the FPGA based MultiIO board and a custom PCB carrying the PixCap assembly (b). PixCap is bump-bonded to the sensor and wire-bonded to the test PCB.

Figure 3.12: A capacitance map of the bare PixCap (without sensor) (a) and a distribution of the parasitic capacitance of the PixCap chip (b). Two peaks in the distribution correspond to the shielded and the non-shielded part of the PixCap chip.

An additional parasitic capacitance is present due to the solder bumps interconnecting the PixCap and the sensor. One PixCap assembly has been obtained with bumps only (see Figure 3.13), and thus the capacitance map could be determined. Not all solder bumps on the chip are perfectly spherical, some of them are shorted together, which could be caused by the imperfections of a single chip processing or by the damage during the chip packaging. Applying a cut on the good bumps, the average capacitance of the bump is 2.1 fF.

In spite of the relative simplicity of the PixCap chip, the design of its configuration register required a careful approach. The size of the configuration register is $326 \times 5 = 1630$ bits. The use of a conventional single phase shift register design (Figure 3.14 (a)) can cause a setup - hold violation. This happens when the configuration data propagate faster than the clock signal. In this case, the chip can not be configured correctly and this issue can not be fixed in any way. In the PixCap design, a dual phase shift register (Figure 3.14 (b)) has been implemented to avoid this issue. The dual phase shift register is driven by two clock lines shifting data either in even or odd flip-flops at the same time. By keeping a sufficient
Figure 3.13: A micrograph of the PixCap chip with solder bumps. Not all bumps are perfectly spherical, some of them are deformed.

The delay between the rising edges of SHIFT_CLK1 and SHIFT_CLK2 lines, a failure due to the setup-hold violation is excluded. A disadvantage of this approach is the use of a double amount of flip-flops (more silicon area) and higher power consumption. However, these issues are not critical in the PixCap design.

Figure 3.14: A schematic of a conventional (single phase) shift register (a) and a fail safe dual phase shift register (b).

The following three sub-sections are focused on the measurement of the pixel capacitance of three sensor types: silicon planar, diamond and silicon 3D sensor. In all following capacitance measurements, the parasitic capacitance of the PixCap chip has been subtracted.

### 3.5.2 Capacitance of a silicon planar sensor

The measurement of the pixel capacitance of the silicon planar sensor is not as straightforward as it was sketched in the previous section. Therefore, first the sensor itself and the effects influencing the capacitance measurement will be introduced. The measured sensor is n⁺ on n type and its cross section is shown in Figure 3.15. The sensor has been fabricated on a high resistive n-type silicon wafer. The collection electrodes (pixels) are the n⁺ type regions. The sensor backplane is formed by highly doped p⁺ region. The sensor operates with a negative high voltage connected to the backplane. The depletion region grows from the backplane towards the n⁺ collection electrodes. The total pixel capacitance $C_{\text{tot}}$ is a composition of an interpixel capacitance $C_{\text{int}}$ and a capacitance to the sensor backplane $C_{\text{bp}}$. The
3.5 PixCap

The thickness of the measured sensor is 230 µm and the spacing between pixel regions is 20 µm. The interpixel capacitance is assumed to be the dominant part of the total pixel capacitance due to the closely spaced n+ charge collection regions (see Figure 3.15).

The collection electrodes are separated by shallow p-regions (p-spray), preventing the pixels from an ohmic short connection. If the sensor is not fully depleted, all the pixels are effectively shorted and the capacitance measurement is not possible.

![Figure 3.15: Cross section of the silicon planar sensor and its capacitance components.](image)

The interpixel current has been studied experimentally with the PixCap by measuring the DC current between two adjacent pixels at a potential difference of 1.8 V as a function of a sensor bias voltage $V_{bias}$. This IV characteristic is shown in Figure 3.16. In the $V_{bias}$ range from 0 to -25 V, the sensor is not fully depleted and a large current (tens of µA) between the pixels is observed. The pinch-off effect occurs at the voltage of about -25 V. Adjusting the $V_{bias}$ to the more negative values, the interpixel current drops significantly below 1 nA. Taking into account the pixel to pixel variations, the capacitance can be measured from -35 V towards the more negative voltage.

Another restriction for the capacitance measurement with the PixCap arises from a bias grid of the sensor. A schematic of the sensor bias grid is shown in Figure 3.17. The original purpose of the bias grid is the measurement of the leakage current of the sensor. The bias grid establishes the same potential at all pixels during the measurement of the leakage current, which is a direct indicator of the sensor quality and is evaluated during sensor production. However, in case of a capacitance measurement with PixCap, the bias grid is rather an obstacle. In the default capacitance measurement configuration, all pixels are grounded by the PixCap and only one is pulsed between 0 and 1.8 V. At the phase when M1 is ON, the pixel is at 1.8 V and the leakage current of all 26880 pixels flows into the $V_{in}$ terminal through the bias grid and spoils the capacitance measurement. To avoid this effect, during the capacitance measurement all pixels must be kept at 1.8 V and the measured pixel is switched between 0 and 1.8 V. For design reasons, the switching voltage swing was reduced down to 1.1 V to achieve the correct switching.

As we have shown, the capacitance measurement works only for the sensor bias voltage above the pinch-off region. In a real pixel detector, the sensors are usually operated in a full depletion mode and at this mode, the capacitance should be measured. The depletion voltage has been determined by the measurement of the CV characteristic of the sensor. The CV characteristic of a single pixel measured with the PixCap chip is shown in Figure 3.18 (a). The total pixel capacitance is inversely proportional to the width of the depletion region. Referring to Equation 2.13, the depletion width is proportional to
Chapter 3  Pixel capacitance and electronic noise

Figure 3.16: The interpixel current as a function of the bias voltage of the silicon planar sensor.

Figure 3.17: A schematic view of the pixel layout with the bias grid.

The square root of the bias voltage. If the sensor is not fully depleted, the quantity $1/C_{tot}^2$ is directly proportional to the bias voltage. As the full depletion is achieved, the depletion width is constant and the capacitance does not change. This behavior of the sensor capacitance has been experimentally observed and is shown in Figure 3.18 (b). Full depletion voltage can be found in the transition region between the linear dependence of $1/C_{tot}^2$ on $V_{bias}$ and the region where this quantity is constant. In our case, the full depletion voltage is about -75 V.

In silicon, pairs of electrons and holes are continuously created by thermal excitations causing a leakage current in the pixels. This current adds up with the switching current generated by PixCap and influences the capacitance measurement. The influence of leakage current is more significant at small switching frequencies. Before each capacitance measurement, the leakage current of the pixel has been measured and the pixel capacitance has been corrected accordingly. For illustration, the leakage current map of the measured silicon sensor is shown in Figure 3.19. The leakage current in most of the pixels is below 2 nA. However, the top row of the pixel matrix exhibits higher leakage current, by an order of magnitude, probably due to the high electric field on the edge of the sensor.
Figure 3.18: The CV characteristic of the silicon planar sensor (a). By expressing the capacitance in the form of $1/C_{\text{tot}}^2$, the full depletion voltage of -70 V can be extracted (b).

During the capacitance measurement, the sensor has been operated slightly over-depleted at -80 V, the switching frequency was 4 MHz, the voltage at the switching pixel has been alternated from 0 to 1.1 V and the remaining pixels have been connected to 1.8 V. A capacitance map of the silicon planar sensor obtained at these conditions is shown in Figure 3.20. The capacitance of the pixels is not perfectly homogeneous across the pixel array. Capacitance gradients and pixels with a capacitance significantly larger than the average are present. This observation can be explained by fabrication process variations of the sensor and also by the non-uniformity of bump-bonding of this particularly small assembly. Therefore, a cut has been made on the homogeneous pixel region (dotted line in Figure 3.20) and the mean capacitance in this region is $(105.5 \pm 1.8) \text{ fF}$. The measurement error has been calculated from an error of the voltage measurement, an error of the current to voltage conversion, an error of the bare PixCap capacitance and an error of the leakage current determination. The capacitance measurement of a second PixCap assembly gives an average pixel capacitance of $(111.7 \pm 3.8) \text{ fF}$. 

Figure 3.19: A leakage current map of the silicon planar sensor.
3.5.3 Capacitance of a diamond sensor

Diamond has very different material properties compared to silicon. Diamond is an almost perfect insulator with a band gap of 5.5 eV. At room temperature, no free charge carriers are present in the sensor bulk and therefore thermally induced leakage current in the diamond sensor is negligible. The measured sensor sample is a polycrystalline CVD diamond with a thickness of 750 µm. The backside of the sensor is continuously sputtered by Ti/W and the surface of the sensor backplane is covered by a thin gold layer. The front-side of the diamond sensor is patterned by Ti/W and under-bump metalization. The diamond sensor does not contain any bias grid. A micrograph of the front-side of the diamond sensor is shown in Figure 3.21.

Due to the absence of the bias grid and the leakage current, the capacitance measurement of the diamond sensor is easier than in the case of the silicon planar sensor. The capacitance of the diamond pixels does not depend on the sensor bias voltage. The bias voltage for the capacitance measurement has been set to -50 V. A capacitance map and a histogram of the diamond sensor are shown in Figure 3.22 (a, b).

Two kinds of pixels can be distinguished in the capacitance map. Type I has the mean capacitance of 20.9 fF, while type II has the mean capacitance of 5.8 fF. A clear separation of these pixel types is visible in the capacitance histogram shown in Figure 3.22 (b). Type II pixels can be explained by imperfect connection of pixels by bump-bonding and therefore the capacitance of type II pixels is smaller compared to type I. By applying a cut on a well behaving pixel region (type I pixels), the mean capacitance of the diamond pixels is extracted to be (21.4 ± 0.1) fF.

In case of the diamond sensor the PixCap chip allows to measure the interpixel capacitance. This capacitance emerges from a capacitive coupling between the metallic electrodes of the front side of the sensor. The largest contribution has the capacitive coupling of the long sides of the pixel, then short sides and coupling to the backplane. The contribution of the cross-side pixels is below 1 fF. The data obtained from the PixCap chip have been compared with the data from simulation performed by Ansys.
Maxwell field solver (ver.14) [46]. Maxwell is a 3D field solver of either static or continuously varying electric and magnetic fields in material using a finite element method. A simple model of the diamond pixel sensor has been developed and a capacitance matrix (capacitive coupling between the sensitive elements of the model) has been computed using this tool. The sensor geometry and the distribution of electric field in the model is shown in Figure 3.23 (a, b).

The results of the interpixel capacitance measurement with the PixCap chip together with the results of the numerical simulations are shown in Table 3.1 and the legend is shown in Figure 3.24.

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>$C_{\text{meas}}$ [fF]</th>
<th>$C_{\text{sim}}$ [fF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>0.84</td>
<td>0.50</td>
</tr>
<tr>
<td>C2</td>
<td>1.18</td>
<td>0.89</td>
</tr>
<tr>
<td>C3</td>
<td>0.85</td>
<td>0.50</td>
</tr>
<tr>
<td>C4</td>
<td>5.55</td>
<td>6.41</td>
</tr>
<tr>
<td>C5</td>
<td>21.49</td>
<td>24.65</td>
</tr>
<tr>
<td>C6</td>
<td>5.55</td>
<td>6.42</td>
</tr>
<tr>
<td>C7</td>
<td>4.85</td>
<td>8.04</td>
</tr>
<tr>
<td>C8</td>
<td>0.73</td>
<td>0.50</td>
</tr>
<tr>
<td>C9</td>
<td>1.21</td>
<td>0.89</td>
</tr>
<tr>
<td>C10</td>
<td>0.73</td>
<td>0.50</td>
</tr>
</tbody>
</table>

Table 3.1: Measured and simulated values of the inter-pixel capacitance of the diamond pixel sensor. A legend describing the position of each capacitive fraction is shown in Figure 3.24.
Chapter 3  Pixel capacitance and electronic noise

Figure 3.22: A capacitance map of the diamond sensor (a) and a capacitance histogram (b) reveal two types of pixels. The pixels with capacitance of about 5 fF are assumed to be imperfectly connected.

Figure 3.23: A geometry of the diamond pixel sensor (a) used in the simulation of the pixel capacitance and electric field. The highest intensity of the electric field is around conductive electrodes on the front-side of the sensor.

Figure 3.24: Legend of the inter-pixel capacitance measurement presented in Table 3.1.
3.5.4 Capacitance of a silicon 3D sensor

The silicon 3D sensor used in the capacitance measurement has been fabricated on a p-type silicon bulk. The charge collecting electrodes are formed by heavily doped polysilicon pillars going through nearly the entire thickness of the silicon bulk. Due to the closely spaced collection electrodes, a higher capacitance of the 3D sensor is expected compared to the silicon planar sensor. Two assemblies have been available for the capacitance measurement. The first sensor exhibited large leakage current of tens nA biased at -30 V. To avoid the excessive leakage current, the sensor has been measured with reduced bias voltage of -5 V. A capacitance map of this pixel sensor is shown in Figure 3.25. By applying the same analysis as in the case of planar silicon and diamond sensor, the capacitance of the silicon 3D sensor has been extracted to be \((169.4 \pm 1.5) \text{ fF}\).

![Capacitance map of the silicon 3D sensor](image)

Figure 3.25: A capacitance map of the silicon 3D sensor.

Due to the exceptionally large leakage current of this 3D sensor, a second PixCap assembly with another 3D sensor has been produced. Unfortunately, during the initial testing of the assembly, the PixCap chip stopped responding and further measurements with this assembly were not possible.

3.6 Summary on the capacitance measurement

The motivation for a precise determination of the pixel capacitance is design of the pixel FE electronics as well as signal and noise modelling. In order to precisely determine the pixel sensor capacitance, the PixCap chip has been developed. The total pixel capacitance of a planar silicon, diamond and a 3D silicon sensor has been measured. The diamond sensor has the smallest capacitance (21.4 fF). The planar silicon sensor has a significantly higher capacitance of about 105 fF. The 3D silicon sensor has the highest capacitance of 169 fF. In the case of the diamond sensor, the PixCap chip allowed to perform a detailed analysis of capacitive coupling to the adjacent pixels.
The on-sensor capacitance measurement with the PixCap chip allowed to measure capacitance values with the precision of the order of a few fF and in some cases even below 1 fF. To verify the measured capacitance data, several scans of the measurement parameter space ($V_{in}$ and $f$) have been performed. The diamond pixel capacitance remained constant well within the space determined by the error bars. However, in case of the planar silicon sensor, a frequency dependence has been observed. The silicon pixel capacitance measured at 1 MHz is about 5% higher than at 10 MHz. This behavior can be explained by the fact that the impedance of the silicon pixel does not only have a pure capacitive component but also a resistive component.

The PixCap chip is not only a precise instrument for capacitance measurement, but also a tool for sensor characterization. The IV characteristics between the pixel regions and the backplane or pixel to pixel can be easily measured with arbitrary pixels. The measurement of CV characteristics with PixCap allows an optimal setting of the bias voltage of the sensor.

The capacitance data obtained by the PixCap chip have been used in studies of radiation dependence of Signal to Noise Ratio (SNR) of diamond and silicon pixel sensors and they are published in [44]. Diamond sensors tend to outperform silicon sensors in terms of SNR at large fluences of $10^{16}$ n_{eq}/cm$^2$ anticipated at HL-LHC. The strong diamond lattice, small pixel capacitance and small leakage current favor diamond sensors for applications requiring high radiation tolerance. However, high price and limited availability prevent diamond sensors from a frequent use in the high energy physics community.

The pixel capacitance is not the only capacitance contributing to the total capacitance seen by the CSA in the FE electronics chip. The bump pad and routing in the FE chip can add several fF (in the case of PixCap, the bump-bond and routing contribute on average by 8.7 fF). In addition, the gate capacitance of the input transistor in FE-I4 chip has the value of 32 fF. By comparing the gate capacitance with for example diamond pixel capacitance, it is clear that in this case the diamond pixel is not the major contributor to the total capacitance seen by FE-I4. By optimizing the CSA of the pixel FE chip to the diamond pixel capacitance, even better SNR could be achieved with the diamond sensor at large radiation doses than reported in [44].

A description of PixCap and the results of the capacitance measurement have been published in [47].
Chapter 4

New directions in pixel technologies

4.1 Motivation

Tracking detectors in modern particle physics often have to meet critical constraints on parameters like spacepoint resolution, radiation tolerance, power and material budget. The specifications are often adjusted to the edge of capabilities of available technologies. The evolution of technologies has a great impact on the performance of the detector. A motivation for the exploration of new technologies is the development of detectors for the future HEP experiments and upgrades of the existing ones.

High Luminosity upgrade of the Large Hadron Collider will require FE chips to operate even closer to the collision point than now, withstanding an extreme radiation tolerance of 1 Grad and processing high hit-rates. This application requires to use an even smaller feature size technology compared to the design of the FE-I4 - most likely a 65 nm CMOS technology. This ultra deep submicron technology allows high integration density of 800 000 gates in a square millimeter of silicon. On the other hand, the analog performance of these technologies might be poor and the solutions which worked in a 250 nm technology may not work in the 65 nm technology. This new generation of FE chips will likely integrate more digital functionality than the previous generation and will include more adjusting features to compensate the imperfections of the analog electronics. Preliminary specifications for the FE chip for the upgrade of ATLAS and CMS experiments are described in Table 4.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>≈150×25 µm²</td>
</tr>
<tr>
<td>Signal amplitude</td>
<td>10 ke⁻ (sensor thickness 100-150 µm)</td>
</tr>
<tr>
<td>Threshold</td>
<td>1 ke⁻</td>
</tr>
<tr>
<td>Hit time resolution</td>
<td>25 ns</td>
</tr>
<tr>
<td>Hit rate</td>
<td>1-2 GHz/cm²</td>
</tr>
<tr>
<td>Hit loss rate</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>Power budget</td>
<td>≈ 0.3 W/cm²</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>1000 Mrad; 2×10¹⁶ n_eq·cm²</td>
</tr>
<tr>
<td>Charge measurement</td>
<td>4-8 bits</td>
</tr>
</tbody>
</table>

Table 4.1: Preliminary specifications of the future ATLAS/CMS pixel FE chip [48].

Ultra deep submicron technologies are very expensive and therefore an alternative approach might be a suitable option for the future pixel upgrades. An alternative way to decrease the pixel size and reduce the hit frequency using a familiar 130 nm technology is by a vertical integration of the pixel FE
electronics. A two-tier pixel FE chip would allow a reduction of the pixel area by a factor of two, while the area for pixel electronics is preserved. The technology of vertical integration requires an additional processing steps to the standard CMOS process, which are not yet mature enough for a large scale production.

A different type of the pixel detectors will be needed at the future $e^+e^-$ linear colliders: CLIC and ILC [49], [50]. Vertex detectors, which will operate in the experiments at these machines, will require low mass and finely segmented pixel detectors, in order to provide a high impact parameter resolution for an efficient heavy flavor tagging. A typical specification of the pixel size is $20 \times 20 \ \mu m^2$, spacepoint resolution $3 \ \mu m$ and a total inserted material budget of 0.2% $X_0$. Required radiation tolerance is in the range of several Mrad and the hit occupancy will not exceed few percent. The bunch structures at the linear colliders will be different from those at the LHC. The bunches of colliding particles will be grouped in bunch trains containing several hundreds (CLIC) or thousands (ILC) bunches spaced by 0.5 ns (CLIC) or 308 ns (ILC). The bunch train repetition rate will be 50 Hz (CLIC) or 5 Hz (ILC). These bunch schemes allow the detectors to operate in a pulsed mode. The sensitive part of the detectors will be active during the bunch train and at this time hits will be accumulated in the pixel memory. During the gap between the bunch trains, the sensitive part of the detector will be switched off and the data from the detector will be read-out (or eventually pre-processed). This power pulsing scheme will allow a significant reduction of the power budget.

A very thin detector with small pixels and FE electronics integrated in one piece of silicon, Monolithic Active Pixel Sensor (MAPS), is an attractive technology for development of a vertex detector for experiments at ILC and CLIC. The suitability of the MAPS sensors for the LHC experiments ATLAS and CMS is questionable due to the not well known radiation tolerance of this sensor concept. The idea of monolithic pixel detectors is not new. First attempts to make monolithic detectors were made in the late 1980s [51]. However, suitable fabrication technologies were not available at that time and hybrid pixel detectors became more popular. Nowadays, the situation is different. Many research groups worldwide start introducing new concepts of MAPS, for example MAPS based on an epitaxial layer, MAPS using quadruple well (INMAPS), High Voltage MAPS (HV-MAPS), High Resistive maps (HR-MAPS) and many more. A special type of a monolithic pixel detector is DEPFET, which is an alternative technology to MAPS.

In this chapter we will discuss ultra deep submicron technologies, 3D integration and MAPS sensors.

4.2 Ultra deep submicron technologies

The use of the advanced ultra deep submicron technologies in the future experiments in HEP is favorable for several reasons. One of them is a need of high speed signal processing from 100 000 pixels per chip at the high luminosity hadron collider. Typical examples are upgrades of the experiments ATLAS and CMS. The development of a new FE chip takes years of research before the full scale chip is produced in a large quantity. During the research time and even later on, the technology must be available. The 65 nm technology is a stable technology node widely used in industry and is provided by several silicon foundries. Therefore, the 65 nm CMOS technology is a serious candidate for the development of the new FE chips for the upgrade of the pixel detectors of ATLAS and CMS experiments. The brief history of the ATLAS pixel FE chips is shown in Figure 4.1. As the transistors are getting smaller over the time, the pixel size is getting smaller as well and FE electronics becomes more complex. Downscaling
is challenging for the pixel designers and issues related to the chip design in the 65 nm technology are introduced in the following paragraphs.

Figure 4.1: A brief history of the ATLAS pixel FE chips. The FE-I3 chips are currently installed in the ATLAS pixel detector. The FE-I4 has been developed for the IBL pixel layer installed in May 2014. The next FE chip will likely be fabricated in a 65 nm technology using by now the smallest transistors in the HEP experiments.

4.2.1 Aspects of ultra deep submicron IC design

Design of the integrated circuits in the 65 nm technology is more challenging compared to the previous generation of CMOS technologies. Densely packed electronics in the design needs to follow more detailed design rules and needs to be more tolerant to the parasitic effects arising from a high density integration. A large gate leakage and off-state current of the MOSFET transistors increases the static power consumption. The ultra small transistors suffer from the degradation of their analog performance. Aspects of a deep submicron design are discussed in this subsection.

Gate leakage current

The 65 nm CMOS technology node uses a gate oxide thickness of 1.5-2 nm (depending on the concrete silicon foundry and process option). The thickness is equivalent to the several tens of silicon atoms. Assuming a typical gate voltage of 1 V, an extreme electric field of the order of $10^8$ V/m develops in the oxide. Due to the small oxide thickness, electrons from the silicon bulk can pass through the oxide to the conductive gates by a quantum tunneling effect. This effect is also present in a 130 nm technology node, but in the 65 nm node it is more significant. A comparison of the gate leakage current between the 130 nm and 65 nm technology is shown in Figure 4.2 (a, b).

In the 65 nm CMOS process, the gate leakage current of a $1 \times 1 \mu m^2$ transistor can be as high as 350 pA. In the design of a pixel FE chip, the gate leakage current has several impacts. The FE chip usually contains thousands of identical pixel electronic cells. The analog electronics requires biasing, which is usually done by current mirrors as shown in Figure 4.3. If each pixel introduces a leakage current of 500 pA, then the entire pixel matrix of 100 000 pixels consumes 50 µA of leakage current, increasing the total power budget. In addition, the biasing circuit has to be designed in a way, that it is able to bias not only the transistor MX (referring to Figure 4.3), but also to cover the loss of the current due to the gate leakage. In dense digital circuits, the static power consumption due to the leakage current can be comparable with the dynamic power consumption.
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Figure 4.2: A comparison of the gate leakage current of NMOS (a) and PMOS transistors (b) in the 130 nm and 65 nm technology. Dimensions of the transistors are $1\times1 \mu m^2$. These data have been obtained by circuit simulations.

Figure 4.3: A current mirror is widely used to bias analog circuits in pixels. Each pixel drains a small gate-leakage current. In case of a large pixel matrix (100,000 pixels), the bias current source has to be designed to cover this extra leakage current.

The 65 nm technology is probably the last CMOS technology node using the silicon dioxide as a gate dielectric. The technologies with a feature size smaller than 65 nm use a different type of the gate dielectric - high $\kappa$ materials (a hafnium based dielectric with a metallic gate) which can be significantly thicker to provide the equivalent transistor parameters. The suitability of technologies smaller than 65 nm for HEP applications is questionable, because problems with radiation tolerance may arise with thicker gate dielectric. Nowadays, very little is known about radiation effects in these new materials.

**Off state current**

A combination of very short channel transistors with low threshold voltage introduces a non-negligible current between the drain and source when the transistor is off. In a transistor with dimensions of $480\times60$ nm$^2$ (the minimum drawn channel length in 65 nm technology is 60 nm), the off-state current can easily reach 100 pA. In a large pixel chip, the off-state current increases the static power consumption.

The threshold voltage of the MOSFET transistor has a great impact on the off-state current. An advanced CMOS technologies usually offer transistors in several threshold voltage domains. Transistors
4.2 Ultra deep submicron technologies

with High Voltage Threshold (HVT) have a small parasitic off-state current flow, but at the same time they have limited current driving capability in the on-state. The HVT transistors are therefore slower. Low Voltage Threshold (LVT) transistors are more suitable for the design of high speed electronics, but at the same time introduce a large off-state current.

To optimize the speed and the static power consumption, the integrated circuit can be divided into several domains using transistors with various threshold voltages, according to the requirements on the speed of the given circuit block.

In pixel detectors, the off-state current represents a critical issue. A large radiation dose introduces a negative shift of the threshold voltage of the NMOS transistors, which can easily increase the off-state current by more than 2 orders of magnitude. To eliminate this problem, large pixel FE chips often use custom, radiation hardened, digital cells. The influence of the radiation dose on the off-state current of the transistors fabricated in the 65 nm technology has been studied at CERN [52] and is shown in Figure 4.4.

![Figure 4.4: The off-state current of the NMOS transistors of various dimensions (W/L) as a function of the Total Ionizing Dose (TID). The absolute value of the off-state current and its scaling with radiation dose strongly depend on the transistor dimensions [52].](image)

**Analog performance**

As we have shown in Chapter 2, the performance of the analog circuits (amplifiers, DACs, biasing circuits etc.) is greatly influenced by two key parameters of the transistors: transconductance $g_m$ and output conductance $g_{ds}$. A high value of $g_m$ is important to achieve high gain of the amplifiers and small $g_{ds}$ is desirable to maintain high internal resistance of the current sources often used in the analog design. The
transistor parameters $g_m$ and $g_{ds}$ of the 130 nm and 65 nm technologies are compared in Figure 4.5 (a, b) and Figure 4.6 (a, b).

![Figure 4.5](image1.png)

**Figure 4.5**: A comparison of the transconductance of the NMOS (a) and PMOS (b) transistors in the 130 nm and 65 nm technology as a function of the channel length. These data have been obtained by circuit simulations.

![Figure 4.6](image2.png)

**Figure 4.6**: A comparison of output conductance of NMOS (a) and PMOS (b) transistors in 130 nm and 65 nm technology as a function of channel length. These data have been obtained by circuit simulations.

The simulation data indicate that the transconductance of the MOSFET transistors in the 65 nm technology is comparable (or even better) to those fabricated in the 130 nm technology. The output conductance increases as the transistor becomes shorter. This effect is more pronounced in the 65 nm technology due to the short channel effects. This behavior makes an impact on the quality of the current sources and current mirrors.

**Voltage swing**

As the transistor feature size decreases, the maximum allowable power supply voltage decreases as well. The core transistors in the 130 nm technology have a maximum $V_{dd}$ voltage of 1.4 V, while in 65 nm it is 1.2 V. Although lowering the power supply voltage is beneficial for decreasing the power consumption, it severely limits the voltage swing of for example amplifiers designed in this technology. A multiple
cascading of the transistors in the 65 nm technology is difficult due to the limited voltage headroom as well. This feature of ultra deep submicron technologies has an impact on the analog performance of the FE electronics in terms of open loop gain and linearity of CSA.

**Power**

The power consumption of a FE pixel chip can be divided into two domains: analog and digital. The power budget of the analog domain is determined by the requirements of speed (rise-time and timewalk). In case of the high luminosity upgrade of the LHC experiments, the speed of the analog electronics must be the same (if not better) as the speed of the existing pixel chips, while the pixel area will be reduced by a factor of almost four. To preserve the speed, the analog power budget of a pixel will remain rather constant, while the power density tends to increase by a factor of four.

The dynamic digital power depends on frequency, capacitance of gates, power supply voltage and number of constantly switching gates. The master clock frequency of a pixel chip is derived from the bunch crossing frequency at LHC (40 MHz) and it will remain constant at a high-luminosity phase. The power supply voltage will be lower than in the 130 nm technology (1.2 V, or if underdriven the logic can also work with 1.0 V). The number of gates in the pixel area will definitely be larger than in the previous chip generation. However, by carefully choosing the architecture and implementing the advanced functions as for example clock gating, the power budget of the digital logic of the pixel chip can be optimized.

### 4.2.2 Existing prototypes and results

In this section, we introduce two prototypes of pixel FE chips designed in the 65 nm technology and one advanced FE chip designed in 130 nm technology which were developed by various research groups.

**ATPIX65A**

ATPIX65A is the ATLAS PIXel prototype Array - a pixel FE demonstrator chip for a hybrid pixel detector designed in the 65 nm CMOS technology by the Lawrence Berkeley National Laboratory research group [53]. The chip contains a pixel matrix of 16×32 pixels with dimensions 125×25 μm². In order to fit into a bump-bonding process with a minimum bump pitch of 50 μm, a staggered layout of the bond-pads is used in this design. The layout of the ATPIX65A with staggered layout of the bond-pads is shown in Figure 4.7 (a, b).

The pixel electronics contains an analog pixel FE and a simplified digital logic. The area of the analog FE is only 65×25 μm². The results of testing show the noise level of about 150 e⁻ and the threshold dispersion of 350 e⁻ before and 60 e⁻ after threshold tuning. The ATPIX65A has been studied under irradiation by protons up to a dose of 600 Mrad. No significant degradation of the analog performance has been observed. However, a slight increase of the noise level and a change of the bias current has been observed after irradiation.
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Figure 4.7: ATPIX65A pixel front-end demonstrator chip (a) designed at LBNL [53] uses a staggered layout of the bond-pads (b).

CLICpix

CLICpix is another hybrid pixel FE prototype chip designed in the 65 nm CMOS technology [54], [55]. CLICpix is shown in Figure 4.8. The CLICpix has been designed at CERN and its purpose is to evaluate this technology for usage in experiments in the future CLIC collider. Specifications of the CLICpix are therefore different from those of the ATPIX65. The goal of the CLICpix is to achieve a pixel size of 25×25 µm$^2$ and advanced hit processing by the means of Time Over Threshold, Time Of Arrival and data compression. Due to the very small pixel size, the sensor cannot be connected using a standard bump-bonding process. The analog tests showed small gain variations of 4.2%, the threshold dispersion after tuning of 22 e$^-$, and the noise level of 51 e$^-$ (without sensor).

Figure 4.8: CLICpix - a prototype FE chip for the experiments at the future CLIC collider [55].
4.2 Ultra deep submicron technologies

The test results of both prototypes mentioned above designed in the 65 nm CMOS technology indicate good analog performance, provide good radiation tolerance and at the same time leave space for the integration of complex digital electronics.

**Timepix3**

Timepix3 has been designed in 130 nm technology but by its complexity and integrated functionality represents a separate direction in the development of the pixel FE chips and therefore it is introduced in this section. Timepix3 is a pixel array of dimensions 256×256 pixels. The pixel size is 55×55 µm². In total, 177 million transistors are integrated in Timepix3. The pixels integrate a functionality of hit counting for radiation imaging, measurement of ToT (Time over Threshold) for spectroscopic measurements and a precise ToA (Time of Arrival) measurement with resolution of 1.56 ns. The analog FE electronics is based on a CSA with the Kummenacher feedback circuit [56] allowing processing of the charge of both polarities and at the same time compensate the leakage current of the sensor. Analog part occupies only a quarter of the pixel area. The digital logic is common for one superpixel (2×4 pixels) allowing an effective data handling. The layout of Timepix3 is shown in Figure 4.9. The readout is continuous and zero suppressed. One of the operating modes allows a binary pixel readout of events tagged with bunch crossings which makes Timepix3 suitable for HEP applications. More details about Timepix3 can be found in [57].

![Figure 4.9: Layout of Timepix3 [57].](image-url)
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4.3 Vertical integration

Miniaturization of electronics and increase of its complexity brings into focus an option of vertical integration using 3D interconnection technologies. A parasitic resistance and capacitance of the conductive interconnecting paths do not decrease with the transistor dimensions. Many commercial applications (typically smart-phones) require a fast interconnection between the complex digital blocks as for example CPU and a memory. A solution coming from industry is 2.5D or 3D integration - vertical integration of the integrated circuits. The 2.5D technology uses the interconnection technology for expanding the high density interconnection arrays using silicon interposers. One example of a 2.5D vertical chip integration is shown in Figure 4.10.

Figure 4.10: An example of a 2.5D vertical chip integration used in a commercial high performance FPGA [58]. A dense array of IO pads of a complex digital chip is expanded using a silicon interposer. The entire assembly can be finally connected to a PCB by a cheap BGA technology.

The integration of many functional layers in one assembly for a relatively low cost by vertical integration represents an attractive option not only for industry, but also for HEP experiments. One possible implementation of this technology in the pixel FE chips is separating the analog and the digital part of the pixel and integrating them vertically. The same procedure can in principle be used for other components of a pixel module like opto-module or cooling capillars as shown in Figure 4.11. Apart from reducing the pixel size, this solution brings additional benefits. Since the sensitive analog part is integrated on a physically different silicon chip than the noisy digital part, the crosstalk between these two parts will be minimized. It allows the fabrication of different tiers at different foundries and possibly in different technologies. In an extreme case, the analog pixel can be fabricated in cheaper 130 nm technology, but the digital part can be made in 65 nm technology.

4.3.1 Aspects of vertical integration

In spite of the simplicity of the idea of vertical integration, a practical implementation is rather difficult. Vertical integration of the integrated circuits involves non-standard processing steps. One of the critical steps is electrical connection from the top side of the chip to the bottom side, which is implemented by a Through Silicon Vias (TSV).
TSV can be formed in two ways:

**Via first** - TSV is processed on a blank silicon wafer within first few steps of the CMOS process. High temperature operations can be used to make the TSV. A via first TSV technology must be compatible with the CMOS process and therefore it can only been done in several silicon foundries.

**Via last** - TSV is made after a full CMOS processing. In the pixel FE chips, it is often needed to transfer just a few (1 or 2) conductive paths from the top to the bottom side of the chip. The TSV pitch is therefore relaxed and the TSV can be produced at a different factory than in which the electronics has been fabricated.

Vertical integration of the pixel electronics requires a high density interconnection technology. Interconnection is usually done by thermocompression. The thermocompression interconnection technology involves deposition of metallic (Cu) pads on both wafers to be interconnected. The connection is established by bringing the wafers together and applying a pressure at high temperature. The wafers are then connected at the exposed Cu pads by thermal vibrations of the Cu atoms. This connection has a very small resistivity (comparable with Cu) and a small pitch of the order of a few µm can be achieved. Unlike the bump-bonding technology, once the chip assembly is interconnected, it can not be reworked if needed.

Fabrication of large silicon chips routinely achieves a yield of 50-80% (depending on complexity). When two tiers are fabricated with a non-standard process (including TSV) and are interconnected, the yield can easily drop to very low levels. Yield optimization and design for testing is of the central importance in the design of the 3D electronics. Complex integrated circuits consume and also dissipate large power. The ability to dissipate heat is proportional to the surface area of the silicon chip. When integrating several tiers on top of each other, the dissipated heat can easily increase several times, while the surface area radiating heat remains constant. An unequal power consumption between different tiers can lead to a thermal stress, which can eventually break the connections between the tiers.
To summarize, the design of 3D electronics requires to pay an increased attention at:

- Yield optimization of each tier
- DFT (Design For Testing)
- Equal power consumption between tiers to minimize thermal stress
- Minimization of power consumption

### 4.3.2 FE-TC4

FE-TC4 is a prototype chip designed in 130 nm technology allowing vertical integration. The design of this chip is based on the design of the FE-I4 and has been submitted in April 2009 within a MPW run organized by the HEP 3D consortium [59], lead by Fermilab. A micrograph of one reticle of the silicon wafer with multiple designs is shown in Figure 4.12 (a).

![Micrograph of silicon wafer](image)

**Figure 4.12**: A micrograph of a silicon wafer (a) shows one reticle containing multiple designs. Red rectangles mark designs belonging to the FE-TC4 project. A concept of vertical integration of analog and digital tier of the FE-TC4 chip is show in Figure (b).

Analog and digital parts of the pixels are located on different silicon dies designed to be vertically integrated after the electronics is processed as shown in Figure 4.12 (b). Both tiers were processed on the same wafer in the way that they can be combined with their counterparts from another wafer. This particular technology uses the via first TSV with the via diameter of 1.2 \( \mu m \) and via pitch of 2.5 \( \mu m \), and depth of about 10 \( \mu m \). Both tiers have been tested separately (before interconnection). Their electrical parameters are comparable with the FE electronics integrated on the FE-I4. However, certain difficulties have been faced in order to produce a full 3D assembly, which has been finally delivered for testing in late 2012. More details about the FE-TC4 can be found in [60], [61].
4.4 Monolithic Active Pixel Sensors

4.4.1 Introduction

A hybrid pixel detector technology is currently a very well established technology for development of pixel detectors. The sensor and FE chip are separate entities. The (planar) sensors are fully depleted and thus sensitive in the entire volume. The FE chips are fabricated using commercial deep submicron CMOS technologies allowing integration of complex electronics necessary for trigger operated pixel detectors. Both components of the detector have reached maturity. In spite of the success of the hybrid pixel detectors, they have a number of limitations. Three different technologies are needed to produce a hybrid pixel detector (sensor, front-end chip and interconnection). The sensitive area of the pixel detector is covered twice: first by the sensor and second by the FE chip. The interconnection represents a significant part of the cost of the entire detector, lowers production yield and limits the minimum achievable pixel size. For the development of a large scale tracking system, the hybrid pixel technology is a rather costly solution.

The idea of Monolithic Active Pixel Sensors (MAPS) is an integration of a sensor and FE electronics on the same silicon, thus overcoming the interconnection issues. An additional advantage of this solution is a possibility to design small pixels with small capacitance and potentially low noise. The MAPS sensor can be thinned down to a thickness of several tens of µm. A thin sensor with fine pixel granularity is demanded in the future HEP experiments, for example at the future linear collider CLIC [50] or ILC [49]. At the time of writing this thesis, a pixel vertex detector based on the MAPS technology is being built for the upgrade of the STAR experiment [62] at the RHIC accelerator.

The concept of MAPS originates from late 1980s [51]. For a long time, the performance of the MAPS sensors has been limited due to the absence of suitable technologies. The integration of a sensor and the complex deep submicron CMOS electronics on the same chip is a technological challenge. The sensor requires pure, high resistivity silicon (several kΩ) and high depletion voltage, while deep submicron CMOS electronics is usually processed on low resistivity (<10 Ω) silicon and biased with low voltage (<2 V). The technologies adopting the desired features have not been widely available until the last decade. Nowadays, many commercial applications require technologies meeting the requirements for fabrication of the MAPS sensors. The CMOS image sensors are a typical example. In recent years, the market of the CMOS image sensors started to grow largely due to their massive integration in mobile devices. The sales of the CMOS image sensors are currently higher than the "old fashioned" CCDs [63] (even though the high-end astronomy cameras still use CCDs). Therefore, these technologies become cheaper and available to the HEP community. Depending on the technology, several concepts of the MAPS sensors exist and they are described in the following paragraphs.

4.4.2 MAPS fabricated on epitaxial layer

The MAPS sensors can be fabricated using a standard CMOS process with an epitaxial layer as reported in [64]. The epitaxial layer is a defect-free layer of silicon grown on a silicon wafer. The thickness of the epi-layer rarely exceeds 15 µm and its resistivity is typically less than 10 Ω·cm. The sensitive elements of the sensors are reverse biased diodes formed in the epitaxial layer. The depletion depth of the charge collection diodes is a few µm. The charge generated by a traversing charged particle is transported by a diffusion mechanism to the close proximity of the PN junction and then drifts towards the collection
electrodes. The charge collection time is of the order of 100 ns. A typical signal generated by a MIP particle is about 600 electrons and the noise level can be as low as 20 electrons. A cross section of this type of sensor is illustrated in Figure 4.13.

The signal from the collection diode is processed by a three transistor structure (3T). At the beginning of the measurement cycle, the pixel is reset by transistor M1. The signal charge induces voltage changes on the gate of the transistor M2 and modulates its current. The transistor M3 enables the current to flow through the transistor M2. The advantage of this sensor technology is its simplicity and compatibility with large variety of CMOS processes.

The complexity of pixel electronics of this MAPS concept is severely limited by the fact that PMOS transistors can not be implemented. An additional n-well, in which the PMOS transistor is embedded, would behave as an additional collection node, which would decrease the signal charge collected by the original collection diode. This drawback can be overcome by using an additional deep p-well effectively shielding both transistor types from the sensitive epi-layer. This sensor concept is called INMAPS (Intelligent MAPS) [65] and is illustrated in Figure 4.14.

Figure 4.13: A concept of the MAPS sensor fabricated in an epitaxial layer (left). The signal is measured by 3T transistor structure shown in the right part of the picture.

Figure 4.14: A deep p-well acts as a shielding of the n-well hosting the PMOS transistor, thus allowing the integration of a full CMOS electronics in the pixel.
4.4 Monolithic Active Pixel Sensors

4.4.3 High Voltage MAPS

High Voltage MAPS (HV-MAPS) are a class of MAPS fabricated by a standard high voltage CMOS technology. These technologies are well established and easily available. The sensitive element is again a diode, which is reversely biased by a voltage of several tens of volts applied to the p-type silicon bulk. The width of the depleted region in the low ohmic silicon bulk is about 10 µm. A high bias voltage generates a strong electric field in the depleted region, establishing a fast charge collection.

The concept of the HV-MAPS sensor is shown in Figure 4.15 (a). A sensitive diode is implemented in a deep n-well. The same deep n-well encloses the pixel electronics. Both types of transistors (NMOS and PMOS) can be integrated in the pixel. An ordinary n-well of the PMOS transistors is ohmically connected with the charge collecting deep n-well. This feature introduces coupling between the PMOS bulk and the sensor part. Any switching performed by the PMOS transistors couples to the sensor part and might be the source of an unwanted cross-talk. An integration of the complex digital electronics in the HV-MAPS pixel is therefore difficult. One solution of this issue is hybridisation of the HV-MAPS sensor as shown in Figure 4.15 (a, b).

In a hybridized assembly, the HV-MAPS chip operates as a sensor, amplifier and discriminator, while the complex FE chip (FE-I4) performs the hit processing and trigger-based read-out. Only digital information is transmitted between the sensor and the digital chip. These two counterparts can be interconnected by a glue establishing an AC coupling. The glued interconnection does not involve difficult and expensive bump-bonding process and the minimum pixel size is not limited by the size of the bump-bond. This concept has been proven to work and to be radiation hard. More details about HV MAPS can be found in [66] and [67].

4.4.4 High Resistive MAPS

HV-MAPS and MAPS fabricated on the epitaxial layer are sensitive only up to a very shallow region (≤ 15 µm), while most of the silicon bulk is insensitive. High-resistive MAPS (HR-MAPS) use a high resistive silicon bulk. The depletion region in this high purity silicon can be extended up to several tens of µm or depleted completely, thus allowing to collect more signal charge. HR-MAPS technologies are
therefore good candidates for the fabrication of a detector with high SNR and potentially high radiation tolerance.

An example of the HR-MAPS chip is LePix [68] fabricated in a 90 nm standard CMOS process using high resistivity silicon substrate of 500 $\Omega \cdot \text{cm}$. This prototype uses an n-well as a charge collection electrode integrated in a high resistive p-substrate. Pixel electronics is placed inside this n-well. The pixel electronics in this prototype contains one PMOS transistor for pixel reset and one transistor for charge to current conversion. Signal processing is implemented outside the pixel array from all pixels at the same time. This read-out architecture requires a dense routing of the signal lines in the pixel matrix, thus representing a danger of crosstalk between the pixels.

## 4.5 Summary on the future pixel technologies

Three new directions in pixel detector development have been introduced: complex FE electronics fabricated by ultra deep submicron technologies, vertical integration and monolithic pixel technologies.

Hybrid pixel detectors represent the state of the art of the modern pixel technologies with excellent tracking performance. A disadvantage of this technology is the hybridization process, which is expensive and not always reliable. Further evolution of the hybrid pixel technologies will likely involve the use of the ultra deep submicron CMOS technologies (65 nm) for implementation of the pixel FE electronics.

An alternative way to reduce the pixel size is by vertical integration. Stacking of several layers of silicon chips on the top of each other can potentially allow the vertical integration of several functional layers (analog, digital, optoelectronics, power and cooling) in the pixel area. However, stacking of each layer will introduce an additional technological complexity and imposes the same kind of difficulty as the bump-bonding process in the standard hybrid pixel detectors. Vertical integration will only work if all layers of the 3D stack and the 3D interconnection including the TSV fabrication can be produced with a high yield. At the time of writing this thesis, it is not the case. After many years of effort to produce the FE-TC4 chip assembly, only a few assemblies containing 2 layers of electronics have been proven to work. If this technology is not a full industrial standard, the fabrication of 3D electronics will be too ineffective for development of a large tracking detector.

Monolithic pixel technologies (MAPS) use a different approach than hybrid pixel technologies. Sensor and FE electronics are fabricated on one piece of silicon by one silicon foundry and without any extra post-processing. Several different approaches have been introduced: epitaxial MAPS, MAPS using CMOS electronics in a quadrupole well, high voltage MAPS and high resistive MAPS. Each of the concept has its advantages and disadvantages. The MAPS concept allows the fabrication of very small pixels with sensor and FE electronics integrated in a pixel area. However, in a large HEP experiment, the detector must operate in a trigger based mode, requiring complex digital electronics in the pixel. This issue is targeted by hybridization of the HV-MAPS sensor and FE-I4 chip. In this case, the hybridization is made by glue, which is far a simpler process than bump-bonding or 3D integration. In spite of many available MAPS technologies, they can not (yet) outperform the conventional hybrid pixel detectors in terms of SNR, radiation hardness and speed of signal processing. However, in the case of large tracking systems, the cost of the technology becomes a more critical parameter than in a small vertex detector. From this point of view, the CMOS MAPS sensors may become a perspective solution for large area trackers.
Chapter 5

Pixel front-end development in 65 nm CMOS technology

5.1 Introduction

Bonn University was among the very first research institutes in the HEP community experimenting with the 65 nm CMOS technology. Since the beginning in 2011, it was clear how big the potential of this technology has in terms of the integration density. However, very little was known about an impact of the downscaling of the transistor sizes on the analog performance of the pixel FE electronics and whether it is possible at all to design an analog pixel FE in the 65 nm technology. In order to explore this new territory, two prototype chips have been designed, manufactured and characterized. They are: FE-T65-0 and FE-T65-1, which will be described in detail in this chapter.

At the time of writing this thesis, the 65 nm CMOS technology is used by many HEP groups worldwide and this technology is a strong candidate for the design of a new pixel FE chip for the ATLAS and CMS pixel detectors, and possibly also for other experiments. A new collaboration - RD53 collaboration [69] has been established for the development of a new ATLAS/CMS/CLIC pixel FE chip foreseen for the high luminosity LHC upgrade and for the linear collider project CLIC.

5.2 FE-T65-0

FE-T65-0 is a prototype of an analog FE designed in the 65 nm CMOS technology and it is a part of a larger silicon chip DHPT01. The dimensions of FE-T65-0 are approximately 1×1 mm². Four different variants of an analog FE are integrated in the design. A micrograph of the DHPT01 with a wirebonded the FE-T65-0 and a layout of one of the FEs are shown in Figure 5.1 (a, b).

The layout of one single FE variant has dimensions of 36×25 µm² and can therefore be easily integrated in a small pixel. Each analog FE consists of a CSA connected to a discriminator. Each CSA has an additional analog buffer connected to an IO pad of the chip for monitoring purposes. These FE variants differ either by feedback capacitance of the CSA or by the architecture of the discriminator. The variants of the FE electronics are labeled FE-1 - FE-4 and they are described in Table 5.1.

The feedback capacitance of 5 fF has been selected to provide a sufficient gain for amplifying a signal of 20 ke⁻ per MIP from the silicon planar sensor. The motivation to include also a CSA with 3 fF feedback capacitance originates from a possibility to use the diamond pixel sensors, which provide smaller signal than the silicon planar sensors.
Chapter 5  Pixel front-end development in 65 nm CMOS technology

Figure 5.1: A micrograph of the DHPT01 chip (a) which contains four square chiplets. The chiplet FE-T65-0, which integrates four analog FE circuits, is wirebonded to the PCB. Layout of one analog FE is shown in Figure (b).

<table>
<thead>
<tr>
<th>FE variant</th>
<th>CSA feedback [fF]</th>
<th>Discriminator</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE-1</td>
<td>5</td>
<td>dynamic</td>
</tr>
<tr>
<td>FE-2</td>
<td>3</td>
<td>dynamic</td>
</tr>
<tr>
<td>FE-3</td>
<td>5</td>
<td>continuous</td>
</tr>
<tr>
<td>FE-4</td>
<td>3</td>
<td>continuous</td>
</tr>
</tbody>
</table>

Table 5.1: Different variants of the analog FEs implemented in the FE-T65-0.

5.2.1 Charge sensitive amplifier

The core of the CSA is implemented with a cascode amplifier. The schematic of the amplifier is shown in Figure 5.2 (a, b). The input NMOS transistor M1 is biased by a current of 6.5 µA provided by a divided current source implemented by the PMOS transistors M3 and M4. The current splitting allows the biasing of the cascode transistor M2 by a small current provided by M3, while the high $g_m$ transistor M1 is biased by a larger current. This solution allows a better optimization of gain and speed of the amplifier than biasing by a single current source. The output voltage of the amplifying stage is buffered by a source follower implemented by the NMOS transistors M5 and M6. The open loop voltage gain of the CSA is 355 (51 dB) and the bandwidth is 5.7 MHz. The reset of the CSA is implemented with a switch, allowing the operation with the reset frequency up to 40 MHz.

5.2.2 Continuous discriminator

The continuous discriminator is a "standard" discriminator widely used in pixel FE electronics (for example FE-I4). In this thesis we call this discriminator a continuous discriminator to distinguish it from a dynamic discriminator which is introduced in the following paragraph. The continuous discriminator
is implemented with a two stage amplifier providing high gain. The first stage is a differential amplifier with NMOS input transistors and the second stage is a common source stage. The output of the discriminator is further buffered. This discriminator operates asynchronously - it appears at the output of the discriminator immediately (within the "analog speed" of the discriminator) when the input signal exceeds the detection threshold and disappears when the signal drops below the threshold. The nominal power consumption of the discriminator implemented in FE-T65-0 is 2.4 $\mu$W and the standard deviation of the input voltage offset is 4.5 mV.

### 5.2.3 Dynamic discriminator

The dynamic discriminator operates synchronously with a driving clock signal. The core of the discriminator is a latch. When a rising edge of the clock signal comes, the latch is brought into a metastable state for a short moment and then quickly flips either to state 1 or 0, depending on the voltage levels on the input terminals. The latch remains in this state and can only change when the next rising edge of the clock signal. A clear advantage of the discriminator is effectively a zero power consumption in the quiescent state. When the discriminator is clocked, its power consumption is directly proportional to the switching frequency. The discriminator has a very small intrinsic delay ($<1$ ns). With an appropriate CSA, the dynamic discriminator can save the power budget of the pixel. A schematic of the dynamic discriminator is shown in Figure 5.3.

### 5.2.4 Measurements with FE-T65-0

The test-chip FE-T65-0 has been characterized stand alone (without the sensor), with an external charge injection circuit. Figure 5.4 shows a response of the CSA to the charge injection and subsequent reset. The analog signal from the CSA is buffered by a large on-chip source follower. Due to the large capacitance of the IO pad and the capacitance of the oscilloscope probe, the rising edge is slower than in the design simulation. The CSA can process signal charge with the frequency of 40 MHz, but at the expense of high power consumption of more than 20 $\mu$W. In case of using a smaller bias current, the CSA becomes unstable during the reset phase, when the feedback switch interconnects the input and output of the CSA. Therefore, the FE-T65-0 has been further tested with a charge injection frequency of 1 MHz to avoid unstable conditions.
The FE variants equipped with the continuous discriminator (FE-3 and FE-4) have better performance than the variants with the dynamic discriminator. Testing of the FE-T65-0 revealed an excessive voltage offset of the dynamic discriminator, which increases with its threshold voltage to more than 100 mV. The reason for the large offset is non-optimal size of the transistors, as well as the discriminator architecture containing four transistors in one current branch, which can not operate properly with a small power supply voltage of 1.2 V required by this ultra deep submicron technology. The voltage offset measured as a function of the threshold voltage is shown in Figure 5.5.
The FE variants with the continuous comparator were tested in detail. Transfer functions (voltage amplitude at the output of the CSA as a response to the charge injection) were measured with the FE variants FE-3 and FE-4 using two methods:

- Voltage measured by oscilloscope
- Voltage measured indirectly on the internal output node of the CSA by means of discriminator response

The results of these measurements are shown in Figure 5.6 (a, b). The voltage amplitude measured with the FE variants FE-3 and FE-4 is proportional to the injected charge. The linear range of the variant FE-3 is larger than in the case of FE-4, due to the larger feedback capacitance. The limitation arising from buffering the analog signal and measuring it externally by oscilloscope is clearly seen here. The analog buffer has the voltage gain of about 0.75. The response of the CSA measured by oscilloscope is therefore smaller than the response determined by the on-chip discriminator.

The transfer functions of the CSA and gain have been simulated during the design of the FE-T65-0 chip. A comparison of these parameters obtained from the measurements and from the design simulations is shown in Figure 5.7 (a, b) for the FE-3 variant and in Figure 5.8 (a, b) for the FE-4 variant. The measured data agree very well with the data originating from the design simulations.

The noise performance of the FE variants FE-3 and FE-4 was determined with a threshold scan. By performing multiple charge injections and counting hits at the output of the discriminator and increasing the discrimination threshold, a characteristic s-curve was obtained. If the FE electronics is noiseless, the s-curve is described by an ideal step function. However, an electronic noise, superimposed on the signal, smoothes out the step function. Steepness of the s-curve is a measure of the noise performance. Assuming that noise amplitude has the Gaussian distribution, the s-curve of the number of hits \( n_{\text{hits}}(V_{\text{thr}}) \) can be fitted by the following function:
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Figure 5.6: Transfer functions of the CSAs of the FE variants FE-3 (a) and FE-4 (b).

Figure 5.7: Transfer characteristic (a) and gain (b) of the CSA implemented in the FE of the variant FE-3. The measured data correspond to the data from design simulation.

\[ n_{\text{hits}}(V_{\text{thr}}) = n_{\text{hitsMax}} \cdot \frac{1}{2} \left( 1 - \text{erf} \left( \frac{V_{\text{thr}} - V_{\text{thr50}}}{\sqrt{2} \cdot \sigma} \right) \right) \]  \hspace{1cm} (5.1)

\[ n_{\text{hitsMax}} \] is the number of charge injections at a given threshold voltage \( V_{\text{thr}} \). \( V_{\text{thr50}} \) is the threshold voltage at which 50\% of the hits pass the discriminator. \( \sigma \) is the standard deviation of the noise voltage amplitude and \( \text{erf} \) is the error function defined by the following formula:

\[ \text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_{0}^{x} e^{-t^2} dt \]  \hspace{1cm} (5.2)

An example of the threshold scan, obtained with the FE variant FE-3 with the injected charge 4 ke\(^{-}\), and fitted by the function described by Equation 5.1, is shown in Figure 5.9 (a).

By using the information about noise voltage and gain of the CSA, the Equivalent Noise Charge (ENC) of the FE-3 and FE-4 was computed and is shown in Figure 5.9 (b). The noise level in both cases is about 80 electrons and increases slowly with the injected charge.
5.3 FE-T65-1

Figure 5.8: Transfer characteristic (a) and gain (b) of the CSA implemented in the FE of the variant FE-4. The measured data correspond to the data from design simulation.

Figure 5.9: An example of the threshold scan (a), obtained with the FE variant FE-3 at the injected charge of 4 ke\textsuperscript{-}. Parameters of the fit are: \( V_{\text{thr}_{S0}} = 0.472 \) V and \( \sigma = 2.3 \) mV. A set of the threshold scans has been used to determine the ENC of the FE variants FE-3 and FE-4 as a function of the injected charge (b).

Laboratory testing of the FE-T65-0 indicates a good analog performance of the FE prototypes in terms of gain, linearity, noise levels and proves this technology to be suitable for design of the analog pixel electronics. However, design of a more complex prototype chip is needed to better understand the noise behavior with connected sensor capacitance, threshold dispersion of many pixels and dynamic performance of the analog FE. There is also ample room for improvements, particularly in the design of the dynamic discriminator. These points are targeted in the next version of the pixel FE prototype chip FE-T65-1.

5.3 FE-T65-1

FE-T65-1 is a successor of the previous prototype FE-T65-0. Dimensions of this pixel FE prototype are approximately 1×1 mm\textsuperscript{2}. A micrograph of the chip and layout of the pixel matrix are shown Fig-
A pixel array of 32 pixels arranged in one double column is integrated in this chip. Four different variants of the analog pixel electronics were integrated in the array. Each variant contains 8 pixels. These variants are described in Table 5.2. One of the goals of the FE-T65-1 is a comparison of the time-continuous, switched and mixed FEs.

<table>
<thead>
<tr>
<th>FE variant</th>
<th>CSA</th>
<th>Discriminator</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE-1</td>
<td>Continuous reset</td>
<td>Continuous</td>
</tr>
<tr>
<td>FE-2</td>
<td>Continuous reset</td>
<td>Dynamic</td>
</tr>
<tr>
<td>FE-3</td>
<td>Switched reset</td>
<td>Continuous</td>
</tr>
<tr>
<td>FE-4</td>
<td>Switched reset</td>
<td>Dynamic</td>
</tr>
</tbody>
</table>

Table 5.2: Different variants of the analog FEs implemented in the FE-T65-1.

A layout of a single pixel is shown in Figure 5.11. The pixel layout is divided into analog and digital part. The analog part contains a CSA with tunable input capacitance implemented by a bank of three different capacitors allowing to adjust the input capacitance $C_{IN}$, which mimics the pixel sensor capacitance, in the range from 0 to 175 fF. This choice has been based upon measurements of the pixel capacitance performed with the PixCap chip (see Chapter 3). The CSA has a feedback current adjustable by a 4-bit Feedback DAC (FDAC). The CSA is followed by a discriminator with a threshold adjustable individually in each pixel by a 5-bit Threshold DAC (TDAC). The digital part of the pixel contains a...
15-bit configuration register and a 8-bit hit counter.

Two architectures of the CSA were implemented in the FE-T65-1: CSA with continuous reset and CSA with switched reset. Their schematics are shown in Figure 5.12. These two architectures differ by the feedback loop. The continuous CSA has a continuous current source connected in the feedback loop, establishing a linear discharge of the CSA in case of charge injection. The switched CSA has also a current source in the feedback loop, which is controlled by a switch. This switch is periodically switched on and off to reset the CSA with a high current. This solution has an advantage with respect to the CSA implemented in the FE-T65-0. This “soft” reset does not cause oscillations of the CSA as was observed in the FE-T65-0.

Each concept of the CSA has certain advantages and disadvantages. The continuous CSA has a linear discharge curve allowing to measure the signal amplitude by Time over Threshold (ToT). The discharge time can reach several hundreds of nanoseconds. The switched CSA allows to discharge the CSA within 10 ns. On the other hand, the signal amplitude from the switched CSA can not be easily measured by ToT.

A response of two different types of the CSA (continuous and switched), captured on an oscilloscope, is shown in Figure 5.13. A signal return to the baseline of the CSA with continuous reset is 360 ns at 20 ke⁻, while in case of the switched CSA it is about 10 ns. However, the fast reset of the switched CSA
introduces a significant undershot and a subsequent recovery time.

Two different discriminators have been implemented in the FE-T65-1: continuous and dynamic. The design of the continuous discriminator is of the same architecture as in the FE-T65-0. The design of the dynamic discriminator in the FE-T65-1 has been reworked with respect to the previous version of the test-chip FE-T65-0. A schematic of the dynamic discriminator is shown in Figure 5.14.

The discriminator has two stages. Each stage contains only three transistors in each current branch, which improves the discriminator performance at small a power supply voltage (1.2 V). The design of the dynamic discriminator has been optimized to low power consumption and low input voltage offset. These quantities are not independent. In order to achieve small offset, dimensions of the transistors must be large. Power consumption of the dynamic discriminator is determined by the parasitic capacitances of the transistors, which scale with the transistor dimensions. The result of the optimization is voltage
offset of 4.5 mV and power consumption of 3.8 µW at 40 MHz switching frequency.

### 5.3.1 Noise

Noise levels of each individual FE variant have been determined by the threshold scans in a similar way as in the case of FE-T65-0. As shown in Chapter 3, noise of the CSA depends on the input capacitance and bias setting of the CSA. To explore these dependencies, ENC has been evaluated as a function of bias current of the CSA $I_{\text{BIAS}}$ and input capacitance $C_{\text{IN}}$. The injected charge was constant (2 ke$^-$). These noise maps of each FE variant are shown in Figure 5.15 (a-d). The measurement results show, that the noise grows with the input capacitance and decreases with the bias current. Mean noise levels (averaged over all pixels of each particular FE variant) of all FE variants are summarized in Table 5.3. The noise levels have been measured with a constant input capacitance of 75 fF and switching frequency of 40 MHz (switched FEs). The capacitance of 75 fF has been chosen as an estimate of the pixel capacitance of a silicon planar sensor with pixel dimensions of 180×25 µm$^2$.

![Figure 5.15: The noise levels of FE-1 - FE-4 are shown in Figures a-d. Noise increases with the input capacitance and decreases with the CSA bias current.](image)
Chapter 5 Pixel front-end development in 65 nm CMOS technology

<table>
<thead>
<tr>
<th>FE - variant</th>
<th>〈ENC〉 [e⁻]</th>
<th>P [µW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>144</td>
<td>10.4</td>
</tr>
<tr>
<td>2</td>
<td>183</td>
<td>10.6</td>
</tr>
<tr>
<td>3</td>
<td>113</td>
<td>14.6</td>
</tr>
<tr>
<td>4</td>
<td>157</td>
<td>14.8</td>
</tr>
</tbody>
</table>

Table 5.3: Mean noise and power consumption of all variants the analog pixel electronics implemented in the FE-T65-1.

The analog FEs equipped with the dynamic discriminator systematically have higher noise. This effect is visible in Figure 5.16 (a, b). A possible cause of the excessive noise was studied in detail by the design simulation. It was shown, that the switching of the dynamic discriminator causes large current spikes (50 µA) and voltage drops (3 mV) on the supply lines. In addition, the switching of the dynamic discriminator partially couples to the signal from the CSA. These parasitic effects are also present in the FEs with continuous discriminator, but with about 50 times smaller amplitude. This additional digital activity can be responsible for the excessive noise observed at the FEs with dynamic discriminator.

By comparing the noise performance of the CSA architectures it was shown, that the switched CSA has lower noise than the continuous CSA. This difference can be explained by different transistor dimensions of the continuous and switched CSA and also by different bias conditions. In addition, the absence of the continuous current source in the feedback loop of the switched CSA is in favor of the lower noise of the switched CSA.

![Figure 5.16: A comparison of the noise dependence on the input capacitance of the continuous CSA (a) and the switched CSA (b) with both types of discriminator. The noise scales almost linearly in all FE variants. However, the FEs equipped with the dynamic discriminator (FE-2 and FE-4) have systematically higher noise levels.](image)

5.3.2 Dynamic performance

The dynamic performance of the analog FEs was determined in terms of timewalk. The timewalk is a charge dependent delay between the charge injection and receiving the hit at the output of the discrimin-
ator. The absolute value of the delay is not a major concern for tracking at LHC experiments. However, if the time difference between receiving a "small" hit and a "large" hit is longer than the period between the bunch crossings (25 ns), then the small hit is assigned to the wrong bunch crossing. Therefore, it is desirable that the timewalk does not exceed 25 ns. Two sources of timewalk can be identified: CSA and discriminator. Figure 5.17 shows the timewalk of variant FE-1. The timewalk significantly depends on the bias settings of the CSA and the discriminator. By increasing the bias current of the CSA, the discriminator increases its speed and decreases the timewalk. To keep the timewalk below 25 ns, this FE variant consumes the power of 18 µW. The variant FE-2 has a dynamic discriminator. Short relaxation time of the dynamic discriminator allows to bias the CSA with a small current to reduce the timewalk below 25 ns. A total power consumption of this variant is as low as 10.6 µW. The variants with the switched CSA (FE-3 and FE-4) work at the switching frequency of 40 MHz (bunch crossing at LHC). Within 25 ns, the CSA collects the signal charge and adjusts the output voltage level, which is then sampled by the discriminator and then the CSA is reset. The FE chain with the switched CSA consumes more power (14.7 µW). Regardless of which kind of discriminator is used, the timewalk of variants FE-3 and FE-4 does not exceed 25 ns.

![Figure 5.17: The timewalk measured with the FE variant FE-1 with two different bias currents of the CSA.](image)

Even though the same bias current is provided to both types of the CSA, their dynamic performance is different. The core amplifiers and source followers have an identical schematic, but they differ in the transistor dimensions. The input transistor of the source follower of the continuous CSA has dimensions $W/L=18/0.12 \, \mu m$, while the transistor of the switched amplifier has dimensions $W/L=4/0.12 \, \mu m$. This difference introduces a different capacitive load $C_{out}$ of the core amplifier and thus a different dynamic performance. This difference is clearly visible when comparing the rise-time of both CSA types (see Figure 5.18 (a, b)). The rise-time of the continuous CSA is longer by a factor of 2 (default bias setting) than in the case of switched CSA and is strongly dependent on the bias current.

### 5.3.3 Threshold dispersion

A large pixel chip often contains thousands (or even tens of thousands) of pixels integrated in an area of several cm$^2$. The parameters of the pixel electronics are not perfectly uniform across the entire pixel
Figure 5.18: The rise-time of the continuous CSA (a) strongly depends on the bias current. The rise-time of the switched CSA (b) is shorter by approximately a factor of 2 (default bias setting) compared to the continuous CSA (time-scale in Figure (a) is 10 ns/div and in Figure (b) is 4 ns/div.

FE chip. Due to variations of the fabrication process, the transistors are subjects of variations of their dimensions, doping profiles and consequently their electric parameters. In the FE electronics for the hybrid pixel detectors, these variations manifest themselves (among the others) by variation of the detection threshold. This threshold dispersion has been measured with the FE-T65-1 and compensated with an in-pixel 5-bit TDAC. This TDAC is based on a resistive TDAC implemented in a source follower. The threshold dispersion of all FE variants is summarized in Table 5.4. The threshold dispersion was measured with 8 pixels of each FE variant, hence covering only a small statistical sample. This analysis does not fully cover the process variations appearing on a cm$^2$ scale pixel chip, but it covers the effects arising from the mismatch of the transistor dimensions.

<table>
<thead>
<tr>
<th>Variant</th>
<th>CSA</th>
<th>Comparator</th>
<th>Disp. before tuning [e$^{-}$]</th>
<th>Disp. after tuning [e$^{-}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE-1</td>
<td>Continuous</td>
<td>Continuous</td>
<td>267</td>
<td>22</td>
</tr>
<tr>
<td>FE-2</td>
<td>Continuous</td>
<td>Dynamic</td>
<td>405</td>
<td>28</td>
</tr>
<tr>
<td>FE-3</td>
<td>Switched</td>
<td>Continuous</td>
<td>272</td>
<td>20</td>
</tr>
<tr>
<td>FE-4</td>
<td>Switched</td>
<td>Dynamic</td>
<td>298</td>
<td>21</td>
</tr>
</tbody>
</table>

Table 5.4: Threshold dispersion before and after threshold tuning of the four pixel variants in the FE-T65-1.

The threshold dispersion of the FE variants containing the dynamic discriminator is slightly higher than in the case of the continuous discriminator. However, after threshold tuning, the dispersion is less than 30 e$^{-}$, which is much less than the noise level and therefore insignificant. In a larger chip, we expect that the threshold dispersion might be larger due to a larger impact of dispersion of the parameters of the fabrication process.
5.3.4 Crosstalk

The ultra deep submicron technologies allow to achieve a large integration density of the transistors and the metallic interconnections. Spacing between the metal routes can be as small as 100 nm. This feature raises the danger of crosstalk. An unwanted crosstalk was observed directly inside the pixel between the charge injection line (INJECT line) and the metallic capacitors ($C_{IN}$). The proximity of the metal line unintentionally increased the value of the injection capacitor and thus the value of the injected charge. Calibration based on the post layout simulation was made to correct the values of the injection signal charge. A screenshot of the INJECT line and the capacitors is shown in Figure 5.19. The effect of the calibration is shown in Figure 5.20 (a, b).

![Figure 5.19: The INJECT line capacitively couples to the bank of the input capacitors, thus varying the charge injected into the CSA.](image1)

![Figure 5.20: Peak voltage at the output of the CSA as a function of the input capacitance. The parasitic coupling of the INJECT line to the input capacitors changes the value of the injected charge, depending on which input capacitors are switched on (a). This effect disappears after the calibration performed with the simulation data (b).](image2)
Chapter 5  Pixel front-end development in 65 nm CMOS technology

The parasitic capacitance of the injection line increased the injection capacitor in the worst case by 38%. In future designs, more attention has to be paid to the shielding of the sensitive CSA input node from all dynamic lines.

5.3.5 Comparison of FE-T65-1 with FE-I4

FE-I4 is probably the most advanced FE chip developed for HEP applications to date. Comparing the performance of FE-T65-1 with FE-I4 is therefore desirable in terms of revealing the advantages and disadvantages of the 65 nm technology. The most important analog parameters of both chips are summarized in Table 5.5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FE-I4</th>
<th>FE-T65-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>130 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>250×50 µm²</td>
<td>180×25 µm²</td>
</tr>
<tr>
<td>Analog part</td>
<td>156×50 µm²</td>
<td>59×25 µm²</td>
</tr>
<tr>
<td>CSA</td>
<td>2 stages</td>
<td>1 stage</td>
</tr>
<tr>
<td>Noise</td>
<td>113-183 e⁻</td>
<td>100-170 e⁻</td>
</tr>
<tr>
<td>Analog supply voltage</td>
<td>1.5 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>12.6 + 5.4 + 3.9 = 21.9 µW(1)</td>
<td>7 + 3.6 µW(2)</td>
</tr>
<tr>
<td>Analog power density</td>
<td>1.75 mW/mm²(3)</td>
<td>2.36 mW/mm²(4)</td>
</tr>
</tbody>
</table>

Table 5.5: Comparison of the analog parameters of FE-I4 and FE-T65-1.

(1) sum of the power contribution of the first stage CSA, the second stage CSA and the discriminator
(2) is sum of the power contribution of the CSA and the discriminator
(3) default setting
(4) pixel variant FE-2

The analog FE electronics in the FE-T65-1 occupies an area more than 5-times smaller than in the FE-I4. A compression of the silicon area of the analog electronics was possible partially due to the reduction of transistor sizes and by simplification of the electronic circuitry (i.e. using a single stage CSA instead of the dual stage CSA). The analog performance in terms of noise, speed and linearity are comparable with the FE-I4. However, the analog power density of the FE-T65-1 is in the best case higher by 35% than in the case of FE-I4.

5.4 Summary of the pixel FE development in the 65 nm CMOS technology

Two prototype chips have been designed in the 65 nm CMOS technology: FE-T65-0 and FE-T65-1. Several variants of the analog pixel FEs have been integrated in the chips and tested. The FE-T65-0 has proven the applicability of the 65 nm technology for the design of the CSA. The gain and linearity of the CSA are in good correspondence with the simulated values. The FE channels equipped with a continuous discriminator were able to perform a threshold scan and determine the level of noise. The noise level of these FE channels was about 80 e⁻. Several issues have been identified with FE-T65-0, in particular with the dynamic discriminators. Their offset was found to be very high (> 100 mV),
5.4 Summary of the pixel FE development in the 65 nm CMOS technology

due to the mismatch of the transistors. Another issue was found with the CSA. The CSA tends to be unstable during the reset phase, when the feedback capacitor was reset by a switch. These issues have been a motivation for designing a new, more complex, test chip FE-T65-1. The FE-T65-1 is a pixel array of 32 pixels containing a full analog FE (CSA, discriminator and DACs for tuning the feedback current and the threshold level, hit counter and configuration logic). This design fixes all issues of its predecessor FE-T65-0 and in addition, allows to measure noise levels with a connected input capacitance. Continuous and switched CSAs have been integrated in the pixel matrix, followed by either a continuous or a dynamic discriminator. The switched CSA has a modified switching feedback circuit (compared to FE-T65-0) allowing "soft switching" thus avoiding oscillations of the amplifier during the reset phase. A different concept (compared to FE-T65-0) of the dynamic discriminator has been chosen and the design has been optimized for a low offset. Each of the four pixel versions was proven to be fully working and their analog performance differs from version to version. The measurements with the FE-T65-1 has shown, that the noise levels scale approximately linearly with the sensor capacitance. Pixel FEs equipped with the dynamic discriminator show a larger noise. This effect can be caused by fast switching of the discriminator and coupling of digital voltage spikes to the sensitive analog part. The excessive noise can be reduced by a more effective decoupling of the power lines of the discriminator and by reducing the speed of the discriminator (a prolonged relaxation time of the latch). The dynamic discriminator has been proven to significantly reduce the power consumption in combination with the continuous CSA. The dynamic discriminator contributes significantly less to the timewalk of a pixel FE than the continuous discriminator. The dispersion of the pixel parameters like noise, gain and threshold was found to be relatively low. The threshold dispersion after tuning was below 30 e−. The power consumption of the pixel FEs spans from 10.6 µW up to 18 µW, in all cases introducing a higher analog power density than the FE-I4. The reduction of the power density of the analog FEs is difficult and has to be further studied. Another critical point is crosstalk, which has been observed in the FE-T65-1. Shielding of the sensitive node of the CSA is therefore critical to increase the crosstalk immunity of the pixels.

FE-T65-0 and FE-T65-1 have proven that in the 65 nm technology an analog FE with parameters compatible with the 130 nm technology can be designed and that the 65 nm technology is from the analog point of view suitable for the design of a large pixel FE chip (with certain precautions).

The results have been published [70].
Chapter 6
Depleted Monolithic Active Pixel Sensors

6.1 A new concept of the Monolithic Active Pixel Sensors

In Chapter 4, several concepts of the Monolithic Active Pixel Sensors (MAPS) have been introduced. Each of them has certain limitations in terms of the signal amplitude, possibility to integrate only one type of transistors (either NMOS or PMOS), or a very slow and incomplete charge collection by diffusion. In this chapter, we introduce a novel concept of Depleted MAPS (DMAPS), based on a high resistive silicon substrate, biased with a high voltage, with the possibility to integrate both transistor types. A high resistivity silicon bulk can be depleted to a substantially higher depth than a standard low ohmic silicon used in the standard CMOS process. In the ideal case, the entire silicon substrate can be depleted.

A fully depleted sensor has several benefits compared to the sensor relying on charge collection by diffusion (MAPS on epitaxial layer). The charge collection in the depleted sensor is fast (typically below 10 ns). Since no free charge carriers are present in the depleted bulk, the entire signal charge, generated in the silicon bulk, is collected without any significant loss due to the recombination of the charge carriers. The difference between the charge collection mechanisms in the conventional and depleted MAPS sensors is illustrated in Figure 6.1.

![Figure 6.1: Charge collection in a conventional MAPS sensor (a) is disordered and incomplete due to a slow diffusion process. A fully depleted MAPS sensor (b) extracts the charge carriers by a directed drift field. Charge collection is fast and efficient.](image)

The charge collection efficiency of the conventional MAPS sensors is sensitive to the number of defects in the silicon crystal lattice. The crystal defects and the charge traps can significantly limit the
sensor performance. The traps are frequently generated as a consequence of irradiation. In the presence of a directed drift field, the silicon bulk quickly extracts the charge carriers. In contrast, the charge carriers in the conventional MAPS have to perform a random walk to reach the charge collection electrode, thus having a higher probability to be trapped or to recombine. The DMAPS sensors are thus potentially radiation harder.

6.2 Technology for fabrication of DMAPS sensors

A standard CMOS technology can not be used to fabricate DMAPS sensors. The fabrication process has to use high resistivity silicon wafers. A special CMOS process, suitable for fabrication of the DMAPS sensors was identified [71]. It is a commercial 150 nm CMOS process, specially developed for the fabrication of CMOS image sensors. In this process, the integrated circuits are processed on the 8” wafers, with the possibility of wafer thinning. The backside processing is possible in this technology, which is an important feature for making the backside contact of the sensor. Up to six metal layers can be used for interconnections. The power supply voltage for the standard MOSFET transistors is 1.8 V and for high voltage transistors up to 12 V. Complex electronics based on a high density 150 nm technology as well as high voltage electronic components can be integrated in the same chip. A quadruple well is used to shield the sensor part from the electronic part.

This technology represents a perfect starting point for the development of a sensor, which can be potentially fully depleted, and complex electronics can be integrated in the pixels. In order to explore the potential of this technology, a test chip EPCB01 has been designed and tested.

6.3 Test chip EPCB01

The EPCB01 is a demonstrator chip designed to prove the functionality of the concept of DMAPS sensors. Several pixel arrays and test structures were integrated in the chip. The chip itself was fabricated on a high resistivity n-type silicon wafer, which was thinned down to a thickness of 50 µm. A structure of the proposed DMAPS sensor with typical bias potentials is illustrated in Figure 6.2. A deep p-well is implanted in the high resistivity n-type substrate and forms a thin p-type substrate for integration of the CMOS electronics. An additional deep n-well resides inside the p-substrate and hosts NMOS and PMOS transistors. The transistors are decoupled from the p-substrate by the deep n-well.

The sensitive elements are implemented by n-wells implanted in the high resistivity n-type substrate. The n-wells operate as charge collection electrodes for electrons. In a standard bias configuration, the n-wells are connected to a high positive voltage, while the p-substrate and the backplane are connected to a zero or slightly negative voltage. The depletion region is formed around the PN junctions, formed at the backplane-bulk and p-substrate-bulk boundaries. Although these collection n-wells do not form PN junctions, they create regions with a high electric potential and thus build up an electric drift field in the depleted bulk. At a sufficient bias voltage, the sensitive high resistivity bulk is depleted. The full depletion voltage is an unknown parameter and has to be determined by measurement.
Assuming a fully depleted 50 µm silicon bulk, this sensor type can in theory collect a signal of 4000 electrons per MIP (Minimum Ionizing Particle). It is at least four times more than the currently best MAPS or HV-MAPS. Advantages of the DMAPS sensor are:

- Large signal of ≈ 4000 electrons per MIP
- Fast signal collection by drift
- Small estimated pixel capacitance and potentially small noise
- Thin silicon substrate introducing low material budget for a tracking detector

A layout of the EPCB01 test chip is shown in Figure 6.3. The chip dimensions are 1.4×1.4 mm² and the silicon area of the chip is almost fully used. The dominant part of the core of the chip is occupied by six DMAPS pixel arrays. There is also an experimental array of small pixels with small pixel pitch (10×10 µm²) called "Tiny Pixels" and an array of the MOSFET transistors of various dimensions. These transistors are meant to be used for evaluation of the radiation hardness of this technology.

The DMAPS pixels integrate a high resistivity high voltage sensor part, analog FE electronics and digital electronics. The pixel size is 40×40 µm². The charge collection electrode occupies approximately 25% of the total pixel area. The complexity of the pixel electronics is about 160-180 transistors (depending on the variant). A micrograph of the EPCB01 and a layout of one DMAPS pixel is shown in Figure 6.4.

The analog pixel electronics adopts a similar scheme as is often used in hybrid pixel detectors. Signal from the charge collection electrodes is amplified by a CSA and further processed by a discriminator. Two architectures of the analog FE were implemented: (time) continuous and switched.

The continuous FE architecture uses a CSA with a constant current source in the feedback loop, followed by a continuous discriminator (continuous and dynamic discriminator are introduced in Chapter 5).
Figure 6.3: Layout of the EPCB01 test chip implementing the DMAPS pixel sensors.

This architecture operates asynchronously (hit appears immediately within the "analog speed" of the FE) at the output of the comparator as the signal is collected from the sensor. The switched FE architecture is based on a CSA with switched reset and clamp-and-sample circuit followed by a dynamic discriminator. Three additional clock lines are needed to control the switched analog FE. The information about a hit comes out of this FE architecture after an exactly defined sequence of pulses on the three clock lines (the FE operates synchronously). The clock lines for the switched FE are: RESET, CLAMP and SAMPLE. The RESET line controls the switch in the CSA feedback, the CLAMP line controls the clamp switch and the SAMPLE line controls the dynamic discriminator. The concept of clamp and sample is often used in the FE electronics processing the signal from image sensors. In each switching cycle, the DC baseline at the input of the discriminator is restored to a well defined potential (VCLAMP). In theory, this circuit suppresses the low frequency noise component coming from the CSA. Sometimes, this technique is called Correlated Double Sampling (CDS) [72]. A true CDS uses an additional sample and hold circuit, which is not implemented in the EPCB01. Therefore, we call the technique implemented in the EPCB01 clamp and sample. The switched analog FE operates with the frequency of 1 MHz.

One pixel of each pixel array (except V4) has the output of the CSA connected to an IO pad (through a source follower buffering the signal) for debugging purposes.

The digital part of the DMAPS pixel provides configuration of the analog part and allows readout of the chip. Each pixel contains six latches and one D flip-flop. The latches store 6 bits of configuration data (4 bits for threshold tuning, one bit to enable charge injection and one bit to enable hitOr function). The flip-flop operates in two modes. In the first mode, it registers a hit in the pixel. In the second mode, the flip-flop is daisy-chained to the adjacent pixels, forming a shift register. This shift register is used either for chip configuration or for the read-out.

Each of the pixel domains (sensor, analog FE, digital logic) can be implemented in many possible
The number of potentially attractive options grows fast. As a compromise, 6 variants of the DMAPS pixels were implemented in six pixel arrays called V1 - V6. They differ by geometry of the collection electrodes, their biasing and by the architecture of the analog FE electronics. These pixel arrays are categorized in Table 6.1 and the corresponding schematics are shown in Figure 6.5.

<table>
<thead>
<tr>
<th>Pixel variant</th>
<th>Biasing</th>
<th>Coupling</th>
<th>FE architecture</th>
<th>Matrix dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>resistor</td>
<td>AC</td>
<td>continuous</td>
<td>8 x 8</td>
</tr>
<tr>
<td>V2</td>
<td>diode</td>
<td>AC</td>
<td>continuous</td>
<td>8 x 8</td>
</tr>
<tr>
<td>V3</td>
<td>CSA feedback</td>
<td>DC</td>
<td>continuous</td>
<td>6 x 8</td>
</tr>
<tr>
<td>V4</td>
<td>switched</td>
<td>DC</td>
<td>switched</td>
<td>6 x 8</td>
</tr>
<tr>
<td>V5</td>
<td>diode</td>
<td>AC</td>
<td>switched</td>
<td>8 x 8</td>
</tr>
<tr>
<td>V6</td>
<td>resistor</td>
<td>AC</td>
<td>switched</td>
<td>8 x 8</td>
</tr>
</tbody>
</table>

Table 6.1: Different variants of the DMAPS pixels implemented in the EPCB01.

The coupling of the high-voltage sensitive nodes and the low voltage CMOS FE electronics require the use of a capacitive AC coupling of the collection electrodes to the FE electronics, in order to prevent breaking of a thin gate oxide in the deep submicron CMOS devices. The AC coupled variants of the DMAPS pixels (V1, V2, V5 and V6) can be biased in two different ways: resistor biasing and diode biasing. A schematic of the resistor biased and the diode biased variant are shown in Figure 6.5 (a, b, e, f). The biasing resistor is integrated directly in each DMAPS pixel, wound around the charge collection electrode. The resistor is implemented by a polysilicon resistor with a resistance of 5 MΩ. The diode biased variants use a forward biased diode. Since the current of the biasing diode is very small (given by the leakage current of the charge collection electrodes), the diode internal resistance is very high (>10 MΩ). The biasing diode is integrated directly in the charge collection electrode and does not consume any additional silicon area.
The charge collection electrodes can also be DC coupled to the FE electronics. In this case, the sensitive electrode can only be biased by a low voltage between 0-1.8 V. The biasing of the DC coupled collection electrode can either be established by the feedback of the CSA (variant V3, see Figure 6.5 (c)), or pulsed by a well defined voltage (variant V4, see Figure 6.5 (d)). Low bias voltage of the charge collection electrodes is not necessarily a limiting factor in terms of sensor depletion. The sensor backplane and the p-substrate can be biased by a negative voltage without affecting the power supply voltage domains of the CMOS electronics. Such a biasing configuration is described in Figure 6.6. All PN junctions in this biasing configuration are reversely biased and conduct only a thermally generated leakage current.

### 6.4 Characterization of EPCB01

As we described in the previous sections, the chip has many biasing nodes of the multiple wells. At the same time, the technology is very non-standard and testing requires a careful approach. Initial measurements of the EPCB01 were oriented on the monitoring of the power supply currents of the sensitive elements and the electronics of the chip. The second step was verification of configurability of the chip, which was performed by transmitting known data patterns to the configuration register and capturing the data at the output. These initial tests were executed with four chip samples and all of them were successful. No excessive currents were observed and all chips were fully configurable. This result indicates a potentially high yield of this technology. Figure 6.7 shows a response of the DMAPS pixels to the β and γ radiation from $^{90}\text{Sr}$ and $^{55}\text{Fe}$ radioactive sources. This indicates, that both charge collection and electronic parts of the chip are alive.
6.4 Characterization of EPCB01

Figure 6.6: An example of the biasing configuration of the DMAPS sensor with reduced bias voltage of the collection electrode. Keeping the surrounding p-substrate and the backplane at a negative potential, the sensor bulk can be fully depleted, while the potential of the sensitive electrode is at the level, which is low enough to be directly connected (DC coupling) to the FE electronics.

Figure 6.7: Initial testing of the EPCB01. The configuration data pass the configuration register unchanged (a). A response of the DMAPS pixels to the radioactive sources $^{90}\text{Sr}$ (b) and $^{55}\text{Fe}$ (c) was observed at the analog outputs of the chip by an oscilloscope.

The EPCB01 was further characterized quantitatively in terms of gain, noise, threshold dispersion, cluster size and radiation hardness.

6.4.1 Gain determination with external charge injection

Gain of the DMAPS pixels was evaluated as a peak voltage amplitude at the output of the CSA divided by the injected charge. In this measurement, the charge was injected via an injection capacitor with the capacitance of 2 fF. The majority of the pixels have only a binary readout. The information about the peak voltage at the output of the CSAs was determined by multiple charge injections and threshold scans. The gain of all pixels of each pixel array, except V4 (this variant does not have the injection capacitor), was determined by this procedure and evaluated as a function of the injected charge. The charge collection electrodes were biased with a voltage of 11 V, keeping the sensor depleted. The backplane
and the p-substrate were biased with a slightly negative voltage of -1.5 V. These "gain curves" for each variant of the pixel array are shown in Figure 6.8. The error bars represent the standard deviation of the gain of all pixels in the particular pixel array. The error bars were scaled down by a factor of 2 to keep the graph readable.

The highest mean gain of 99.8 µV/e\(^-\) (measured with 1 ke\(^-\) injection) was achieved with the variant V2. The standard deviation of gain of the CSA (determined by threshold scan) in this 64-pixel array is 19.1 µV/e\(^-\). A comparison of the gain curves of the arrays V1 and V2 is particularly interesting. The pixels in these arrays have identical electronics (layout included). They differ only by the sensor biasing and the geometry of the sensitive elements. Both pixel versions are AC coupled and the FE electronics is not influenced by the sensor leakage current. Nevertheless, the pixel variant V1 has lower gain than V2. The gain curves of V1 and V2 are equidistant, but shifted by 20.5 µV/e\(^-\) on average. This effect can be explained by the different capacitance of the charge collection electrodes and the associated biasing circuit. The shape of the collection electrode used in variant V2 (and V5) is shown in Figure 6.9. The exact layout of the collection electrode used with the other variants of the DMAPS pixels was provided by the foundry and is not available to the designers. However, if the design uses a broader collection n-well or n\(^+\) region, it will cause the higher capacitance. Another capacitance contribution might come from the biasing resistor.

The gain of an ideal CSA is independent of the sensor capacitance. In the case of the DMAPS pixels, the core amplifier is implemented with a common source stage with an open loop gain of 76 in all pixel variants. The small open loop gain introduces a strong gain dependence on the sensor capacitance (see Equation 2.17).

The gain curve of V3 is shifted with respect to V2 even more than V1. This effect can be caused by the fact, that the collection electrode of V3 is biased by a low voltage of approximately 370 mV.
6.4 Characterization of EPCB01

Figure 6.9: A schematic cross section of the collection electrode used in the DMAPS variants V2 and V5.

provided by the feedback of the CSA. The sensor is not depleted, causing the capacitance to be even larger.

The shift of the gain curves of the continuous variants of the DMAPS pixels was confirmed by measurements performed with the switched variants (V5 and V6). At the beginning of their dynamic range, the gain shift is the same as in the case of the continuous variants (V1 and V2). However, non-linear character of the switched variants is different with respect to the continuous variants. The gain curves of V5 and V6 are not equidistant and the reason for this behavior is not yet clear.

6.4.2 Noise performance

The noise level of the DMAPS pixels was determined by the threshold scan and evaluated in terms of ENC as a function of the injected charge. The noise performance of all measured pixel arrays is shown in Figure 6.10.

Each variant of the DMAPS pixels has a different noise level. The differences of the noise curves directly reflect the differences of gain of these pixel variants. The lowest noise of 30 e\(^{-}\) was measured with the DMAPS pixel variant V2. A higher noise of the pixel variants V1 and V3 can be attributed to the higher sensor capacitance. The highest noise was measured with the pixel variants V6 and V5 (at the end of the dynamic range). The excessive noise of the switched FE variants might be caused by the dynamic discriminator. At the moment of "activating" the discriminator (rising edge of CLK signal) a large voltage change (in this case from 0 V to 1.8 V) occurs at the drains of the input transistors in very short time (100s ps). This voltage change couples capacitively through a parasitic capacitance \(C_{gd}\) (see Figure 6.11) of the input transistor M1 back to the CSA and disturbs the signal of the CSA. This parasitic charge injection is abrupt and occurs in short time when the discriminator departs from the metastable state and is sensitive to small perturbations of the signal coming from the CSA leading to an excessive noise commonly called the kick-back noise (see [73], [74]).

A significant component of noise represents a Random Telegraph Signal noise (RTS) [75]. The RTS noise is caused by trapping and releasing the charge carriers moving near Si-SiO\(_2\) boundary in a similar way as in the case of 1/f noise. However, in deep submicron electronics the physical size of the trap can affects an area as large as 1 \(\mu\)m\(^2\) and might affect the entire area of the MOSFET channel.
In this case, the drain current of the MOSFET transistor switches between two discrete levels [75]. The RTS noise was visually observed by the oscilloscope at the analog outputs of all pixel variants in EPCB01 (except V4, which does not have an analog output). The RTS noise, superimposed on the signal, is shown in Figure 6.12.
6.4 Characterization of EPCB01

The RTS noise is not special only to EPCB01. This noise component often appears in monolithic pixels as described for example in [76], [77] or in the CCD image sensors [72]. In the MAPS sensors, small (deep submicron) transistors are favoured to be used in the FE electronics due to their small input capacitance and thus high gain. However, by decreasing the transistor size, the FE electronics is more vulnerable to RTS.

6.4.3 Threshold dispersion

A dispersion of the detection threshold was evaluated in the same way as in the FE-T65-1 prototype chip (see Chapter 5). Each DMAPS pixel has a 4-bit DAC (TDAC) for equalization of the detection threshold (threshold tuning). An implementation of the TDAC is different in the continuous pixel variants (V1-V3) and switched variants (V4-V6).

The continuous variants use a resistive TDAC embedded in a source follower as shown in Figure 6.13 (a). The advantage of this solution is the possibility to adjust the threshold tuning range (if needed) with the $V_{\text{bias}}$ voltage. However, the source follower is imperfect and the output voltage of the TDAC is a non-linear function of the input threshold voltage. The resistor array is arranged in a common centroid layout and consumes a substantial area of the analog part of the pixel. In addition, the TDAC consumes an additional power.

The switched variants use a two stage dynamic discriminator. The input voltage offset of the dynamic discriminator is very sensitive to the capacitance of the routing. This fact was used in the design of switched capacitors TDAC as shown in Figure 6.13 (b). By adjusting the capacitance between the two branches of the discriminator, the voltage offset (discriminating threshold) can be adjusted. This TDAC does not introduce non-linearity to the threshold setting. In addition, this TDAC is very compact in the pixel layout and does not increase the power budget of the pixel.

Both variants of the TDAC significantly reduce the threshold dispersion. Dispersion of the threshold was evaluated at the mean threshold of 1 keV. In the DMAPS variant V2, the initial threshold dispersion was 248.8 e$^{-}$ and after threshold tuning the dispersion decreased to 134.5 e$^{-}$. In the case of switched variant V5, the threshold dispersion was reduced from initial 297.2 e$^{-}$ down to 78.2 e$^{-}$. The corresponding threshold distributions of the DMAPS pixel arrays V2 and V5 are shown in Figure 6.14 and Figure 6.15.
Chapter 6 Depleted Monolithic Active Pixel Sensors

Figure 6.13: Two different variants of a discriminator with TDAC were implemented in the EPCB01. A continuous discriminator with resistive TDAC (a) and a dynamic discriminator with switched capacitors TDAC (b).

Figure 6.14: Threshold dispersion of DMAPS pixels of the variant V2 before (a) and after threshold tuning (b).

Figure 6.15: Threshold dispersion of DMAPS pixels of the variant V5 before (a) and after threshold tuning (b).
6.4 Characterization of EPCB01

6.4.4 Cluster size measurement

In a fine-pitch pixel sensor, the signal charge originating from an ionizing particle diffuses on its path to the collection electrodes. The signal charge is often collected by a cluster of neighboring pixels, the size of which depends on the depleted thickness of the sensor and on the pixel size. The cluster size at the DMAPS pixels was measured with a radioactive source $^{90}$Sr. Typical events recorded by the EPCB01 are shown in Figure 6.16.

![Figure 6.16: Various shapes of events recorded with the EPCB01 irradiated with $\beta$ radiation originating from the radioactive source $^{90}$Sr.](image)

A data selection was performed prior to the cluster analysis. The clusters, whose parts lie at the edge of the pixel matrix or closely surround a hot pixel, were rejected from the analysis. The analysis of the cluster size was conducted with the pixel array V2 at several sensor bias voltages (HV_BIAS) connected to the charge collection electrodes. The detection threshold was adjusted to 1 ke$^{-}$ and was equalized over the matrix. The distributions of the cluster size measured at bias voltages of 2 V and 11 V are shown in Figure 6.17 (a, b).

By comparing these distributions, we can see that at 2 V bias voltage, 29% less events are recorded than with a bias voltage of 11 V. The events from $^{90}$Sr are predominantly single pixel clusters. However, double pixel clusters become more pronounced at 11 V than at 2 V. This effect can be explained by the fact that at a higher bias voltage, a larger sensor volume is depleted and the total charge spreading by diffusion becomes larger. In addition, more charge is collected. This results in a larger cluster size.

The total number of events (frames with at least one hit) as a function of the bias voltage is shown in Figure 6.18 (a). The sensor starts working at 2 V bias voltage. At 3 V and beyond, the number of detected hits does not increase. It means, that at 3 V a pixel collects more than 1 ke$^{-}$ from a majority of electrons emitted by $^{90}$Sr. Maximum cluster size is 8 pixels. However, large clusters (3 and more pixels) are caused by multiply scattered electrons in the sensor and their number is negligible with respect to the single and double pixel clusters. The double pixel clusters are caused by a charge diffusion between pixels. The ratio of single pixel clusters to double pixel clusters carries information about the depletion of the sensor and the charge collection efficiency. The ratio of single to double pixel clusters as a function of the bias voltage (HV_BIAS) is shown in Figure 6.18. This ratio decreases with increasing
sensor bias voltage and saturates at a voltage of about 6 V, while the event rate does not increase beyond this point. This result implies that at a voltage of 6 V and above, the sensor does not collect any more charge and the cluster size ratio remains constant. Saturation of the cluster size is a direct indication of full depletion of the sensor.

6.4.5 Gain determination using an $^{55}$Fe - radioactive source

The response of an ideal detector does not depend on whether the signal comes from an external charge injection circuit or from the collection electrode. To verify this assumption, the gain of the FE electronics was measured independently using a $^{55}$Fe radioactive source. This source emits gamma rays with a characteristic peak in the energy spectrum at 5.9 keV, which translates into a signal of 1640 electrons.

The DMAPS pixels can detect only particles which generate signal higher than threshold. Each pixel holds binary information about the hit (either hit is detected or not). This binary resolution of the signal
measurement does not allow to measure the energy of photons on event by event basis. The energy spectrum of $^{55}$Fe was determined by measuring the number of hits in the pixel with a successive increase of the detection threshold. By performing a derivative of this hit count with respect to the threshold voltage, the spectrum of $^{55}$Fe was obtained at each pixel. From the position of the dominant energy peak of $^{55}$Fe, the gain of the DMAPS pixels was determined and compared with the gain determined with an external charge injection of 1640 electrons. This analysis was performed with the pixel array V2. A comparison of the gain measured with $^{55}$Fe and external charge injection is shown in Figure 6.19 (a). An example of the $^{55}$Fe spectrum reconstructed using binary resolution of a single pixel is shown in Figure 6.19 (b).

![Graph of gain vs channel with two plots labeled gain_Fe and gain_inj.](a)

![Histogram of hit count vs threshold voltage with label 1640 electrons.](b)

Figure 6.19: A comparison of the gain of the DMAPS pixels of variant V2 determined independently by an external charge injection and by an $^{55}$Fe source (a). This analysis was done for every pixel (channel) of the array V2. An example of the $^{55}$Fe spectrum, reconstructed using a binary resolution of a single pixel, is shown in Figure (b).

Two effects can be seen in Figure 6.19 (a). 1. The gain fluctuations between the channels determined by $^{55}$Fe are strongly correlated with those seen when the signal is provided by the external charge injection. This result indicates that the gain fluctuations between the pixels are predominantly caused by the gain fluctuations of the FE electronics rather than by a non-uniform charge collection efficiency of the collection electrodes. 2. The mean gain determined by $^{55}$Fe is on average higher by 34% than the mean gain determined by the charge injection. This effect has been studied in detail by design simulations and is most likely caused by the parasitic capacitance of the charge injection circuit and of the capacitor coupling of the collection electrode and electronics.

#### 6.4.6 Radiation effects in the FE electronics of the DMAPS sensors

Radiation tolerance of the FE electronics of the EPCB01 was investigated with radiation from an X-ray tube with an end-point energy of 60 keV. The irradiation was performed within several steps, achieving a total ionizing dose of 50 Mrad. After each irradiation period, the chip has been annealed for 100 minutes at 80 °C. Several tests of the analog and digital part of the pixels were done after each irradiation period. The radiation induced effects were only observed in the analog part of the FE electronics. The most sensitive node of the analog part of the DMAPS pixel is the NMOS feedback transistor in the CSA. Radiation induced shift of the threshold voltage of the feedback transistor changes the discharge time of the CSA. The greatest difference in the discharge time has been observed between an unirradiated
Chapter 6 Depleted Monolithic Active Pixel Sensors

state and after the first irradiation period (200 krad). At higher doses, the discharge time changes only insignificantly up to 50 Mrad, as can be seen in Figure 6.20.

The X-ray irradiation has an overall impact on the FE electronics in terms of changes of gain and noise level of the DMAPS pixels. The dependence of these parameters on the level of irradiation is shown in Figure 6.21 (a, b). The digital part of the DMAPS pixels was tested between the irradiation periods by writing test data patterns in the configuration shift register and reading them back. No difference was observed in the data patterns passing the configuration register of the irradiated EPCB01.

Additional radiation studies have been performed on an array of individual NMOS and PMOS transistors which is a part of the EPCB01, and more detailed results can be found in [78]. All transistors
in the array have a constant channel length of 150 nm but variable channel width between 320 nm and 3070 nm. The NMOS transistor with the channel width of 3070 nm has an enclosed layout geometry, while all other transistors have a standard layout. The radiation induced shift of the threshold voltage has been observed, as well as the degradation of the maximum transconductance of the transistors. Both results are shown in Figure 6.22 (a, b). The threshold voltage of both transistor types shifts by less than 30 mV within the range of radiation dose. The maximum transconductance of the NMOS transistors degrades by less than 2% and in case of the PMOS transistors the transconductance degrades by less than 15%. In general, the radiation effects are more significant in small channel width transistors.

![Figure 6.22: Threshold voltage shift ΔVth (a) and maximum transconductance g_m (b) of the MOSFET transistors as a function of total ionizing dose. The irradiated transistors differ by channel width w while the channel length remains constant (150 nm). These data have been extracted from the work presented in [78].](image)

6.5 EPCB02

The results obtained from the characterization of the EPCB01 test chip indicate good performance of the test chip and proved the concept of a fully depleted MAPS (DMAPS) sensor integrating the complex electronics in the pixel. Motivated by these measurement results, a new version of the test chip was designed - EPCB02. This second version of the test chip differs from its predecessor in several aspects. The goal of the EPCB02 is to fix the issues of the EPCB01 and allow to study the performance of the DMAPS pixels in greater detail. The differences between EPCB01 and EPCB02 are explained in the following sub-sections.

6.5.1 Variants of the DMAPS pixels

The EPCB01 did not allow a direct comparison of the analog performance of two different collection electrodes. If we take for example V1 and V2, they differ in the geometry of the collection electrodes and their biasing at the same time. One could not say with certainty, whether the different performance is due to the biasing or due to the different geometry. In the test chip EPCB02, the DMAPS variants were chosen to comprehensively compare the different variants of the DMAPS pixels. The influence of the geometry of the collection electrodes, type of biasing, FE architecture and dimensions of the input transistor can be studied independently. A list of the variants of the DMAPS pixels is shown in Table 6.2.
Chapter 6  Depleted Monolithic Active Pixel Sensors

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<tr>
<td>V1</td>
<td>D2</td>
<td>diode (AC coupl.)</td>
<td>continuous</td>
<td>1 µm/300 nm</td>
<td>8×8</td>
</tr>
<tr>
<td>V2</td>
<td>D2</td>
<td>resistor (AC coupl.)</td>
<td>continuous</td>
<td>1 µm/300 nm</td>
<td>8×8</td>
</tr>
<tr>
<td>V3</td>
<td>D1</td>
<td>DC coupled CSA</td>
<td>continuous</td>
<td>1 µm/300 nm</td>
<td>6×8</td>
</tr>
<tr>
<td>V4</td>
<td>D2</td>
<td>diode (AC coupl.)</td>
<td>switched</td>
<td>1 µm/300 nm</td>
<td>6×8</td>
</tr>
<tr>
<td>V5</td>
<td>D1</td>
<td>diode (AC coupl.)</td>
<td>switched</td>
<td>1 µm/300 nm</td>
<td>8×8</td>
</tr>
<tr>
<td>V6</td>
<td>D2</td>
<td>diode (AC coupl.)</td>
<td>switched</td>
<td>2 µm/150 nm</td>
<td>8×8</td>
</tr>
</tbody>
</table>

Table 6.2: Different variants of the DMAPS pixels integrated in the EPCB02.

6.5.2 Collection electrodes

The design of the EPCB02 does not rely on the layout of the charge collection electrodes provided by the foundry, and created our own layouts called D1 and D2. Both layouts use a circular geometry of the charge collection electrodes. The circular layout reduces the high electric field, which otherwise appears on the edges of the rectangular collection electrode. The circular geometry should have a smaller leakage current and should be more radiation tolerant than the rectangular electrode. A screenshot of the layout of the charge collection electrodes is shown in Figure 6.23 and a schematic cross section of the collection electrodes is shown in Figure 6.24.

Figure 6.23: A layout of two DMAPS pixels with a different layout of the circular charge collection electrodes. Left: a pixel with the collection electrode of the variant D2. Right: a pixel with the collection electrode of the variant D1.

Both collection electrodes have the same diameter of the opening in the p-substrate, but they differ in the width of the n+ regions. The motivation for the two different layouts is to study their charge collection efficiency and capacitance.
6.5 EPCB02

Figure 6.24: A schematic cross section of the structure of the collection electrodes D2 (a) and D1 (b).

6.5.3 Changes in the FE electronics

Several changes have been made in the FE electronics, particularly in the design of the CSA. The size of the input transistors of the CSAs has been increased from the original $W/L = 400/300$ nm to $W/L = 1000/300$ nm and $W/L = 2000/150$ nm in V6. The motivation for larger transistors is the elimination of the RTS noise, which has been observed at the EPCB01.

The pixels of the EPCB01 suffered from a large dispersion of the gain of the CSA. In addition, the gain of the DMAPS pixels was found to be too high (signal from $^{90}$Sr often saturated the CSA). These issues have been addressed by the redesign of the CSA. The core amplifier in the EPCB02 uses a cascode amplifier with the feedback capacitance of 2 fF. A high open loop gain of the cascode CSA will remove the sensitivity of the closed loop gain on the sensor capacitance. The feedback capacitance of 2 fF will reduce the pixel gain and homogenize the gain distribution across the pixel matrix with respect to the EPCB01.

The layout of the charge injection circuit was reworked as well, in order to minimize its influence on the gain of the CSA.

The analog outputs of the EPCB01 were found useful for the initial chip testing, studying the signal shapes and measuring spectra of various radioactive sources. Since the EPCB01 always has only one fixed pixel of the particular matrix connected to the analog output, the potential of the analog outputs to study the parameters of more pixels was limited. In the EPCB02, the analog output is programmable and can be connected to an arbitrary pixel of the particular matrix. Each matrix has its own programmable analog output. The analog output of each pixel matrix is connected to an IO pad via a strong rail to rail buffer.

6.5.4 Monolithic PixCap

The results of the gain measurements of the EPCB01 raised a question of the capacitance of the charge collection electrodes. It is expected not to be higher than a few fF, but the exact number is unknown. With the previous experience with the capacitance measurement of the pixel sensors obtained with the PixCap chip, a similar structure, using a charge-pump based capacitance measurement, was implemented in the EPCB02 to determine the capacitance of the charge collection electrodes. A schematic of this capacitance measurement circuit is shown in Figure 6.25.
A pair of switching transistors is connected to the collection electrode via an AC coupling capacitor \( C_{AC} \) in the same way as in the DMAPS pixel. Due to the AC coupling, the collection electrode can be biased by a high voltage without affecting the low voltage switching part. This "Monolithic PixCap" will allow not only the measurement of the absolute value of the capacitance, but also its scaling with the bias voltage. This experimental method will allow the measurement of a full depletion voltage of the DMAPS pixels in the same way as the full depletion voltage was determined in the case of the planar silicon sensor with PixCap (see Section 3.5.2).

Three capacitance measurement cells are integrated in the EPCB02 for the measurement of the capacitance of the charge collection electrodes D2 (diode biased), D2 (resistor biased) and D1 (diode biased). One more cell is disconnected and will be used for the determination of the parasitic capacitance of the switches. A layout of the entire circuitry for the capacitance measurement is shown in Figure 6.26.

### 6.6 Summary of the DMAPS pixels

A novel concept of the Depleted Monolithic Active Pixel Sensor (DMAPS) was introduced in this chapter. A test chip EPCB01 was designed and tested. Several variants of the DMAPS pixels were integrated in the EPCB01, differing by the geometry of the sensitive elements, their biasing and architecture of the FE electronics. The best analog performance was achieved with the diode biased variant with time-continuous FE electronics. The gain of this variant is approximately \( 100 \, \mu V/e^- \) and noise 30 e\(^-\) (measured with a charge injection of 1 ke\(^-\) and return to the baseline of 1 \( \mu s \)). An unexpected RTS noise component was observed in all variants of the DMAPS pixels.

The dispersion of the detection threshold of the DMAPS pixels is approximately 135 e\(^-\) after threshold equalization by a 4-bit DAC. By a cluster analysis, the full depletion voltage was determined to be 6 V. Radiation hardness of the pixel FE electronics was evaluated with an X-ray tube by irradiating the EPCB01 up to a total ionizing dose of 50 Mrad. Small radiation induced effects were observed in the analog FE electronics, but no effects at all were observed in the digital electronics. More radiation tests need to be done to study radiation effects arising from bulk damage and their impact on the amount of signal to be collected and on the charge collection mechanism itself.

The concept of the DMAPS pixels is therefore very promising and may become a competitor of hy-
6.6 Summary of the DMAPS pixels

Figure 6.26: A layout of the electronic circuit for the capacitance measurements of the charge collection electrodes of the DMAPS pixels.

In spite of the fact that the EPCB01 is the first demonstration of the DMAPS pixels, its overall performance is very good and many important lessons have been learned. Based on the results obtained with the EPCB01, a new prototype chip, EPCB02, was designed and submitted for manufacturing. New features, like a programmable analog output and a capacitance measurement circuit, were implemented. After fabrication, the EPCB02 will become a powerful tool to study the analog performance of the DMAPS pixels.

This work was submitted for publication [79].
Chapter 7

Conclusions

The High Luminosity upgrade of the Large Hadron Collider (LHC) imposes new challenges for the tracking systems of the ATLAS experiment. In particular, the pixel detector will face up to ten times higher hit rates and radiation doses than it was originally designed for. New, more advanced, technologies are needed to be implemented in the pixel detector to keep track with increasing luminosity of the LHC. This thesis is oriented to exploration of new technologies of the pixel sensors, the front-end (FE) electronics of the hybrid pixel detectors and development of the monolithic pixel sensors.

The silicon pixel sensors in the high luminosity environment will have to withstand fluences of about $2 \times 10^{16}$ $\text{n}_{\text{eq}}/\text{cm}^2$, causing a substantial radiation damage in terms of increased leakage current and reduced charge collection efficiency. Diamond sensors are potentially more radiation tolerant technology compared to silicon planar sensors. To quantitatively compare the Signal to Noise Ratio of both sensor technologies a key ingredient is needed to be determined, the pixel capacitance. For that purpose a dedicated integrated circuit for a precise measurement of the pixel capacitance was designed and capacitance of various sensor types was measured. The chip for capacitance measurement is called PixCap. Capacitance of three sensor types was measured with the PixCap chip: silicon planar sensor, diamond sensor and silicon 3D sensor. The highest capacitance was measured with the silicon 3D sensor of approximately 169 fF. The conventional planar silicon sensors have a capacitance of 105 fF. The lowest capacitance has the diamond sensor of approximately 21.4 fF. Using these data, the diamond sensor was shown to provide a better SNR than planar silicon sensor at high fluences.

An extreme hit rate of the order of 1-2 GHz/cm$^2$ is expected in the innermost layers of the ATLAS pixel detector after the High Luminosity upgrade. A fast signal processing from a highly segmented pixel sensors is required. An ultra deep submicron CMOS technology is a good candidate to meet the requirements for design of a new generation of the pixel FE chips. Two chip prototypes were designed in 65 nm CMOS technology: FE-T65-0 and FE-T65-1. The laboratory testing of the FE-T65-0 demonstrated applicability of this technology to design an analog pixel FE electronics. Based on the results obtained with FE-T65-0 a new, more complex, prototype FE-T65-1 was designed. A matrix of 32 pixels with four variants of the FE electronics was integrated in the FE-T65-1 and advanced features for evaluation of analog performance were implemented. One of them uses an adjustable input capacitance representing capacitance of the pixel sensor allowing for example the determination of the noise performance as a function of the input capacitance. This feature allows to estimate the noise levels which could be achieved with different sensor types. Noise levels projected for the silicon planar sensors (capacitance of 75 fF) is 113-183 e$^-$, depending on the FE variant. The noise scales almost linearly with the input capacitance. One of the goals of FE-T65-1 was the implementation of a dynamic (switched) discriminator. Advantage of this discriminator is high speed and small contribution to the timewalk of the analog front-end and is a potentially interesting solution to reduce power consumption of the pixel electronics. Use of the dynamic discriminator was proven to reduce the power budget of the pixel com-
pared to the pixel with a continuous (standard) discriminator while preserving a timewalk below 25 ns. On the other hand, periodical switching of the discriminator introduces an additional noise in the pixel increasing the total noise budget by 20-30%. The detection threshold has dispersion values from 267 to 405 e\textsuperscript{-} (depending on the FE variant) and can be tuned by a 5-bit TDAC to levels below 30 e\textsuperscript{-} in all pixel variants. The analog parameters of the pixel electronics integrated in FE-T65-1 are well comparable with those of the latest version of the pixel chip FE-I4. However, by reducing the pixel size, the power density did not remain constant. In the best case, the analog power density in FE-T65-1 is 35% higher than in FE-I4.

A new direction in the pixel technologies for HEP applications are Monolithic Active Pixel Sensors (MAPS). A new concept of Depleted MAPS (DMAPS) is introduced in this thesis. The DMAPS sensors are fabricated in high resistive silicon substrate and therefore allow to achieve full depletion of the silicon bulk. This solution allows fast collection of the entire signal charge generated in the depleted silicon bulk. A test chip EPCB01 was designed to prove this concept. Six slightly different arrays of the DMAPS pixels were integrated in the chip. The performance of the DMAPS pixels was evaluated in the laboratory. The highest gain of the pixels is approximately 100 µV/e\textsuperscript{-} and noise 30 e\textsuperscript{-}. The dispersion of the gain is about 20% and the dispersion of the threshold is in the best case 78 e\textsuperscript{-}. The cluster analysis performed with a radioactive source (\textsuperscript{90}Sr) shows a typical cluster size of one pixel. The ratio of the single to double pixel clusters increases with voltage applied to the charge collection electrodes and saturates at 6 V. This effects indicates a full depletion of the sensor. Good response of the sensor was shown also when irradiating with \textsuperscript{55}Fe and reconstruction of the characteristic peak at energy 5.9 keV. Radiation tolerance of the FE electronics of the DMAPS pixels was evaluated by radiation from an X-ray tube. After absorbing a total ionisation dose of 50 Mrads only small effects in the analog electronics have been observed. Shortening of the pulse at the output of the CSA is a consequence of the radiation induced shift of the threshold voltage of the transistors. Noise levels of the pixels increased from 30 to 45 e\textsuperscript{-}. The results indicate a good overall performance of the DMAPS pixels. However, many another tests need to be done to fully evaluate the potential of the DMAPS for their application the future tracking detectors. Several lessons have been learned with EPCB01. The pixels are subject of gain variations and the gain is sensitive to the input capacitance. These issues have been targeted in a new version of the DMAPS prototype EPCB02 which was submitted for manufacturing in the time of writing this thesis.
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My research projects involved design of several integrated circuits, which needed to be wirebonded to PCBs. Some of them were mechanically difficult chip and sensor assemblies, others had complicated wirebond plans and some of them were thinned and fragile silicon chips. Walter Ockenfels and Wolfgang Dietsche always found a suitable solution for wire-bonding of my chips. Many thanks belong to them.

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Bibliography


Bibliography

[34] F. Hügging, Upgrades of the ATLAS Pixel Detector - From IBL to Phase 2, presentation, 22nd international Workshop on Vertex Detectors Vertex 2013, 2013.


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