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13 November 2017

The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

This work is part of AIDA-2020 Work Package 6: **Novel high voltage and resistive CMOS sensors.**

The electronic version of this AIDA-2020 Publication is available via the AIDA-2020 web site <http://aida2020.web.cern.ch> or on the CERN Document Server at the following URL:
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Simulations of depleted CMOS sensors for high-radiation environments

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ABSTRACT: After the Phase II upgrade for the Large Hadron Collider (LHC), the increased luminosity requests a new upgraded Inner Tracker (ITk) for the ATLAS experiment. As a possible option for the ATLAS ITk, a new pixel detector based on High Voltage/High Resistivity CMOS (HV/HR CMOS) technology is under study. Meanwhile, a new CMOS pixel sensor is also under development for the tracker of Circular Electron Position Collider (CEPC). In order to explore the sensor electric properties, such as the breakdown voltage and charge collection efficiency, 2D/3D Technology Computer Aided Design (TCAD) simulations have been performed carefully for the above mentioned both of prototypes. In this paper, the guard-ring simulation for a HV/HR CMOS sensor developed for the ATLAS ITk and the charge collection efficiency simulation for a CMOS sensor explored for the CEPC tracker will be discussed in details. Some comparisons between the simulations and the latest measurements will also be addressed.

KEYWORDS: Solid state detector; Radiation-hard detectors; Particle tracking detectors (Solid-state detectors).

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1. Introduction

At the end of 2022, the LHC will have a major upgrade, called Phase II Upgrade. From 2024 on, the HL-LHC will provide unprecedented pp luminosities to ATLAS[1] with a levelled instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. Simulations predict that the maximum 1 MeV neutron-equivalent fluence and ionizing dose will be $1.4 \times 10^{16} \text{ cm}^{-2}$ and 770 MRads at the centre of the innermost barrel layer[2]. A new full-silicon tracker, called Inner Tracker (ITk) is proposed for the ATLAS in order to withstand the much harsher radiation and occupancy conditions of the HL-LHC environment. The very high hit rate requires complex readout logic towards small radius of the ITk. For the outer layers of the ITk, the hit rates and radiation level are comparable to the present running pixel detectors, which means it may be possible to replace the module of passive silicon sensor with readout IC by a module consisting of only a single HV/HR CMOS monolithic chip. This kind of depleted HV/HR CMOS sensor could offer improved spatial resolution, better two-track separation and lower construction price.

The proposed Circular Electron Position Collider (CEPC) [3] would operate at $\sqrt{s} \sim 240 \text{ GeV}$ as a high luminosity Higgs factory. The e^+e^- collision could offer a much cleaner environment than the LHC for the Higgs study. The CEPC detector mainly consists of a vertex detector, a silicon tracker, a Time Projection Chamber (TPC), a calorimetry system, a superconducting solenoid and a muon detector. The CEPC silicon tracker derives its baseline design from the concept of “Silicon Envelop” [4] with necessary modifications. In order to fulfill the high precision track reconstruction, the single point resolution should be $< 7 \mu\text{m}$ and the material budget $< 0.65\% X_0$. The basic elements for the silicon tracker would be the mature silicon microstrip sensors. However, an alternative solution of a pixelated CMOS sensor is also under study. Compared with the micro-strip sensor, the pixelated CMOS sensor could offer better spatial resolution and less material budget.

2. Simulation Methodology

In this paper we discuss some simulation results which were carried out by using Technology Computer Aided Design (TCAD) simulation tools. The TCAD refers to the use of computer simulations to develop and optimize semiconductor processing technologies and devices. The simulations were performed by the SYNOPSIS Sentaurus TCAD [5].

2.1 TCAD Simulation

The TCAD simulation software simulates the semiconductor physics processes by solving some specific equations with finite element method. Devices for simulation were generated by using the Sentaurus Process and the Sentaurus Structure Editor (SDE). They support various advanced process options, such as isotropic or anisotropic deposition and etching, trench formation, diffusion and implantation. Sentaurus Device (SD) is a multidimensional, electro thermal, mixed-mode device and circuit simulator for one-dimensional, two-dimensional (2D), and three-dimensional (3D) semiconductor devices. The simulations were performed by solving the Poisson equation and the drift-diffusion equations on the meshed devices. Various physical models and numeric methods can be chosen in the SD, such as concentration-dependent mobility, avalanche generation, Shockly-Read-Hall recombination and heavy ions model (impact ionization). The physical models should be chosen properly and some default parameters, for instance the lifetime of the free carriers in substrate should also be tuned for a specific simulation in order to obtain precise simulation results and save computing time. The DC simulations were performed in order to investigate the leakage current, the depletion and the breakdown voltage. The sensor responses for Minimum Ionizing Particle (MIP) were simulated through the transient simulations. The temperature was set to ambient temperature in the simulations.

2.2 Radiation Damage

In a silicon sensor, the radiation damage is divided into bulk and surface defects. The bulk damage is caused by the displacement of crystal atoms. The surface defect consists of the fixed charge which accumulate in oxide and of the interface traps which build up at the silicon oxide interface. Both types of defects can lead to an increase of the leakage current, an increase of the full depletion voltage, and charge trapping. Many efforts have been done for the radiation damage modeling

Type	Energy(eV)	$\sigma_e(\text{cm}^2)$	$\sigma_h(\text{cm}^2)$	$\eta(\text{cm}^{-1})$
Acceptor	Ec -0.42	9.5×10^{-15}	9.5×10^{-14}	1.613
Acceptor	Ec -0.46	5×10^{-15}	5×10^{-14}	0.9
Donor	Ev +0.36	3.23×10^{-13}	3.23×10^{-14}	0.9

Table 1: P-type bulk damage model. σ_e is electron capture cross-section. σ_h is hole capture cross-section. η is introduction rate.

within ROSE and CERN RD50 collaborations. For the simulations in this paper, the bulk damage model we used is listed in Tab. 1 [6]. As for the interface defects, we assumed that the density of interface traps is equal to the density of fixed charge. Two interface states were introduced on the

Si/SiO₂, a deep trap (Ec-0.6eV) accounting for 60% and a shallow traps (Ec-0.39eV) accounting for 40% [7].

3. Simulations for the ATLAS HV/HR CMOS sensors

Several HV/HR CMOS prototypes fabricated with AMS 180 nm, GF 130 nm and LF 150 nm technology were developed and characterized by the ATLAS HV CMOS collaboration. In this chapter, the guard-ring simulations for the LF prototypes will be discussed. The first prototype with high resistivity, called CCPD LF, was designed by using LF 150 nm technology in 2014, and was characterized in 2016. Some design and test results can be found in [8]. A large demonstrator ($1\text{ cm} \times 1\text{ cm}$) that has the same pixel size as FE-I4 [9] was designed in LF 150 nm technology and submitted in March of 2016 in order to demonstrate the sensor performance for the ATLAS ITk. The demonstrator has two different versions called LF CPIX V1 and LF CPIX V2 respectively. For the LF CPIX V1, the guard-ring layout has the same parameters as CCPD LF. With respect to the measurements of CCPD LF, the guard-ring layout for the LF CPIX V2 has been optimized by performing the TCAD simulations in order to improve the breakdown voltage and reduce the inactive area.

3.1 Simulation Geometries

The diagrams of the guard-rings for simulation are shown in Fig.1. The DNW-pixel is the outer most pixel in the matrix. The PW-pixel is the guard-ring surrounding the pixel. The NWellring aims to give a smooth electric field distribution for the DNW-pixel. The PWellring is the first guard-ring, which can be floating or connected to -HV. The g1 to g7 are floating guard-rings. The bb, called back-bias, is connected to -HV and the sr is seal-ring. For the guard-rings, the LF CPIX V1 used a conservative strategy with the guard-rings having exact the same size as for the earlier CCPD LF prototype, as sketched in Fig.1a. Compared with LF CPIX V1, the guard-rings of LF

Figure 1: The guard-ring layout scenarios. The value unit is μm . (a) Guard-ring of the LF CPIX V1. The same size as CCPD LF except for the DNW-pixel size. (b) Guard-ring of the LF CPIX V2. Shrunk NWelling + reduced floating guard-rings: To improve the breakdown voltage and reduce the inactive area.

CPIX V2 have been optimized trying to increase the breakdown voltage and reduce the inactive region. The diagram of this guard-ring is shown in Fig.1b. The NWellring was shrunk to increase

the breakdown voltage. The M1 (first layer of metal) overhang was also optimized and the outer five guard-rings were removed to reduce the inactive region.

Figure 2: Device for the LF CPIX V2 simulation

The partially pixel region implemented in the simulation is shown in Fig.2. The fixed charge and the interface trap were implemented in the STI and the NIEL effects were also taken into account in the substrate. In simulation, the current recorded by the DNW-pixel and by the NWring were measured.

3.2 Simulation Results

Concerning the LF CPIX V1, the leakage currents before and after a fluence of $1 \times 10^{15} n_{eq}/cm^2$ are shown in Fig.3. In this simulation, the PW-pixel, the PWellring and the bb (back-bias) was connected to -HV. One can see that the DNW-pixel dominates the breakdown for both before and

Figure 3: The leakage currents as a function of HV depending on fluences. (a) Decreased breakdown voltage with increasing irradiation fluence. The similar behavior observed from the measurement. (b) The breakdown voltage reduced compared with LF CPIX V2. The simulation result precisely predicts the breakdown voltage with respect to the measurement.

after irradiation. After irradiation, the breakdown voltage decreases from -90 V to -105 V in the simulation. A similar behavior was observed from the proton irradiation test at CERN PS. The measured breakdown voltage changed from approximately -76 V to -90 V after the fluence of $1 \times 10^{15} n_{eq}/cm^2$. The simulation results show good agreement with the measurements.

For the LF CPIX V2, only the bb was connected to -HV and the remaining guard-rings were floating. As shown in Fig.3b, the breakdown voltage decreases to roughly -240 V by shrinking the

NWellring and tuning the M1 overhang. After irradiation, the breakdown voltage decreases from approximately -240 V to -360 V. The first measurement showed that the breakdown voltage of LF CPIX V2 is roughly the same value as simulations.

The depletion regions and electric field distributions for the LF CPIX V1 and the LF CPIX V2 are shown in Fig.4. For LF CPIX V2, the distance between the end of the depletion area and the cutting edge (inactive distance) is roughly $100\ \mu\text{m}$ when the high voltage is -100 V. Compared with LF CPIX V1, one can see that the inactive distance reduced from $330\ \mu\text{m}$ to $100\ \mu\text{m}$. The improved breakdown voltage and reduced inactive area would result in better radiation tolerance and improved charge collection efficiency for the LF CPIX V2.

Figure 4: The electric field distribution of LF CPIX V2.

4. Simulations for the CEPC CMOS sensors

In order to explore the performance of the CMOS pixel sensor for the CEPC silicon tracker, a prototype [10] has been designed by using the TowerJazz 180 nm CMOS imaging sensor technology. For this technology, a $18\ \mu\text{m}$ epi-layer with the resistivity of $1\ \text{k}\Omega \cdot \text{cm}$ is grown upon a low resistivity substrate. Therefore an enlarge depletion region and improved breakdown voltage could be achieved due to the high resistivity epi-layer, which could result in better charge collection efficiency and radiation hardness.

4.1 Simulation Geometries

In order to investigate the charge collection efficiency and signal to noise ratio (SNR), the pixel matrix is divided into 9 submatrices in terms of the charge collection diode size and the pixel pitch. Each submatrix consists of 64 rows and 16 columns. The pitch of the pixel is fixed to $21\ \mu\text{m}$ in X-axis. Along the Y-axis, there are three different pitches of $21\ \mu\text{m}$, $42\ \mu\text{m}$ and $84\ \mu\text{m}$. The layout of the diode and the doping diagram are shown in Fig. 5a and Fig. 5b respectively. The diode is implemented with a octagonal N-Well (NW) and a P-Well (PW) guard-ring. Between the NW and the PW, a PW-opening is drawn in order to keep the same resistivity as the epi-layer in this area. The detailed diode parameter and the pixel pitch in the 9 submatrices are listed in TABLE. 2.

(a) The layout of the diode

(b) Doping diagram of the diode

Figure 5: Charge collection diode. (a) The diode formed by a octagonal NW and a PW guard-ring. The PW-opening (P-) means no PW implementation in this area. (b) The region between the NW and PW keeps high resistivity thanks to the PW-opening layer.

Pixel	P1	P2	P3	P4	P5	P6	P7	P8	P9
Pitch (x) (μm)	21	42	84	21	42	84	21	42	84
F (μm^2)	11	11	11	5	18	18	15	44	50
S (μm^2)	8	8	8	4	12	12	6	20	20

Table 2: Overview of the pixel parameters. F represents the area of both the NW and PW-opening. S represents the area of the NW. For example, the diode F11_S8 means the NW area is $8 \mu m^2$ and the PW-opening area is $3 \mu m^2$.

4.2 Simulation Results

In this chapter, the transient simulations for the pixel P1 will be discussed. A 3D device implemented with 5×5 -pixel array was created, as shown in Fig. 6. The MIP impinges the center of

(a) 3D device for simulation

(b) 5×5 -pixel array

Figure 6: Transient simulation overview for the pixel P1. (a) The 3D device (5×5 -pixel array) is created for the transient simulation. (b) The MIP impinges the center of “Pixel 13”. The MIP direction is perpendicular to the device surface.

“Pixel 13” perpendicularly to the device surface. The induced signals for the “Pixel 13”, the “Pixel 12” and the “Pixel 17” are shown in Fig. 7. The substrate is biased at -3.3 V. The contributions of the signal for the “Pixel 13” are from both the charges collected by drift and by diffusion. The charges collected by the “Pixel 12” and “Pixel 17” are only from diffusion due to the non-depleted region of the epi-layer. After the irradiation fluence of $1 \times 10^{14} n_{eq}/cm^2$, there are almost no charges can be collected for the “Pixel 12” and the “Pixel 17” due to the diffusion charges losing. Whereas, the charges moving by drift can still be collected for the “Pixel 13”. The accumulated charges collected by the “Pixel 13”, “Pixel 12” and “Pixel 17” with different radiation levels are shown in

Figure 7: The MIP responses of pixels (P1) depending on radiation fluences. The signals for the “Pixel 13”, the “Pixel 12” and the “Pixel 17” are plotted in red, green and blue respectively.

Fig. 8. The collected charges decrease with increased radiation fluence. For the “Pixel 13”, the collected charges are approximately 1700 before irradiation. After the fluence of $1 \times 10^{14} \text{ neq/cm}^2$, the collected charges reduces roughly in half. Before irradiation, the charges collected by the “Pixel 12” and the “Pixel 17” are around 470 and 400 respectively. As discussed above, no charges can be collected by these two pixels after the irradiation fluence of $1 \times 10^{14} \text{ neq/cm}^2$.

Figure 8: Collected charges as a function of fluence. The charges collected within $20 \mu\text{s}$ are counted.

Due to the limited voltage (the minimum value is - 10 V from DC simulation) which could be applied to the substrate and the small surface of the diodes, large un-depleted areas exist between the diodes, as shown in Fig. 9. The not fully depleted epi-layer leads to a reduction of the charge collection. Further modifications will be performed in order to improve the breakdown voltage and enlarge the depletion area.

5. Summary and perspectives

In this paper, the guard-ring layout of the LF CPIX V2 has been optimized by the TCAD simulations, and preliminary measurements reveal that the simulations are in good agreement with the test results. The improved breakdown voltage and the decreased inactive area could allow the sensor to have a full depletion with the substrate thickness of $100\mu\text{m}$ and ensure sufficient depletion area

Figure 9: Depleted region. The substrate is biased at - 3.3 V. The contour in white is the depletion edge. The regions between the diode in yellow and the contour are depleted area.

after radiation level of $1 \times 10^{15} \text{ neq/cm}^2$. Further characterization will be performed to explore the improvement of the detection efficiency for the LF CPIX prototypes.

The charge collection behavior of the CMOS sensor which was developed for the CEPC tracker was also simulated particularly the NIEL radiation damage. The charge collection mechanism was studied through the simulation. After the radiation fluence of $1 \times 10^{12} \text{ neq/cm}^2$, all of charges collected by diffusion would be lost due to the induced traps in the bulk. For this prototype, the limited bias voltage applied to the substrate results in inadequate depletion region in the epi-layer, which would cause detection efficiency problem after radiation. The corresponding optimizations will be made in the next prototype with respect to the simulation and further measurements.

Acknowledgments

This work has been supported by the H2020 project AIDA-2020, GA no. 654168.

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