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**A 66 MHz, 32-CHANNEL ANALOG MEMORY CIRCUIT WITH DATA
SELECTION FOR FAST SILICON DETECTORS**

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ABSTRACT

An analog memory array with 64 memory cells for each channel has been designed and manufactured in CMOS. A new skip logic controller allows to write at 66 MHz without dead time and to read out at a lower frequency simultaneously. The input circuit is charge-sensitive and integrates continuously. Pedestal non-uniformity is 1.4 mV r.m.s. from cell-to-cell and 3.5 mV r.m.s. between channels. The linearity range is -2.5 V to +1.5 V, which corresponds to 11 bits. The chip has been used in a particle detection test.

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1. INTRODUCTION

At the future high-luminosity hadron colliders Large Hadron Collider (LHC) at CERN and Superconducting Super Collider (SSC) in Texas each experiment will use a variety of detector systems. The Silicon Tracker and Preshower (SITP) detector is designed to achieve high-precision track reconstruction and electron–hadron identification of particles just before the calorimeter. Such a detector has to cover an area of several tens of square metres and it will contain about ten million silicon sensor elements. This large number of sensors, together with a LHC collision rate of 66 MHz will generate an enormous amount of data which practically cannot be transmitted off detector. Moreover, the power dissipation in the interior of such an hermetic detector system must be limited to a few kilowatts.

Analog signal storage in a hierarchical data processing architecture, called HARP, has been proposed [1–3] as a new approach to detector readout for the hadron collider environment. If mixed-mode analog/digital Very Large Scale Integration (VLSI) microelectronic circuits are used, it can be envisaged to locate some data processing immediately on the SITP detector. Only the data corresponding to the interaction which is chosen by the first-level trigger (LVL1) will be selected for relatively slow, low-power analog-to-digital conversion. Further compression of data is achieved by zero suppression. In this way one can avoid a bottleneck in data transmission and reduce at the same time the power consumption inside the detector by eliminating analog driver circuits. A data reduction of $\sim 10^6$ may be obtained in such a filtering scheme.

In this paper we present the characteristics of the first comprehensive 32-channel circuit that aims at implementing this basic HARP architecture for data filtering. Each channel of the circuit is composed of a fast front-end amplifier of the current conveyor (ICON) type [4] and an array of 64 addressable analog memory cells. These store the analog information during the time needed to reach the first-level trigger decision (LVL1 latency period).

The design options for the amplifiers and the analog memory in the front-end system are described in sect. 2. The experimental realization of the 32-channel analog memory chip “32-SITP” is described in sect. 3 with emphasis on the skip controller, which represents a novel scheme for simultaneous write and read operations. In sect. 4 the characteristics of the 32-SITP are listed, e.g. linearity, noise, dynamic range and speed. For practical reasons, the similar 4-channel analog memory “4-HARP” chip [3] has been used for the radioactive source measurements with a silicon particle detector (sect. 5).

In particle physics experiments using electronic detectors, each sensor element has traditionally been regarded as a separate detector/readout channel. In the HARP architecture the output multiplexing reduces the effective number of readout channels in the Data Acquisition (DAQ) system. Thus, the number of separate electronic readout chips is more significant for the DAQ structure than the number of sensors. The on-chip data selection and zero suppression alleviates further the data acquisitions task.

A low-power ADC has been studied in a separate chip [5,6] but is not yet incorporated in the experimental 32-SITP circuit. All front-end electronics from preamplifier until digitization will eventually be integrated onto a single VLSI chip. Beyond the advantage of a very high density of components this approach offers lower-noise and lower-power consumption than can be obtained with hybrid or multi-chip technology. With 32 or 64 channels per chip in a submicron CMOS technology the power consumption can be < 5 mW per sensor element.

Analog memories based on switched capacitor techniques can now be designed to have a precision and a dynamic range better than that of CCDs (charge coupled devices). Compared to CCDs they have the advantage of static charge storage, random access addressing, read-while-write at even different frequencies, and a lower power consumption.

Other switched capacitor based analog memories for use in high-energy physics experiments are described in refs [7,8].

2. THE HARP SIGNAL PROCESSING ARCHITECTURE

2.1 General description

The signal processing for the SITP detector will use the HARP architecture. The key feature in this device is the addressable analog memory array for temporary data storage. The analog signals from each sensor element are stored in cells which sequentially act as the feedback capacitor of a fast input amplifier. Various aspects will be treated in more detail in sect. 2.2.

The HARP architecture [2] is based upon the assumption that only a small fraction of the data coming from the sensor elements will be of interest for further processing. A selection of data has to be made in time and in space to identify this valid information. Most particle interactions, while creating signals in some of the sensor elements, will not pass the LVL1 filter because they do not fulfil the selection criteria. In a hadron collider environment one expects less than one in $\sim 10\,000$ interactions to give an LVL1 trigger, i.e. on average less than one every

2 μ s. The direct sensor data themselves may or may not contribute to this LVL1 decision process. The signals are stored in the analog memory at 66 MHz sampling frequency, until the moment at which it has been decided that an interesting interaction has occurred. During this LVL1 “trigger latency period”, one has to keep all data, with the possible exception of those coming from sensors which had a zero signal. The exact length of this period in an LHC experiment will become clear at a later stage, but it is expected to be $< 2 \mu$ s. Subsequently, the memory must continue to hold the LVL1-selected data until the moment that these can be digitized.

A silicon detector delivers a current signal of ~ 10 ns duration. This allows the use of a fast amplifier with a peaking time of 15 ns which corresponds well to the LHC bunch crossing interval. In this case, the occupancy of the memory and the pile-up effects can be considerably reduced. If all signal charge can be stored in one or two cells the data processing is also simplified because no complex analog signal reconstruction is needed. One has a direct correspondence between the location of the data in the memory and the LHC timing.

Only a small number of sensor elements will have been “hit” by particles in the LVL1-selected event-time slot, even if several simultaneous interactions have occurred. This occupancy ratio is expected to be typically 10^{-3} . In the HARP architecture it is foreseen to read out only the sparse non-zero data. This sparse data selection (sparsification) can be implemented in different ways (one possibility is illustrated in fig. 1). The discriminator is placed after the analog memory array. It selects the data that will be converted by the medium-speed, low-power ADC. Besides compressing the data into useful information, the HARP architecture also allows to read the data at a reduced frequency, while writing at the input side proceeds at 66 MHz, without any deadtime. This presents also advantages in power dissipation and in noise.

The block diagram of fig. 1 illustrates the conceptual design for the future SITP detector front-end circuit. Various ancillary functions, like digital output buffers, time and position tagging will be included eventually. The LVL1 trigger is autonomous and not influenced by the SITP detector data. Final specifications for the various blocks in the chip and for the output formats will depend on the external data acquisition system.

2.2 Design of the analog memory

The analog memory uses switched capacitor cells to store the analog information and fast linear CMOS circuits as write or read amplifiers. The design has to match the characteristics of the detector that must be read out. For segmented,

300 μm thick silicon detectors like the pad and microstrip detectors in the SITP, the typical signal charge from a Minimum Ionizing Particle (MIP) is equivalent to that of 25 000 electrons. This charge signal from one MIP is converted to a 30 mV signal on the storage capacitors. The minimum acceptable signal-to-noise ratio is 10 and therefore the tolerable Equivalent Noise Charge (ENC) should be below 2500 e⁻ r.m.s.

The write section of the analog-memory cell is configured as a charge sensitive amplifier with 64 signal storage capacitors (fig. 2). The capacitors in a row are sequentially connected in the feedback loop to integrate the signal current during the clock period. Each complete memory cell consists of one capacitor and 5 NMOS analog switches for addressing that capacitor in the write, read or erase mode. The capacitors are made with 2 polysilicon layers and they have a value of 0.4 pF. In the charge-sensitive configuration, the signal current coming from the front-end charge amplifier is integrated onto the capacitor over the 15 ns clock period. An advantage of this configuration is that errors due to noise or sampling time jitter are reduced.

The read section of the memory senses the voltage on the storage capacitor, which is proportional to the integrated charge sample. Since the leakage of the switches is very low (< 10 pA), the signal can be read out at a much later time, typically a few microseconds afterwards.

An erase switch makes direct connection between the two capacitor nodes in order to cancel the charge just before a new integration is made. The dynamic range of the analog storage cell depends on the size of the capacitor, the voltage swing and the noise floor. The linearity is mostly determined by the characteristics of the write and read amplifiers.

The analog memory must present sufficient uniformity among the cells to avoid the need for calibration of individual cells. This is determined by the uniformity of the physical properties along the array and can be obtained by careful processing. Matching between capacitors in a commercial CMOS technology is usually 0.1% to 0.2%. This gives a linearity variation from cell-to-cell of the same order of magnitude. Careful layout along with the optimization of the component parameters and shapes minimizes cell-to-cell random effects which limit uniformity. In theory it should be possible to achieve a pedestal variation of < 1 mV r.m.s.

Systematic effects can be tolerated if they affect all the cells equally. Some examples are charge injection during the switching, clock feedthrough via parasitic capacitors, the DC offset and the slew rate of the amplifiers. Limited precision in the pedestals and the gain of the analog memory comes from gradually or randomly distributed effects. Gradually distributed effects like capacitor oxide thickness

variation and pattern variation due to lithography or etching are induced mainly during the wafer processing. Values have been published [9,10] for the randomly distributed, localized pattern variations.

The non-uniformity combined with other sources of noise gives rise to a noise level of a few millivolts. The signal-to-noise ratio is then sufficient for the detection of a single minimum ionizing particle without further cell calibrations. Channel-to-channel variations on a chip are caused mainly by the offset variations of the write and read amplifiers. These can be corrected for by one calibration factor for each sensor element.

3. THE 32-CHANNEL ANALOG MEMORY CHIP

3.1 Circuit description

The 32-SITP chip is a prototype version of the SITP front-end electronic circuit using the HARP architecture. It features real-time data acquisition and readout. In comparison with the conceptual block diagram of HARP (fig. 1), the implementation of the 32-SITP is indicated in more detail in the block diagram in fig. 3.

Each of the 32 sensors is connected to an integrated preamplifier of the current conveyor type [4], which includes a circuit to compensate for detector-leakage current. The addressable analog memory operates in the charge-sensitive mode as discussed before. The addressing is controlled by the “skip controller” which will be described in sect. 3.2. The data are then multiplexed and serially transmitted off-chip. An error detection unit supplies a “fault” flag if problems have occurred and it sends a “loop” signal indicating how many positions in the pipeline are frozen. The chip has fully differential logic inputs and outputs in order to reduce clock feedthrough.

The analog storage cell size is $60\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$. The channel pitch is $100\text{ }\mu\text{m}$ which is large enough for detector connections. The $60\text{ }\mu\text{m}$ depth allows sufficient spacing between the switch lines and the storage capacitor. The size of the skip controller cell on the side of the memory array matches this $60\text{ }\mu\text{m}$. The chip has been manufactured in the $1.5\text{ }\mu\text{m}$ CMOS process of Mietec^(*), which has two polysilicon and two metal interconnect layers. A photograph of the $7.2\text{ mm} \times 6.8\text{ mm}$ chip is shown in fig. 4. The chip has 97 bonding pads and is mounted in a 100-pin grid array package.

(*) Mietec N.V., Oudenaarde, Belgium

3.2 The skip controller

The skip controller in the 32-SITP chip is a new approach to data management. A row of 64 skip controller cells is placed along the memory array and each cell provides the necessary write and erase signals for the column of 32 memory cells which have to integrate the charge in the next “active” clock period for this column. On request, any previous time period that may contain interesting data can be protected, i.e. writing of this column can be skipped. One address decoder is used for indicating the time periods to be skipped and a second one for selecting a protected column for readout.

The skip controller diagram is shown in fig. 5 and the corresponding timing diagram in fig. 6. The skip controller cells are connected as a static shift register ring clocked at 66 MHz. The start pulse with a duration of one clock period is injected by a clocked monostable. Each cell must first provide to all 32 channels an erase pulse (QCL) and then a write pulse (QW) to initiate charge integration. One flip-flop in each cell gives the shift from d to q and sends an erase signal, and a second flip-flop provides an extra shift of one clock period and then sends the write signal. Column n receives a write signal at the same time as column $n + 1$ receives an erase signal.

The skipping function is controlled by the clock manager (clk_mn) which provides the clock signals for the transmission gates in the flip-flops of each skip cell. The clk_mn receives an enable bit which indicates whether that particular column should be frozen or not. Figure 7 shows the master/slave flip-flop with the transmission gates a, b, c and d. During transmission the gates a and d operate together receiving one clock phase, and c and b receive the other phase. However, if the column is protected by a first-level trigger the transmission gates a and b are closed. This causes the pulse at d to be transferred to q without being shifted and hence the column is skipped. Transmission gates c and d are kept open whilst in “skip mode”. Additional logic in the skip cell makes sure that the outputs QCL and QW are disabled during “skip mode”.

The effect of the skip logic control at the level of the analog memory is shown through fig. 8(a)–(c). The squared array represents the analog memory cells organized in locations corresponding to time slots (horizontal direction) and channels (vertical direction). In fig. 8(a), significant data relative to an event are stored in two successive locations of channel i . In fig. 8(b), following the first-level trigger decision, the data corresponding to the event are protected and frozen. Three positions are protected, two which contain the signal charge and one before in order to check the pedestal in case of pile-up. The readout at low speed can start. In fig. 8(c), new data are stored during the readout process of the previous event.

The circuit can accept simultaneous storage of several triggers and organize their corresponding readout. The maximum number of simultaneously stored events is limited by the number of positions in the analog array. If the maximum latency time of the first-level trigger is $1\text{ }\mu\text{s}$, 64 cells are necessary to store events during this latency time. If, for example, 3 locations are protected and skipped for the readout, the number of analog cells has to be 67. The minimum number of locations M needed in each channel can be expressed as a function of the maximum latency time AD [ns] in the formula

$$M = AD/15 + NS$$

with N the maximum number of simultaneously stored events and S the maximum number of adjacent locations that must be frozen for each event. For example, if $AD = 64$ ($1\text{ }\mu\text{s}$ latency period), $S = 3$ and $N = 8$ (can store up to 8 events) then the minimum number of locations needed in the memory is 88.

3.3 Operation of the chip

The operation of the 32-SITP chip can best be described with the help of the timing diagram in fig. 6 for a 3-cell skip controller. A start pulse (ST) is applied, which after passing through the clocked monostable appears at s and triggers the shift register. All enable lines are high (write mode) for the first cycle and then erase and write signals are activated in all cells in succession. Column 2 is then put into “skip mode” for clock cycles 2 and 3, causing $QCL2$ and $QW2$ to be blocked during this time hence unavailable for overwriting. The skipping function can be clearly seen since the Q signals of column 3 now take up the time positions which column 2 would have occupied if it had not been skipped. For cycles 2 and 3 the shift register is 2 clock periods long. Column 2 is then released again and cycles 4 and 5 resume to normal operation before being reset in cycle 6.

This system makes it possible to skip any column within the pipeline and also any number of columns at once. There is a delay caused by the propagation time of a pulse through a skipped cell. This delay can become too long if a large number of consecutive cells are selected for skipping. Detailed system simulations of the detector operation, in particular physics event rate, occupancy, etc. need to clarify the possible limitations. The situation where many cells are skipped has to be investigated so that a minimum deadtime is guaranteed.

The analog memory in the 32-SITP chip might have been organized as a dual port digital RAM (Random Access Memory) via externally addressing for the memory cell to be written or to be read out. Continuously addressing a memory at 66 MHz from an external controller, however, is complex at the level of the board,

and also requires more power to drive off-chip lines. Therefore, as power consumption and minimum crosstalk between detector signals and digital data signals are crucial issues in the SITP front-end design, the memory control is included in each VLSI chip. From the fixed delay between the event and the occurrence of a first-level trigger, it is possible to immediately locate columns of the storage cells which contain the event data, then protect these data from overwrite until the readout is made.

4. ELECTRICAL MEASUREMENTS

Figure 9 shows a typical output from the chip running at 66 MHz, after a charge has been injected in one of the channels. The picture shows the output signal from 32-channels, for 4 successive time slices. The read clock is 2.5 MHz. The channel with an input charge shows an output signal with the typical distribution of charge on 2 consecutive capacitors. The pulse shape is determined by the ICON preamplifier and the write amplifier. The signal-to-noise ratio is affected by the distribution of charge over two capacitors. Possibilities are now studied to increase S/N by putting almost all the charge in one capacitor, or by increasing the gain of the preamplifier. The S/N is optimum when the charge is captured in one clock period, minimizing the parallel noise contributions of the ICON preamplifier [4] and the detector leakage current. On the present chip, the output voltage obtained from a 1 MIP-equivalent input charge (25 000 electrons) is 30 mV.

Fixed-pattern pedestal variations (or fixed-pattern pedestal noise) in one channel is one of the most important parameters. If the pedestal variation is $< 10\%$ of the signal value, there is no need for individual capacitor offset correction. This parameter, together with the random noise of the channel, determines the dynamic range and the absolute precision of the system. The typical pedestal variation among capacitors on one channel is shown in fig. 10 and has a value of 1.4 mV r.m.s. This value is obtained with simultaneous write (66 MHz) and read (2.5 MHz) operations, and the skip function enabled. The measured value is greater than the one expected from calculation (< 1 mV), which did not include some additional parasitic effects on pedestal non-uniformity among cells. One dominant contribution has been identified to be crosstalk between analog and digital inputs/outputs via the ceramic chip package. Other detailed measurements are now under way to analyze the effect of different parameters on the pedestal variations, like the capacitor size, analog switch geometry, layout non-uniformity and proximity of digital functions. Finally, the random noise of the channel is dominated by the noise performance of the ICON preamplifier and amounts to $\sim 2000 e^-$ r.m.s.

The distribution of the overall output offset from channel to channel on one chip is measured as 3.5 mV r.m.s. This value represents the distribution of offsets of the write and read amplifiers in the analog array. It includes large effect variations observed on the channels close to the analog array extremity. This variation is important because it can affect the sparsification efficiency in the case of discriminators placed after the analog storage array, as shown in fig. 1.

Linearity measurements made on one analog memory element show a good linearity (fig. 11) from -2.5 V to $+1.5$ V when using $+3$ V and -3 V power supplies. When including the fixed pattern non-uniformity, the linear dynamic range of the memory exceeds an 11-bit level. The voltage swing is limited towards the positive power supply because of the single NMOS analog switches used in the cell design.

The power consumption of the analog part of the 32-SITP chip with skip logic running at 66 MHz has been measured to be 8.9 mW per channel (including the charge preamplifier, the analog memory and the readout amplifier). The power consumption of the digital part at the 66 MHz clock rate is 78 mW for the complete chip, i.e. 2.5 mW per channel.

5. TESTING WITH A RADIOACTIVE SOURCE

A silicon particle detector chip has been connected to the input of an experimental 4-channel analog memory chip, as shown in fig. 12. The analog memory chip is operated in this test with sequential write and read operation. A second Si detector, aligned with the first, provides a fast-trigger signal if a particle has passed through both detectors in coincidence with the “write” burst. If a trigger is generated during a write cycle, successive digitization of the complete memory content with an external ADC module is enabled. The trigger also starts a TDC in order to measure the time of passage of the particle relative to the end of the write burst, labelling the time or cells where the charge relative to the particle has been stored. After each digitization the values of the charge on all 64 capacitors and the TDC are read by a computer.

Noise, pedestal and gain characteristics obtained in this system with test pulses are in agreement with the electrical measurements. Figure 13 shows a typical waveform as it has been stored in the analog pipeline upon the passage of an electron from a ^{90}Sr source. The write clock was running at 66 MHz. The total charge created in the detector can be obtained by summing the contents of the capacitors labelled for each event by the TDC. The signal occupies in fact two capacitors but since the trigger cannot be synchronized with the write clock, it is still necessary for this test to sum over 3 capacitors. Figure 14 shows the energy

deposition spectrum obtained with the electrons from a ^{90}Sr source. The signal height for the most probable energy deposit corresponds to 30 mV for one minimum-ionizing particle. The pedestal to the left is due to trigger inefficiency from inadequate alignment.

6. CONCLUSIONS

A 32-channel, 64-cell analog memory chip has been designed and fabricated in a commercial CMOS process as a prototype version for an analog front-end VLSI data-acquisition system for the SITP detector. The chip has proven the feasibility of a front-end system including fast preamplifiers, analog storage elements with simultaneous write and read operations and an output multiplexer. It occupies an area of 42 mm² on silicon. The analog data in the addressable memory array is internally managed in an efficient way by a skip logic technique using an on-chip controller. First test results with a radioactive source show the possibility of detecting a single particle signal deposited onto a silicon pad, with a sufficient signal-to-noise ratio, and with a system running at 66 MHz.

The development now continues towards the improvement of the performance for single particle detection and reduction of the power consumption per channel. New functional blocks will be added in the future, like an ADC with 1–5 MHz conversion frequency, an efficient sparse-data scan, a calibration unit and some additional blocks to improve testability and on-line control of the chip. Transfer of this design to a radiation-hardened technology will take place in the future. Test structures are already being fabricated using several radiation-hard microelectronics technologies. Ultimately, the complete system must provide unprecedented performance in terms of channel density, data compaction and power for an affordable cost per sensor element.

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REFERENCES

- [1] A. Olsen, H. von der Lippe, P. Jarron, F. Anghinolfi and E. Heijne, A switched capacitor analog storage line, proc. of the ECFA Study Week, Barcelona (1989) 678 (and CERN report CERN 89–10).
- [2] F. Anghinolfi, P. Aspell, M. Campbell, E. Heijne, P. Jarron and G. Meddeler, HARP: hierarchical analog readout processor with analog pipelining in CMOS, proc. of the Large Hadron Collider Workshop, Aachen (1990) (and CERN report CERN 90–10, Vol. III, 84 and 284).
- [3] F. Anghinolfi, P. Aspell, M. Campbell, J. Dorenbosch, E. Heijne, P. Jarron and G. Meddeler, Monolithic CMOS front-end electronics with analog pipelining, IEEE Nucl. Science Symp. conf. record Vol. 1 (1990) 543 (and preprint CERN/ECP 90–13).
- [4] F. Anghinolfi, P. Aspell, M. Campbell, E. Heijne, P. Jarron, G. Meddeler, J.C. Santiard and S. Buytaert, ICON, a current mode preamplifier in CMOS technology for use with high-rate particle detectors, IEEE Trans. Nucl. Science NS–39 (1991) to be published (and preprint CERN/ECP 91–35).
- [5] F. Anghinolfi, M. Declerq, P. Deval, E. Heijne, P. Jarron, F. Krummenacher and V. Valencic, 1 MHz sampling rate 12-bit low-power pipelined analog-to-digital converter for data processing in particle detectors, Nucl. Physics B, 23A (1991) 389 (and proc. of the Como Conf. 1990).
- [6] V. Valencic, F. Anghinolfi, P. Deval, F. Krummenacher, P. Jarron, E. Heijne and M. Declerq, 1 Msample/s 12-bit low-power pipelined A/D converter, proc. of the Internat. Symp. on Circuits and Systems ISCAS, New Orleans, Vol. 3 (1990) 1360.
- [7] S.A. Kleinfelder, M. Levi and O. Milgrome, Towards a 62.5 MHz analog virtual pipeline integrated data acquisition system, Nucl. Phys. B, 23A (1991) 382 (and proc. of the Como Conf. 1990).
- [8] J. Mochen et al., High-speed analog CMOS pipeline system, Nucl. Instr. and Meth. A288 (1990) 180–186.
- [9] J. McCreary, Matching properties, voltage and temperature dependence of MOS capacitors, IEEE Journ. of Solid-state Circuits, Vol. SC–16, No. 61 (1981) 608.
- [10] C. Michael and M. Ismail, Statistical modeling of device mismatch for analog MOS integrated circuits, IEEE Journ. of Solid-state Circuits, Vol. 27, No. 2 (1992) 154.

Fig.1 Block diagram of the architecture adopted for the SITP front-end signal processing chip.

Fig. 2 Three out of 64 analog memory capacitor cells in charge sensitive configuration with dual-port operation.

Fig. 3 Block diagram of the existing 32-channel chip "32-SITP".

Fig. 4 Photograph of the 32-channel chip "32-SITP".

Fig. 5 The skip controller diagram.

Fig. 6 Timing diagram for the skip controller.

Fig. 7 The master/slave static flip-flop.

Fig. 8 (a) An event is stored on channel i on two time slots.
 (b) Positions are frozen due to a positive first-level trigger.
 (c) New data can be accepted during the readout of a previous event.

Fig. 9 Train of signals from the multiplexed output of the 32-SITP chip. The successive time slices, each with 32 cells, are represented one after the other due to the multiplexing. The charge injected in one of the inputs can be seen in 2 cells which are 32 positions apart.

Fig. 10 Pedestal distribution for 4 channels on the 32-channel chip.

Fig. 11 Linearity curve on the analog memory channel of the 32-SITP chip.

Fig. 12 Test set-up of the 4-channel analog memory chip connected to a silicon detector, irradiated with a radioactive source.

Fig. 13 Output of the 4-channel analog memory after an electron has been detected.

Fig. 14 Energy deposition spectrum for electrons from a ^{90}Sr source measured with a silicon detector connected to the 4-channel analog memory chip.