The Design and Function of a Radiation Tolerant Silicon Tracker for an LHC Experiment

CERN Detector R & D Collaboration RD-2, presented by S.J. Bates¹

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We present a description of the RD2 design for a silicon tracking detector and discuss its function as an integrated component of an LHC experiment. An advantage of the design is that considerable flexibility is possible in the granularity and radial position of each plane; these parameters are determined by the physics requirements as well as by the radiation environment, engineering and electronics considerations. The simulated performance of the detector is discussed and our experimental investigations of irradiation effects are summarised. The development of an analogue pipe-line and related front-end electronics for the storage and processing of the signals is described. Our work indicates the suitability of silicon as a detector for LHC experiments.

1. INTRODUCTION

The high luminosity at the LHC and the required detection of signatures of both expected and unexpected rare physics processes impose severe constraints on any tracking detector. We have studied the relevant aspects of silicon detectors and present our results which lead to a viable design (SITP) for a tracking detector for the proposed Eagle/Ascot experiment [1]. More details have been presented elsewhere [2]. We assume that the detector will be integrated

into one of the Eagle/Ascot designs which includes a liquid argon electromagnetic calorimeter and an embedded cold preshower. The SITP would then perform as an outer barrel tracker, used

- i) as part of a combined central tracker with other systems,
- ii) as part of the electron identification by track preshower matching, and
- iii) as part of the muon identification by providing the crucial measurement of the muon entry point to the calorimeter material.

In the event of a warm EM calorimeter being the preferred option, the SITP layout can be easily reconfigured to provide a precision preshower layer (see the original SITP proposal [3]). Many studies have in fact been made with this configuration.

2. DESIGN

An advantage of the SITP design is that considerable flexibility is possible in the granularity and radial position of each plane. We assume here that the radial space from 65 to 115cm is available for the outer barrel tracking. In this design the tracker consists of 6 detector layers, arranged as 3 superlayers with radii 70, 85 and 100cm. (Figure 1). Each layer contains crystals that overlap in both ϕ and z , giving hermetic coverage. A further 5-10cm of space before the calorimeter will be occupied by a polythene moderator, which will be required to reduce the damage levels from neutrons to the silicon detectors (see below for the radiation tolerance expected) and also to the electronics of all the detectors in the central cavity.

Two types of detector are foreseen, currently 2.4cm square and of 250 μm thickness. Strip detectors have 64 strips with a pitch of 375 μm , while pad detectors have 64 square pads of 3mm by 3mm. The strip geometry is likely to be of 200 μm strips on 5cm crystals in the case of an outer-tracker layout. In this configuration, the strip detectors give measurements of r - ϕ with a 60 μm precision, and a z precision of 15mm. The pad detectors have a z measurement precision of 1mm, thereby reducing the overlap area for ambiguous hits. In this design the tracker covers the z range from -125 to +125cm, giving a total silicon area of 80 m^2 with $8.7 \cdot 10^6$ readout channels.

The material per layer would be 1.5-2% of a radiation length (4% per superlayer, 12% total) at $\eta = 0$, if a conventional copper multilayer board readout is used. It will be possible to reduce this figure if novel fibre-based readout schemes can be used. Such schemes are under investigation.

Fig 1: An Eagle/Ascot design showing the barrel tracking

3. SIMULATED PERFORMANCE

One great advantage of silicon detectors is their high efficiency, measured in test beams to be $> 99\%$ for tracks crossing 250 μm of material. One must nonetheless design for some inefficiency due to bad electronics channels, or connection problems. In addition, activity near tracks, created by secondary processes in preceding material, can render some space points useless. For these reasons our benchmark design contains 3 superlayers, each measuring both ϕ and z . This allows a track vector to be reconstructed in the event of a point being lost.

Studies have been made for the outer barrel tracker, assuming that it is preceded by an

inner tracker containing 4% of a radiation length of material.

For isolated hadrons, the momentum resolution using the outer tracker alone with 3 layers of 200 μm strips and a transverse vertex precision of 20 μm , is

$$dp_t/p_t = 1.5p_t(\text{TeV}) \oplus 0.004\sqrt{(\sin \theta)}$$

where the second term is the multiple scattering contribution added in quadrature. Although the momentum resolution is considerably improved by combining the information of all tracking detectors, the resolution is adequate using the SITP detector alone.

While the tracking efficiency for isolated hadrons is close to 100%, the presence of material significantly reduces the identification and measurement capability for low- p_t electrons. Table 1 shows the efficiency of electron identification. A mono-energetic electron is traced through the full apparatus. The calorimeter energy used as a level 1 trigger is then reconstructed as a cluster (80 MeV cell cut) using an adjacent-side algorithm, and an rms radius evaluated. A search is then made for reconstructed tracks pointing to the cluster, using the following 3 cuts:

- a requirement on the cluster radius of less than 1 cell unit in both the η and ϕ directions [isolation cut, cut a],
- a requirement that the reconstructed calorimeter energy is within 3σ of the peak energy assuming a calorimeter resolution of $0.1\sqrt{E}$, [correct-energy cut, cut b]
- the reconstruction of a unique 5- or 6- point track pointing to the cluster within a window of $d\eta \times d\phi = 1.5 \times 4.0$ cell units about the cluster centroid [track-cal match, cut c].

The main loss results from the calorimeter selections on the electromagnetic cluster and from accompanying (correlated) track activity caused by earlier material.

Table 1
Electron Identification Efficiency, including Calorimeter Selections.

CUT	Energy (GeV)		η
	10	40	
a	.96	.99	0.
	.92	.99	1.2
a+b	.94	.99	0.
	.88	.98	1.2
c/a+b	.99	.99	0.
	.98	.99	1.2
a+b+c	.93	.98	0.
	.86	.97	1.2

Figure 2 shows a two jet event which passes the level 1 electron trigger, with a 76.7 GeV/c p_t electron on one side. This electron is successfully found by the pattern recognition software. Other high p_t tracks are indicated by straight lines linking the inner and outer detectors. More recently, it has been shown that the pattern recognition efficiency is unaffected by the addition of an average 60 minimum pileup events.

Electron bremsstrahlung in the inner material also causes a deterioration in momentum resolution for some fraction of events. Figure 3 shows the reconstructed inverse p_t for generated 1 TeV and 40 GeV p_t electrons at $\eta = 0$. At lower energies bremsstrahlung effects become important, emphasising the need to reduce material both within and before the outer tracking layers.

Subsequent work has shown that the electron efficiency can be improved by performing an "electron fit" in which the effect of a discrete bremsstrahlung is allowed for in the track fit. With this electron fit, the overall electron identification efficiency $\epsilon \sim 95\%$ for electrons with energy above 10 GeV and the high tail in figure 3 is greatly reduced.

Fig 2: An electron in a 2 jet event successfully found by pattern recognition software.

Fig 3: Reconstructed inverse p_T showing how bremsstrahlung effects due to tracker material are important. (The abscissa units are normalised to the appropriate energy).

4. ENGINEERING

Several engineering options are being considered to assemble the crystals as a full-sized detector. One such option is described below. Issues being studied include:

- the electrical and mechanical contact of the crystals and associated electronics, with a required crystal precision of less than $60 \mu\text{m}$,
- the assembly of this motherboard on a support cylinder, and
- the electro-mechanical aspects of signal readout (see below).

Alignment will be needed to a level of less than $60 \mu\text{m}$. Crystals will be mounted in a tile structure onto a circuit board (Figure 4a). Nominally 64 counters are considered per board. The mask pattern of each crystal is known to better than $5 \mu\text{m}$, and can be aligned with respect to known fiducial points to this level. These boards will then be mounted either directly on the support cylinder or onto intermediate modules of length 125cm, using precision drilled holes, and checked by travelling microscope. In this latter case, the assembled modules would be mounted on the support during final installation. Finally a track based alignment will be used since the number of modules is small.

A double layer of counters (see Figure 4b) will be mounted on each side of the carbon fibre support sandwich (approx. 1mm equivalent carbon fibre), and the mass of each layer will be approximately 150 kg. The 3 support tubes will have reinforcement flanges at each end, and will be mechanically linked to maintain a static deformation of less than 1mm.

The major issue to be faced is not initial alignment but rather the alignment stability. This is especially crucial given the possibility of detector operation at low temperature to minimise the effect of bulk radiation damage in the detectors (see below). The board mounting must take account of thermal dilation, and the different expansion coefficients of component materials. Tests are planned to measure the reproducibility of a prototype after extended temperature cycling.

Fig 4: Layout of silicon counters on an SITP module, showing the tile structure and the arrangement of modules on the support structure.

Cooling may be provided by circulating an inert fluor (for example Fluorinert FC72) through cooling pipes built into each module. The pipes have an internal cross section of $\sim 1\text{mm}^2$, and will directly contact the silicon crystals and the electronics chips. Silicon counter operation below 10°C is assumed. Assuming a power of 5 mW per channel, the estimated cooling power of 1 kW m^{-2} is more than sufficient. Prototype tests are in progress.

The full detector will be placed in a gas-tight volume circulated with dry nitrogen and insulated from external heat input.

5. ELECTRONICS AND READOUT

The electronics specifications of the main SITP detector chip foresee the following major elements (blocks) as shown in Figure 5:

- i) A fast ($<15\text{ns}$ risetime) preamplifier operating in charge integration mode with an rms noise <1500 electrons. Good noise performance with detector currents of up to $5\text{ }\mu\text{A}$ per channel.

- ii) Storage of the signal charge on an analogue memory for up to $2\text{ }\mu\text{s}$ (128 cells at a clock speed of 67 MHz). Deviation from stability and cell-to-cell uniformity of the memory cells have to be small ($<1.5\text{mV rms}$) compared with a minimum ionising charge deposition, to avoid calibrations. Charge deposition over two 15ns cells. Asynchronous read/write of the memory with full skip and other control logic.
- iii) A discriminator and a sparse data scan logic block preceding an ADC.
- iv) A final ADC and memory buffer block.

Fig 5: Front end chip architecture

A single chip of approximate area 1cm^2 will be produced with 32 or 64 channels, each having a $2\text{ }\mu\text{s}$ memory and a power consumption of $<5\text{mW}$. A minimum signal to noise ratio of $\sim 10:1$ for a minimum ionising particle is envisaged, even after a full lifetime of operation at predicted LHC radiation levels.

The use of analogue readout electronics is highly desirable in order to monitor the detector behaviour and to give the maximum information on physics events in these severe experimental conditions.

To achieve these design aims, we are proceeding step by step with the successive

electronics blocks. Figure 6 shows the Sr^{90} signal at the output of a 4-channel chip prototype connected to a silicon diode, and operating at a clock rate of 67 MHz.

Fig 6: Time distribution of a source signal at the output of the 4-channel chip prototype (a), and pulse height distribution after integration over 3 time buckets (b).

The preamplifier and memory elements have been successfully merged with close to the required functionality and performance at the intended 67 MHz clock speed. As already noted, we envisage that all the functional blocks should be part of a single chip. The present emphasis is firstly to implement a full working architecture, and secondly to reach the required noise and power specifications, which, together with size reduction will determine the viability of the chip. In addition, the use of fibre optic readout from the board is being investigated. Such readout would be after either the preamplifier or ADC on the chip.

A second major specification of our electronics is resistance to high radiation levels:

~10-20 Mrad charged particle radiation,
~ $2 \cdot 10^{14} \text{ cm}^{-2}$ for neutrons.

Three possible radiation hard candidate technologies are being investigated for the SITP detector. They are the HSOI3-HD process of Thomson-TMS (RD9), the DMILL process developed by LETI-CEA (Grenoble), and the bulk CMOS Harris process being investigated by RAL.

It is intended that the full SITP data be available for a second level trigger. In the case of the mechanics structure described above, a chip would be mounted behind each silicon crystal. Each motherboard would be electrically independent, with digitised signals from each chip being serially transferred via the circuit board to one or more memory buffers. The signals would subsequently be transferred via optical fibre to the data acquisition. The clock signals for each mother board would also be received via optical fibre. Both the electronic and detector bias voltages, however, must be distributed on the board.

6. SECOND LEVEL TRACK TRIGGER

The outer silicon detector can be used to provide a second level trigger on high p_t charged particles. This will be important in the case of electrons as the calorimeter electron trigger will

tend to select π^0 dominated jets. Therefore, false electron candidates can be removed by demanding the presence of a high p_t charged track pointing to the calorimeter trigger cluster. The high p_t track trigger can also be used to help trigger on muons and taus.

This trigger study has been performed with a design for the SITP barrel tracker which differs slightly from the benchmark, by including an extra layer of $r-\phi$ strips at the expense of one layer of pads. This has the advantage of improving the pattern recognition and redundancy for the momentum measurement, at a cost to the z resolution in the case of inefficiency. The best optimisation of the final setup will have to take into account the performance of the trigger, and of the global pattern recognition.

A high p_t track trigger has been simulated using Geant. The algorithm requires at least three out of four $r-\phi$ strip planes in a road to be hit. The road is defined by a width of $2\pi/2064$ radians in the $r-\phi$ plane, which is equivalent to a trigger threshold of about 20 GeV/c. To keep the occupancy low, roads are constructed out of 40 overlapping z slices.

Fig 7: Second level trigger efficiency estimated using the SITP detector to identify a high p_t track associated to a calorimeter cluster.

The efficiency for isolated electrons as a function of p_t is shown in Figure 7. The effect of high luminosity running was allowed for by

adding an average 10 minimum bias events to each electron. The trigger shows a reasonably sharp threshold at 20 GeV/c. The rejection power of the trigger against jets passing the level 1 calorimeter trigger is currently a factor of ~ 100 .

The trigger could be implemented in fast processors or could be done in hardware in a similar way to the ZEUS first level track trigger.

7. RADIATION HARDNESS

The deterioration of detector performance at LHC caused by both neutral and ionising radiation is a major concern. Two categories of damage can be distinguished; bulk damage from either neutral or charged radiation, and damage at the diode surface. We have initiated a study to estimate the neutral and charged particle fluence expected, and to measure the effect of radiation damage. This work is well advanced[4,5]. The final goal is to demonstrate the satisfactory operation of radiation-damaged detectors, under LHC conditions.

The principal cause of bulk damage to silicon detectors by radiation at the LHC is that due to slow (~ 1 MeV) neutrons. Most neutrons occur indirectly as a result of the absorption of hadrons in the calorimeter. A substantial fraction of the energy deposited results in slow neutrons which backscatter into the central cavity of the detector (albedo). This has been our focus of attention so far. Radiation damage is also caused by ionising radiation which causes both bulk damage and surface effects, and these radiation studies will be started during 1992.

A number of inter-related effects lead to a deterioration in detector performance. These include:

- an increase (measured from IV characteristics) in the leakage current under reverse bias, resulting in a higher noise level,
- a decrease in the charge collection efficiency, resulting in a smaller signal, (radioactive source measurements),
- a change in the effective donor

concentration which leads to 'inversion' (the phenomenon in which a detector changes from n-type to p-type) and at high doses to an increase in the full depletion voltage, (measured from CV characteristics).

The expected bulk damage due to neutrons, at the SITP radius, is much greater than that caused by charged particles, and our initial efforts have investigated neutron irradiation to levels beyond those calculated to be reached in the Eagle/Ascot detector at the proposed SITP radius. The predicted neutron fluxes [6], believed to be reliable to within a factor 2, are in the range $2-4 \times 10^{12} \text{ cm}^{-2} \text{ yr}^{-1}$ for the proposed rapidity range; this assumes a 10cm thick neutron moderator which reduces the fluence in the relevant energy range by a factor 10.

Fig 8: Effective doping concentration of a typical silicon detector versus neutron fluence.

The CV and IV characteristics of a silicon diode after neutron irradiation have been extensively investigated. We have shown that the devices can continue to work at LHC levels of

irradiation. When the effective donor concentration N_{eff} is plotted against neutron fluence ϕ_n , the values drop to near zero and then increase again as shown in Figure 8. This is interpreted as an "inversion" of the material from n-type to apparent p-type. We have shown that there is a decrease in inter-pad resistance at the same time but that it still remains high enough for the detector to continue functioning, despite the type inversion. Typical values of interpad resistance at depletion voltage are shown in Figure 9 for neutron fluences up to $\sim 10^{14} \text{ cm}^{-2}$. Little difference in inter-pad resistance was seen between different manufacturers or detector passivation type. Values scale simply with the size and separation of the pads, and thus the measurements are normalised to the same size for comparison.

Fig 9: Interpad resistance for different segmented silicon test structures after neutron irradiation.

All of the types of damage listed above are reduced by annealing, which may occur both during and after irradiation. This self-annealing involves several repair processes, each with a characteristic time constant ranging from minutes to many months. Annealing is strongly temperature dependent. This annealing allows a detector to survive longer when undergoing the

steady irradiation during an LHC operating period. Moreover we have established that the annealing takes place to the same extent when a detector which has been irradiated while cooled as far as -20°C is subsequently warmed up. This would allow a detector which is cooled during operation to recover during relatively infrequent periods at room temperature and continue operation when cooled again.

Self-annealing corrections are therefore necessary to predict the behaviour in real operation [7]. At an operating temperature of -20°C most self-annealing processes are frozen out, and so the detector will recover from radiation damage during scheduled shutdowns at room temperature. Figure 10 shows the depletion voltage over 10 years of operation at LHC estimated according to the following scenario:

- i) Initial diodes of $5\text{ K}\Omega\text{ cm}$ with a thickness of $250\text{ }\mu\text{m}$,
- ii) A 100 day run per year, followed by 20°C annealing for 265 days,
- iii) A neutron-fluence of 10^{13} cm^{-2} per year (ie. a factor 2 greater than the latest prediction).

Figure 11 shows a similar estimate for the leakage current. For the calculations, actual measured damage constants and self-annealing parameters are used. In both figures the solid line shows operation at $+20^{\circ}\text{C}$ whilst the dotted line shows operation at -20°C . This cold temperature value was chosen for simulation some time ago, it now looks likely that operating temperatures will be in the range $0-10^{\circ}\text{C}$.

The cold operation gives an advantage in the case of the leakage current, although the warm operation value of $2\text{ }\mu\text{A}$ per pad still meets the performance specification for the noise. The depletion voltage is higher during cold operation because of less self-annealing but even the maximum value of 170 volts is within the operating capability.

We note however that the above results are for neutron damage alone, and ignore possible annealing effects with time constants greater than 6 months. They also do not consider possible charge trapping effects at low temperature.

Fig 10: Predicted depletion voltage during 10 years of LHC operation (solid line: irradiation and annealing at $+20^{\circ}\text{C}$; dotted line: irradiation at -20°C and annealing at $+20^{\circ}\text{C}$).

Fig.11: Predicted leakage current during 10 years of LHC operation (as for Fig.10).

The charge collection after high neutron fluences has been studied and results presented in these proceedings [8], where after a neutron fluence of 10^{14} cm^{-2} , at a bias of 160 volts and integrating over 20ns the charge collected from relativistic electrons is still 90% of that collected before irradiation.

8. CONCLUSIONS

Our interim results have shown that silicon is a suitable detector medium for an outer tracker at the LHC, and that our design meets the performance specifications for the Eagle/Ascot experiment. We can achieve the granularity that simulation has shown to be necessary for efficient electron and muon tracking. A prototype read-out chip incorporating a $2\mu\text{s}$ analogue memory has been manufactured and has been shown to be capable of operating to the required LHC speeds. The use of the readout for a level 2 track trigger is under investigation.

Neutron irradiation studies have so far shown that this detector is capable of operation after 10 years at predicted LHC radiation levels. Long term effects together with charged particle irradiations are now being studied.

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