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THE READOUT SYSTEM OF THE CPLEAR ELECTROMAGNETIC CALORIMETER

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ABSTRACT

A digital readout system for the CPLEAR electromagnetic calorimeter is described. The calorimeter is composed of 2.5 m long mini streamer tubes and pick-up strip boards interleaved with lead converter sheets. The Fastbus standard is used throughout for the electronics. A novelty is the utilization of daisy-chain lines for the fast block transfer mode. A total of 64 000 channels requires 42 Fastbus (front-end) crates to house the 1000 front-end modules, each containing 64 channels. Modern design techniques have been used to achieve the required performance, including the development of two application-specific integrated circuits (ASIC) using CMOS gate arrays.

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1. INTRODUCTION

The architecture of the digital readout system for the CPLEAR (Charge and Parity Violation Experiment at the Low-Energy Antiproton Ring) [1, 2] electromagnetic calorimeter [3, 4] has been optimized for readout speed and the possibility of transferring reduced data sets to a second-level trigger processor [5, 6], which determines shower feet coordinates. The high readout speed has been achieved by a fast block transfer mode using the two pairs of daisy-chain lines available on the Fastbus [7] backplane, and by parallel data transfers from all "front-end" crates to associated processing modules, which all process their respective data concurrently. Data pattern transfers instead of discrete coded channel information guarantee a high readout speed. Masking of unwanted channels is provided for groups of 8 channels. The final readout is performed by a Fastbus master module (CERN Host Interface (CHI) [8]) using a sparse data scan protocol and block transfer mode for fastest readout.

The preamplifier and input circuitry for the front-end module have been designed in SMD technology. Two ASICs (CMOS gate arrays) have been developed: one for the digital delay in the front-end module, and the other for the address calculation in the processing module.

2. GENERAL DESCRIPTION

This section describes the readout chain [9] (fig. 1) starting from the detector.

2.1 Detector

The electromagnetic calorimeter of the CPLEAR experiment (fig. 2) at CERN is of the barrel type with a 2.6 m length, a mean diameter of 1.754 m, and a radial thickness of 0.22 m. It is divided into three 120° sectors of 18 concentric layers with a thickness of 10.6 mm each. Each layer consists of a 1.5 mm lead converter sheet supported by 2×0.3 mm aluminium foils followed by mini-streamer tubes (4 mm $\times$ 4.5 mm cross section, 40 μ m wire diameter) [3, 4], eight of which form a chamber. Chambers are covered by two pick-up strip planes — below and above — which are inclined by $\pm 30^\circ$ with respect to the axis of the streamer tubes in order to provide the z-coordinate information. The high-gain mode of the streamer tubes permits their wires to be read out without amplification, while the strip signals are amplified (gain of 10). The high voltage for each chamber is provided by high-tension (HT) boards, and preamplifier cards are used for groups of 16 strip signals. Both elements are constructed using the surface-mount technology (SMT). Wire signals are transmitted to the front-end modules via twisted-pair cables, one side of the pair being directly driven from the wire, the other is terminated via a 120 Ω resistor to ground. Strip signals are transmitted in differential mode from the driver to the preamplifier.

2.2 Front-end module (CRAM)

The front-end modules — calorimeter receiver and memory (CRAM) modules [10] (block diagram in fig. 3) — contain 64 channels of input receivers, discriminators, shapers and digital delays and the circuitry needed to read out these channels with the block transfer daisy-chain protocol. Four input channels are grouped on a surface mount receiver (SMR), each channel consisting of a receiver, a discriminator and a shaper. The input signal range is $2.5 \text{ mV}_{\text{pp}}$ to $25 \text{ mV}_{\text{pp}}$ which is similar to that of the readout system used for testing the calorimeter prototype [11]. The digital delay is an ASIC (sect. 3) called DDAR (digital delay and register) and is composed of 16 channels of derandomizers, 16 shift registers (20 cells deep) and 16 output register cells. Additional features are selectable after-pulse cancellation times and selectable acceptance windows for the output register which is updated with each trigger signal. The clock frequency ($\leq 33 \text{ MHz}$) for the DDAR determines the delay time (table 1).

Clock and trigger signals, as well as the threshold voltage, are provided via the special Fastbus crate controller CPT (calorimeter pattern transmitter, sect. 2.3). A "hit group pattern" byte formed by ORing 8 outputs of the DDARs, yielding an 8-bit pattern per CRAM, provides a reduced data set. This is required for the address calculation in the processing modules (sect. 2.4) and for the second-level trigger processor. In order to facilitate the testing of the front-end electronics, the following features have been implemented: test pulses to the inputs of the preamplifiers and HT boards, test pulses to the SMR circuits, setting of odd and/or even channels at the output registers of the DDARs.

2.3 Special CPT crate controller

Up to 24 CRAM modules in a Fastbus "front-end" crate are read out via a special CPT crate controller which makes use of the two daisy-chain line pairs (left and right) available on the Fastbus backplane in order to obtain a short readout time. The left-to-right daisy chain controls the readout of hit group pattern (HGP) bytes from groups of four CRAMs in such a way that they form a hit group pattern word of 32 bits (fig. 4). Thus, a crate with 24 CRAMs will provide 6 HGP words. The right-to-left daisy chain is used for the control of the readout of data patterns (32-bit wide) from lower and/or upper half of a module in a sparse data scan mode; only non-zero data patterns will thus be read out from each CRAM (fig. 5). The readout cycles are controlled by the associated processing module CPM (calorimeter pattern memory, sect 2.4). Data pass under the control of the two daisy chains to the CPM in a strobed (non-handshaked) mode block transfer. In order to reduce the bandwidth requirements on the connecting cables, transfers occur on both the leading and the trailing edges of the strobe signal. Transfer times of 100 ns/word are thus obtained.

Additional features are the detection of time outs for either HGP or data pattern transfers, and of mismatches between HGP and data pattern transfers. The protocol between each CPT and CPM pair is provided via four bi-directional control lines; details on this are described elsewhere [12]. Initialization, setting of odd or even data patterns and start of data transfers are provided via the CPM.

Timing signals such as clock, trigger and test pulses, as well as the threshold voltage received from a central distribution system (CPT driver [9]), are distributed to all CRAMs in a crate via the CPT. The low voltage required for the preamplifiers is provided via busbars situated at special pins on the Fastbus backplane, and passes via the CRAM modules and twisted pair cables.

2.4 Processing CPM module

The processing CPM module (block diagram in fig. 6) connects to the relevant parts via the CPT port, the Fastbus port and the hard-wired processor (HWP) port. Control space registers (CSR) are provided for the functional control (enables, disables, etc.) and data spaces for data storage. It is beyond the scope of this paper to describe all functions in detail, so only highlights will be discussed.

The data reception phase commences with a start signal, received via a front-panel input or a dedicated line from the Fastbus backplane; data (HGP words and data patterns, fig. 5) from the associated CPT are received via the CPT port and terminated by an end-of-block (EOB) control word (timing sequences in fig. 7). The first word of each transfer is the so-called first CRAM address which identifies the first CRAM in a crate. The transfer time is between 3 μ s and 7 μ s depending on the number of data patterns to be transferred; HGP words are always transferred. HGP words are stored in a register file in the RAW-HGP space, data patterns in the RAW memory space. Error messages, such as time out on HGP transfers, data transfers and data mismatch, are received with the EOB. Any error occurring is recorded in a CSR register which, if enabled, provides a service request (SR) signal to the Fastbus master module, which in turn takes the necessary actions.

The masking phase (≤ 800 ns) — removing of unwanted channels in groups of 8 — starts after the reception of EOB, and takes place within the register file, yielding the masked information which in turn is stored in the MASK-HGP space. This function can be disabled via a CSR register. The HOT-HGP space contains the information about the channels to be suppressed.

In the HGP transfer phase which follows, HGP words (transformed to 12 words of 16 bits each) are transferred to the second-level trigger processor via the HWP port, if enabled, taking ≤ 800 ns.

The next sequence is the processing phase or formatting: constructing the intermediate format (fig. 8) from the total RAW-HGP space, MASK-HGP space and RAW space. RAW words of 32 bits are split into 16-bit patterns; only those containing valid (non-zero) information are stored, complemented with the address information calculated via a specially developed ASIC circuit — PERAC [13] (sect. 3). Results are stored in the output memory (OPM) space. At the same time the so-called vernier at least one hit in 8 consecutive channels — information (16 bits) will be stored in the VERNIER memory. It can be requested via the HWP port and provides the precision information for shower feet coordinates (sect. 6). Additional bits stored in the OPM space provide information for data reduction which takes place during the final readout phase. The processing phase takes between 3.2 μ s and 24.3 μ s depending on the number of 32-bit patterns to be treated.

A front-panel daisy-chain signal indicates the completion of the formatting. This signal, if chained through all CPM modules, provides a trigger signal via the calorimeter timing controller (CTC) [9] module for final readout. The CHI requests information from all CPM modules using the T-pin scan [7] and constructs a list of non-empty stations. Thus, only non-empty CPM modules will be accessed in block transfer mode. Further data reduction is achieved during the block transfer by selecting from the 16-bit patterns of the OPM space only those 4-bit patterns which contain hits and which are not masked (using a PERAC circuit). This final data format (fig. 8) contains two 4-bit patterns including addresses and CPM station information in a 32-bit word. The target readout time is ≤ 1 ms for ≈ 200 words transferred from ≈ 25 CPM modules containing data. All CSR registers and all data spaces can be verified by read/write operations.

An additional feature — provided by a piggy-back board on the CPM — is the calculation of 8-bit multiplicities which are stored in the MULT data space. This is made concurrently with the processing phase. The multiplicity information is read out via the HWP port.

Special signals, such as "start" and "abort", are distributed via the CTC to all CPM modules in a crate. The abort signal, generated by the trigger control [14], will terminate the processing phase. A subsequent start signal restarts the CPM, commencing with the reception phase. No special reset sequence is required. Additionally, if the processing phase is terminated without receiving an abort signal, and if no readout is requested via the CHI due to a second-level trigger decision, a following start signal restarts the CPM as mentioned above.

2.5 Data structuring by the CHI

The CHI adds data structuring information — header information for the data acquisition (DAQ) system, total word count, etc. — to the event data block which is

copied in DMA (direct memory access) mode into a special data transfer module (FVSBI [15]). The FVSBI data space is part of the event-builder memory. The complete DAQ system is described elsewhere [16].

3. DEVELOPMENT OF APPLICATION-SPECIFIC INTEGRATED CIRCUITS (ASICs)

Two ASICs were developed for the readout system described: the DDAR circuit (2600-cell gate array) and the PERAC circuit (540-cell gate array). They were described with the assistance of an ASIC design house (Eljapex, Switzerland), which provided the translation of the schematic diagrams using elements of CMOS gate array libraries of Fujitsu (Japan), as well as simulation runs and tests required by the manufacturer. Test vectors and test sequences were defined by the designers. The designs were verified using simulations before and after the layout stage. Tests of prototype samples completed the design phase. More than 4500 DDARs and 700 PERACs have been produced. The PERAC circuit is also used in another part of the CPLEAR experiment [17].

4. CONCLUSIONS

We have designed a large digital readout system — 1000 modules in 42 crates containing 64 000 channels — using the Fastbus standard. The digital delay, adjustable by changing the clock frequency, provides a long decision time (delay = 740 ± 20 ns, acceptance width = 120 ± 20 ns). Short transfer times (100 ns/word) are achieved by using daisy-chain lines for the control of data transfers from front-end modules to processing modules. Parallel data transfers and processing reduce the dead time of the system. Several levels of data reduction (zero suppression) yield a compact data block which is finally sent to the DAQ system.

The digital readout system described above is general-purpose in nature. It could be used in other experiments requiring discriminator electronics for their detectors, such as MWPCs, PMs, etc. The high input sensitivity and the finely adjustable threshold provide excellent discriminating functions. The adjustable delay can be useful for experiments with long trigger decision times. Whether or not the quantification of the input signal is acceptable should be decided on a case-by-case basis. The possibility of receiving quickly the reduced dataset information (HGP words) is ideally suited for experiments with second-level trigger decisions. The built-in test facilities are very useful for debugging and self-checking of the system.

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Table 1 Calculations for delay and acceptance

f_c	clock frequency
$T_c = 1/f_c$	clock period
k	number of cells used for the after-pulse cancellation
n	number of shift register cells (20)
m	number of cells for the acceptance width
ap_w	after-pulse cancellation width
a_c	acceptance width
$ap_w = k * T_c$	
$delay = (n - m/2) * T_c \pm T_c/2$	
$a_w = m * T_c \pm T_c/2$	
Selection used: $f_c = 25$ MHz ($T_c = 40$ ns), $k = 2$, $m = 3$.	

FIGURE CAPTIONS

Fig. 1 Block diagram of calorimeter readout.

Fig. 2 Cross section of the CPLEAR detector.

Fig. 3 CRAM block diagram.

Fig. 4 CPT data formats.

Fig. 5 CPT data block.

Fig. 6 CPM block diagram.

Fig. 7 Timing sequences.

Fig. 8 Intermediate format and final format.

AMP	Preamplifier
CC	Cal. trigger Controller (CTC)
CH	Chamber
CH	CERN Host interface (CHI), P-Card and C-Card
CI	Cluster Interconnect
CM	Cal. pattern Memory (CPM)
CP	Cal. Pattern transmitter (CPT)
CR	CRAM
FE	Front-End trigger proc.
FV	Fastbus VSB interface (FVSBI)
RRO	Root ReadOut [16]

Fig. 1

Fig. 2

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8