EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN-Pre 93018
6 May 1993

SW9322

A new Fastbus-VMEbus interface and its use in the JETSET experiment at LEAR

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Abstract

CM-P00063051

A set of VMEbus modules has been developed, its primary purpose being to provide the experimenter with a high-speed data sink for Fastbus digitisers and a sequencer-controlled interface between Fastbus and VMEbus. One application of these modules is the parallel detector readout implemented for the PS202 (JETSET) experiment at CERN-LEAR. Operation and performance of the new devices as an integral part of the data-acquisition system are described. For a full Fastbus crate loaded with ADCs or TDCs, complete readout and subevent buffering is accomplished within a few hundred μ s.

(Submitted to Nuclear Instruments and Methods in Physics Research A)

1 Introduction

The data-acquisition systems of many experiments in today's high-energy particle and nuclear physics use various electronic bus standards, namely Camac, Fastbus and VMEbus. Although Camac features a relatively low intrinsic speed, it is still widely used for event-by-event operations and in particular for control tasks. For larger-sized experiments, Fastbus provides high-density digitising modules and high-bandwidth backplanes for maximum data throughput. The VMEbus standard with its large number of commercially available processors and memory modules is a good tool with which to collect and organise data from various sources and subdetectors, and to log the complete event data to a permanent storage medium such as magnetic tape.

The simultaneous use of more than one bus standard requires that interfaces be available. For this purpose we have developed two VMEbus modules. One of them [1] is a high-speed VMEbus dual-port Memory, type FPF-223B, which is meant to acquire data from Fastbus digitisers at maximum rate. The other one [2] is a VMEbus-Fastbus input/output Sequencer, type FPF-225B, which allows the VMEbus user to perform event-by-event Fastbus operations efficiently and with very little software overhead, and which gives the experimenter control over the Fastbus segment in a convenient fashion.

These developments were originally initiated to meet the requirements of the PS202 (JETSET) experiment [3, 4] at CERN-LEAR, where front-end Fastbus segments were going to be linked with VMEbus-based data-acquisition computers. In fact, since its complete construction in 1992, the JETSET experiment has successfully recorded physics data, digitised mostly in Fastbus, utilising several units each of the Memory 223B and the Sequencer 225B. Various additional implementations in particle-physics experiments have been made in the meantime. The Memory 223B and the Sequencer 225B are being used in the context of experiments [5] centred around the Omega Spectrometer Facility at CERN-SPS. Several units of the Memory 223B are used in the E813 experiment [6] at BNL-AGS.

Both the Memory 223B and the Sequencer 225B are fast general-purpose devices. In the application described in this paper, the modules are hooked up to the SMI 1821 Fastbus master available from LeCroy. However, the Memory 223B can be connected to any source that provides 32-bit (or 16-bit) data in the form of differential ECL signals. It easily copes with data rates in the 10 MHz range, and besides Fastbus readout our experiment also uses it together with LeCroy's FERA system.

A brief description of the JETSET experiment and its data-acquisition environment is given in Section 2. This is followed by highlighting some features of the employed VMEbus and Fastbus components in Sections 3 and 4, respectively. Operation of the newly developed interfaces in the context of the overall system is detailed in Section 5.

2 Overview of the JETSET data-acquisition system

The JETSET experiment [3, 4] at LEAR studies rare proton-antiproton annihilation channels, which are of special interest in hadron spectroscopy. Examples are $\bar{p}p \rightarrow \phi\phi$ and $\bar{p}p \rightarrow K_S K_S$, where the detected decay channels are $\phi \rightarrow K^+ K^-$ and $K_S \rightarrow \pi^+ \pi^-$, respectively. The experiment is schematically shown in Figure 1. It is installed in the LEAR machine and utilises an internal hydrogen-cluster jet target. The interaction of

the circulating unbunched antiproton beam with the hydrogen jet can provide a high luminosity up to $\mathcal{L}_0 = 10^{30} \text{ cm}^{-2} \cdot \text{s}^{-1}$ and a good resolution $\Delta(\sqrt{s}) \approx 1 \text{ MeV}$ for the final-state mass determination. The interaction region is surrounded by a compact detector system, which is divided into forward and barrel parts. The inner detector comprises 60 scintillation counters arranged around the beam pipe, 2400 high-resolution drift tubes (“straws”) for the recording of charged-particle tracks [7], a 400-wire proportional chamber (MWPC), and 5000 silicon-pad counters for measuring the energy loss of slow charged particles. The outer detector consists of a 5000-cell ring-imaging Cherenkov counter (RICH) providing a velocity measurement of fast charged particles [8], a set of 48 threshold Cherenkov counters for on-line particle identification, a 144-element multilayer scintillator hodoscope, and 350 electromagnetic shower counters [9] made of lead and scintillating fibres (Pb/SciFi). For purposes of normalisation and luminosity monitoring, data on $\bar{p}p$ elastic scattering at large angles are recorded in parallel with the main physics channels.

The first-level on-line trigger is based on the multiplicity of charged particles, on the discrimination of particle types $\pi/K/p$, on photon multiplicity, and on the specific event topologies of the reactions under study. At peak luminosity, the total $\bar{p}p$ interaction rate is $N_0 = \mathcal{L}_0 \cdot \sigma_{tot}(\bar{p}p) \approx 10^5 \text{ s}^{-1}$. As an example, the on-line trigger used for $4K^\pm$ final states falling into the region accepted by the detectors reduces this rate by roughly a factor 1000. Since the experiment records several trigger types simultaneously, the non-gated event rate at peak luminosity is typically of the order of 200 Hz with nearly 100 % duty cycle of the LEAR machine.

A decision of the first-level trigger logic can be produced within about 250 ns after the *physical* occurrence of an event (i.e., to be more precise, after arrival of the signals at the electronics input). The trigger output provides a strobe to various parts of the experimental electronics, thereby initiating the conversion and subsequent readout of the digitised data. The detector readout is performed by means of four front-end computers working in parallel. Each of them reads data belonging to a subdetector of the experiment, hence each computer produces a so-called “subevent”. The latter are sent to the “event builder”, where the subevents from the four front-end computers are combined to give a single “event”. The complete event data are then passed to a fifth local computer. This one writes all data to cartridge tapes for off-line analysis, and it also sends a fraction of the data to a VAXstation cluster for immediate analysis. A general layout of this data-acquisition system [10] is shown in Figure 2.

Each of the four front-end computers fulfils all tasks related to the particular subdetector to which it is attached. They are, for instance, responsible for the correct initialisation at start-up time, such as verification of high-voltage values and down-line loading of discriminator thresholds. The main purpose of a front-end computer during the experimental run is to function as an integral part of the complete data-acquisition system. But it can also operate as a stand-alone acquisition system for that subdetector, which is conveniently exploited during the setting-up phase of the experiment. The front-end computers also perform their own monitor tasks. To this end, histograms specific to its subdetector are filled and stored in local random-access memory (RAM).

The decentralised use of several front-end computers provides flexibility, but it also adds complexity to the overall structure of the system. Therefore, standards must be set and obeyed, in terms of frameworks for data acquisition and data flow, in order to facilitate integration. All front-end computers are based on the VALET-Plus system [11] developed at CERN. This is built around a standard central processing unit (CPU) of the

M680x0 microprocessor family. It runs under a resident monitor and debugger program, called MONICA, which provides support for assembler as well as high-level languages. User programs for this system are most conveniently written in the interactive language named PILS [12], which can be run in either one of the interpreting or the compiled mode. The VALET-Plus additionally includes a number of program libraries, such as standard routines for accessing peripheral equipment in VMEbus, Camac or SCSIbus, and for histogramming or graphic display. The framework for data acquisition and data flow in the VALET-Plus environment is provided by a modular program package called SPIDER [13]. This takes care of run control, interrupt handling, buffer management, event formatting and optional data recording.

A total of five VALET-Plus systems is used in the JETSET experiment. Four of these act as front-end computers that produce data coming from the subdetectors: (a) scintillator hodoscopes and electromagnetic shower counters; (b) Cherenkov and RICH detectors; (c) drift-tube ("straw") chambers and a proportional chamber; (d) silicon-pad detectors. All four subevents are collected in an event builder [14]. For this purpose the experiment uses three transputers, which are housed in and driven by a personal computer. Each of these transputers (INMOS T800) has four serial links operating at 20 Mbit/s, which are designed for communication with other transputers and processors. A powerful feature of such a transputer array, namely its possible expansion into a parallel or tree-type structure for higher-level trigger decisions, has not yet been exploited in the JETSET experiment. At present these links are just used to receive subevent data from the four front-end VALET-Plus computers, and to pass the complete event data to the tape-writing fifth VALET-Plus system. The latter logs all information to a SCSIbus cartridge-tape station (StorageTek 4280). In addition, events can be transferred to a cluster of VAXstations for display and further analysis. An Ethernet connection and a technique [15] known as "remote procedure call" (RPC) is employed for such data transfers.

Six Digital Equipment VAXstations together with five VALET-Plus systems form an Ethernet "local-area network" (LAN). This implies that one can remotely access the VALET-Plus computers basically from any terminal. Other links, for instance to read LEAR beam characteristics off the accelerator's data base, can be easily established as well. The purpose of the VAXstation cluster in the JETSET data-acquisition system is manifold. Its central node is a file server, from which user programs are down-line loaded to the VALET-Plus systems before the actual data acquisition can begin. It is also the target for complete event data sent by the tape-writing computer during runs. The central node buffers these data and distributes them to satellite nodes, for which the MODEL management and control environment is used [16]. Data analysis can be performed on any node of the cluster without interfering with the actual data-acquisition procedure. This includes one- or two-dimensional histogramming of subevent data taken with any one of the front-end computers, graphics display in different projections and evaluation of complete event data, as well as more complex tasks like running the whole off-line analysis program of the experiment.

Overall run control for the system is provided by a program called MASTER that runs on any one of the VAXstations [10]. It synchronises begin and end of experimental runs on all VALET-Plus systems, and it passes messages pertaining to run status or error conditions. For example, in the "begin run" procedure an RPC is made to each "subdetector service routine" down-line loaded in the four front-end VALET-Plus systems. These execute appropriate initialisation codes and confirm their successful start-up by

means of an RPC to the MASTER program. The latter then issues an RPC to the program running in the tape-writing VALET-Plus system, which responds by removing the global “Busy” signal from the trigger electronics, so that physics-data taking is enabled.

3 VMEbus data-acquisition components

The most complex subsystem is that one handling data from the charged-particle tracking chambers of the experiment, which includes “straw” drift-tube chambers and a proportional chamber. It is an example combining VMEbus, Camac and Fastbus equipment. The drift-time and charge-division readout of 2400 individual “straw” drift tubes [7] constitutes the genuine motivation for the new developments reported here. Figure 3 shows this subsystem in some detail. Owing to a novel multiplexing scheme, the number of electronic readout channels is much smaller than the number of drift tubes.

All VMEbus modules employed in the JETSET data-acquisition system are housed in five standard 21-slot VMEbus crates (CERN-Spec. V422), each of which is equipped with an additional J2 backplane to provide full access to the 32-bit data field. The implementation makes use of processor and memory modules, as well as of various link modules to peripheral equipment, and it comprises the following items (for technical details see Refs. [1, 2, 17, 18, 19, 20, 21]).

- For monitoring of the VMEbus backplane activity the VMDIS 8003 Display and Diagnostic Module from CES is used.
- The heart in each VMEbus crate is the FIC 8230 Fast Intelligent Controller from CES. This is a 32-bit real-time processor module built around the MC68020. It runs at a clock frequency of 16 MHz (or 24 MHz) and is equipped with a MC68881 (or MC68882) floating-point coprocessor. The WE32104 four-channel direct memory-access (DMA) controller allows to transport data between memory and VMEbus at increased speed. Installed on-board are 128 kbyte of static RAM and 4 Mbyte of dynamic RAM, where the latter is used as program work space and for filling histograms. Limited single-board operation of the FIC is possible, because a minimal amount of VALET-Plus firmware is installed on-board in the form of 256 kbyte programmed read-only memory (PROM).
- The VALET-Plus firmware comprises monitor and communication routines as well as the PILS language and a number of program libraries. The bulk of all this resides in a TSVME 204 Memory Board from Tekmis, which holds up to 24 PROM chips with 64 kbyte capacity each.
- The static-RAM module MVME 215-3 from Motorola allows an additional 1 Mbyte of stored program or data information to be accessed very quickly from VMEbus. We use it, for instance, to hold all data relevant for the on-line subtraction of pedestals from digitised amplitude information. Since the module includes a battery backup, the data are retained permanently until overwritten by the user.
- The VALET-Plus system is connected to the local-area network by means of a FILTABYTE 25.2 Ethernet Controller from LRT. This path is used for down-line loading programs from remote disk space to FIC or other VMEbus memory and for transferring histograms or event data from the FIC to one of the VAXstations.

- A full branch of up to seven Camac crates can be accessed by means of the CBD 8210 Camac Branch Driver from CES. A standard branch-highway cable is connected from this unit to the “first” Camac crate controller (type CC-A), as well as from there to the next Camac crate, if any. Our system utilises Camac, for instance, as the source of event-trigger interrupts during experimental runs. The Status-A Module type 155 from CERN is programmed to generate a “look-at-me” (LAM) flag upon receipt of the event trigger, and it also sets the “Busy” signal for the trigger logic until cleared at the end of an event-readout cycle.
- Two VMEbus dual-port Memories FPF-223B are employed to receive 32-bit data coming from Fastbus digitisers over differentially driven 16-bit wide ECL cable links. The Memory 223B has a capacity of 128 kbyte, corresponding to 32768 long-words, which is ample for our purpose. Data received at the Memory’s cable port are latched upon receipt of an accompanying “Strobe” signal. The Memory 223B increments its internal address counter, and it generates an “Acknowledge” pulse which can be used in certain applications (asynchronous handshake) to initialise the next transfer. However, highest-speed transfers (synchronous strobe) may occur with a maximum write frequency above 16 MHz, which is faster than the actual speed of most data-sending devices. After all Fastbus data belonging to a given subevent have been stored, a VMEbus command (A24/D16) reads the actual address-counter information, and subsequent commands (A24/D32) are issued to read the actual data block. Since the Memory 223B has only one address counter, the user must set (or reset) a mode register in order to select the “cable-port write” mode (or the “VMEbus read” mode). In addition to the described operation, the module supports various types of VMEbus read- or write-data cycles (A24/D32 and A24/D16). Single-word access times around 100 ns have been measured (from DS0-1 to DTACK protocol signals). However, the module’s VMEbus port has been optimised for data-read block transfers (A24/D32). During running periods of the experiment we operate the FIC in the so-called “quad-word mode”, where four 32-bit words are transferred per addressing cycle. This leads to average block-mode access times of about 70 ns.
- Communication with and control over the Fastbus segments is accomplished by means of two VMEbus–Fastbus input/output Sequencers FPF-225B. The 60-pin TTL cable port of this module includes a 16-bit wide data bus. In addition there are 14-bit lines for (sub-) address selection and full handshake control of the connected external device. The cable-port bits are mapped in a straightforward fashion onto VMEbus data and address space, where details depend on how the user operates the Sequencer 225B. We have made extensive use of “generic-array logic” (GAL) when designing the module’s main building blocks: a VMEbus decoder, a control section, and a state machine run by a 10 MHz oscillator. Two principally different ways of operation have been implemented in the Sequencer 225B, which make the device both versatile and complex (in our application, the external device used is LeCroy’s SMI 1821 Fastbus master).
 - The genuine “sequencer” or “list-processing” mode invokes an internal sequencer list memory of 8 kbyte capacity, and it comprises five different types of transfer between that memory and either VMEbus or the external device. In this mode, the module’s list memory is assumed to have been loaded, by

means of VMEbus commands (A24/D32) issued at start-up time, with lists that are to be used to drive the Fastbus master. During actual data-taking of the experiment, the execution of such a command list (or several thereof) is ignited by means of the on-line event trigger or, alternatively, under software control. Full handshake between the Sequencer 225B and the SMI 1821 ensures that conditions such as “Wait” or “Active”, which may be due to either side of the link, are properly taken care of. This mode allows to perform event-by-event operations essentially without use of software. Being fast, it is the most appropriate one for data acquisition.

- The “immediate” mode has a single type of bi-directional communication between VMEbus and the cable port to the external device. In this mode, a single write or read command (A24/D16) issued from VMEbus through the Sequencer 225B to the SMI 1821 is executed promptly. The module then behaves in principle like a simple I/O register. Clearly, this mode is sufficient for applications such as system test or initialisation, where speed is not important.
- Each VMEbus data-acquisition crate employs a PTL 8145 Parallel Transputer-Link Module from CES, which provides bi-directional signal buffering and parallel-serial protocol conversion. On the one hand, this unit is connected by means of a flat cable to the FIC’s byte-wide general-purpose port. On the other hand, a differentially driven twisted-pair cable transmits serial information to or from the event-builder transputers at rates of 20 Mbit/s.
- When a data-acquisition system is composed of several distributed front-end computers, like in our case, an active mechanism is required which ensures that the various subevents collected in the event builder and logged to tape belong to one and the same *physical* event. To this end, each VALET-Plus crate attached to a subdetector is equipped with a Cycling Event-Number Module developed at CERN, of which there is one master (CENM) and several slaves (CENS) on a common cable bus. The master module, type 437, generates a 16-bit event number upon receipt of the event trigger. This number is received by all slave modules, type 436, situated on the same cable bus. During event readout such numbers become part of the header in the individual subevent data, and they can therefore be easily checked for consistency in the event builder.
- The complete event data sent from the transputers arrive at the central FIC processor in the tape-writing VALET-Plus crate. The latter contains a second FIC module, equipped with a SCSIbus interface, which readily connects to the cartridge-tape station.

4 Fastbus front-end electronics

All Fastbus modules used in the JETSET experiment are housed in three standard 26-slot Fastbus crates (CERN-Spec. F6852), each of which is additionally equipped with ancillary logic (CERN-Specs. F681D and F6826) and a two-row auxiliary backplane. The commercially available Fastbus modules include nearly 4000 digitiser readout channels and comprise the following items (for technical details see Refs. [22, 23]).

- The SFDM 197 Snoop Diagnostic and Slave Module and the FBM 160 Fastbus Monitor from Struck are used for diagnostic purposes and for display of the backplane activity.
- A total of 13 modules LeCroy 1879 Pipeline Multihit Time-to-Digital Converter (TDC) is used to measure electron drift times in single-wire drift tubes (“straws”) with a 9-bit resolution (512 counts). Each module having 96 inputs, the segment comprises 1248 TDC channels. The TDC 1879 operates in a “common stop” mode, in which the inputs receive their “Start” signal from the drift-tube wires. The common “Stop” pulse is derived over a suitable delay from the first-level event trigger, the latter being available some 250 ns after the *physical* event. The clock frequency used is 500 MHz, so that the time-bin size (least count) of this TDC is $b_{t1} = 2$ ns. Since the detectors give relatively short drift times, the active time range is reduced under software control from its maximum value of 512 down to 160 time bins (320 ns). Assuming that the “Start” signals, the common “Stop” pulse, and the free running TDC clock are uncorrelated, the theoretical measurement error is

$$\sigma_{th} = \sqrt{\sigma_{start}^2 + \sigma_{stop}^2} = \frac{b_{t1}}{\sqrt{6}}.$$

For the used time-bin size of 2 ns, we thus have $\sigma_{th} = 0.82$ ns. The experimental value measured previously [24] is slightly higher, $\sigma_{ex} = 1.0$ ns. All single TDC inputs are buffered and presented at the auxiliary backplane connector. A card is plugged in here, which is part of a custom-made multiplexing scaler system [24]. Up to 16 such cards, handling up to 1536 TDC inputs individually or in hex-groups, are daisy-chained together with a control and display unit. The purpose of this device is to monitor single-wire count rates independent from trigger conditions of the experiment.

- Six modules LeCroy 1875 High-Resolution Time-to-Digital Converter (TDC) are employed for time-of-flight measurements with scintillator hodoscopes and electromagnetic shower counters. With 64 inputs per module, there are 384 TDC channels. The TDC 1875 features a 12-bit measurement precision (4096) counts. Again, the mode of operation is using a common “Stop”, the time reference being derived from the first-level trigger information. The time-bin size (least count) used in this case is $b_{t2} = 50$ ps.
- A total of 22 modules LeCroy 1885F Charge-to-Analog Converter (ADC) is used to measure the charge-division information from “straw” drift tubes (14 modules), dE/dx information from scintillator hodoscopes and luminosity-monitor counters, as well as neutral-energy information from electromagnetic shower counters (8 modules). Each ADC 1885F having 96 inputs, there are 2112 individual ADC channels. The two charge ranges in the ADC 1885F feature a 12-bit measurement precision (4096 counts). Depending on the detector type actually connected to an ADC, the charge-bin size (least count) used is $b_{q1} = 400$ fC or $b_{q2} = 50$ fC, and the width of the “Gate” signals is as long as 400 ns (drift tubes) or less than 100 ns, respectively.
- In each of the three Fastbus crates, a LeCroy 1810 Calibration and Trigger Module (CAT) is employed to help integrating the various time- or charge-digitising modules

into a coherent system. The CAT 1810 synchronises testing of TDCs and ADCs, their initialisation at system start-up time, and — most importantly — many of the event-by-event operations during the actual readout in the experimental run. This module receives the common TDC “Stop” and ADC “Gate” signals from the first-level trigger decision logic. The strobes are immediately fanned out via the Fastbus backplane, and multiple strobes within a given event are vetoed by the CAT 1810. After the end of TDC and ADC readout, a “Clear” pulse for the CAT is generated and fanned out to the digitisers, thereby enabling the system for the next event.

- Each Fastbus crate is mastered by a LeCroy 1821 Segment Manager and Interface (SMI). This is a micro-programmed controller and host interface featuring a high intrinsic speed. The SMI 1821 microcode is implemented in the form of PROM or RAM chips, of which one at a time is down-line loaded into the 2 kbyte sequencer control memory. For the application reported here, a somewhat modified version of the standard LeCroy PROM 0.7.1 has been used throughout. The SMI 1821 needs 33 ns for the execution of an instruction, however, this may consist of several actions to be performed in parallel. Most important for event-by-event operations in the actual experiment are complex Fastbus operations, such as “sparse data scan” and double-edge “hardware block-transfer” for highest-speed readout of a whole Fastbus crate filled with TDCs or ADCs. Depending on the digitiser module, the data processed in the SMI 1821 can be subjected to both pedestal subtraction and zero suppression (e.g., ADC 1885F), zero suppression only (e.g., TDC 1875), or they are just passed through because of earlier on-board compression (e.g., TDC 1879). The Fastbus data can be buffered in a 16 kbyte internal data memory of the SMI 1821. Alternatively, and most relevant to our application, the 32-bit data bus of the SMI 1821 is accessed directly and the data are transferred over a ECL cable link with rates up to 40 Mbyte/s (corresponding to 100 ns per long-word) to the dual-port Memory FPF-223B located in a VMEbus data-acquisition crate. Control of the SMI 1821, and down-line loading of microcode, is performed by means of a separate I/O port giving access to eight internal “host registers” of the SMI 1821. In our system, this second port connects to the VMEbus–Fastbus input/output Sequencer FPF-225B. Therefore, the user sees the SMI 1821 host registers simply as VMEbus addresses.

5 Operation of the Fastbus–VMEbus interfaces

A software package for operating the Fastbus front-end systems through the VALET-Plus computers has been written in the PILS language. This includes for instance: a general-purpose library of subroutines for Fastbus operation, VMEFB_LIB; a user program for the determination of ADC pedestal-subtraction parameters, FBAPED_STR; and, most importantly, the “interrupt service routine” of the subdetector concerned, ISR_STRAWS, which handles for all JETSET tracking chambers the actual readout that is to be performed event-by-event, and also the entire initialisation procedure of VMEbus, Fastbus and Camac at system start-up time. In writing the software we have exploited a feature called “aliased arrays” [12], which facilitates the use of shared memory and provides a significant gain in terms of speed. For instance, variables or arrays thereof can be directly mapped onto VMEbus space such as the absolute address of an I/O device. All PILS programs down-line loaded into the FIC are run in compiled mode for highest speed.

The library VMEFB_LIB contains an exhaustive set of subroutines which are used to perform Fastbus operations as driven from a VMEbus device. It includes primitive as well as compound Fastbus operations, such as arbitration, single-listener and broadcast addressing, secondary addressing, T-pin or sparse data scan, single-word and block-mode data transfers. Many routines are specific to the use of LeCroy's SMI 1821 as the assumed Fastbus master, for instance those for initialisation and setting up the pedestal-subtraction pipeline, for down-line loading of SMI 1821 microcode or modifying that code, and for invoking the very fast "hardware block-transfer readout" of a whole crate of TDCs or ADCs (with pedestal subtraction and zero suppression in case of the latter). Each routine typically contains less than ten instructions, which configure the relevant SMI 1821 host registers and subsequently ignite the execution of a particular piece of microcode running in the SMI 1821. We note that the entire program library can be easily coded in the form of Sequencer 225B instructions and stored in the module's list memory.

When the experimental running period is about to start, one determines the pedestal distributions of the "detector-amplifier-ADC" chain using the program FBAPED_STR. This must be done with exactly the same detector and electronics configuration as the one used during physics-data taking. The only difference is that the trigger on *physical* events is replaced during a "pedestal run" by random pulses from an electronic noise generator [25]. In order to avoid as much as possible that a *physical* event occurs in coincidence with a random trigger pulse, the hydrogen-cluster jet target or the antiproton beam should be just off during such pedestal runs. From mean and width values of the measured pedestal distributions we determine the numbers that are to become effective in the SMI 1821 pedestal-subtraction and zero-suppression pipelines. The program writes these values (one for each ADC input and one common threshold value) into the battery-backed static-RAM module.

Data acquisition is preceded by the "begin run" procedures as part of the program ISR_STRAWS, which in this case means to clear and initialise all parts of the tracking chambers' readout system.

- The Camac dataway and attached registers are set up, one of which connects to the Receiver-Memory Hybrid (RMH) crate [26] where the MWPC information is latched and encoded.
- In the VMEbus-based VALET-Plus system, the list memory of the Sequencer 225B is loaded with codes, which are to be executed during actual data-taking of the experiment, in order to prepare the appropriate activities in the two Fastbus segments.
- The two Fastbus segments are initialised one after the other. For the SMI 1821 this includes in particular that the correct microcode be moved from PROM into the control memory, and that the pedestal and threshold values previously stored in the static-RAM module are now loaded into the internal pedestal memory. The CAT 1810 is cleared in order to remove an eventually present "Gate" or "Stop" condition. The series of ADC 1885F and TDC 1879 are configured to have the desired resolution (bin size) and full-scale value (range), and in the TDC case one also chooses a suitable double-pulse resolution. All setting-up of ADCs and TDCs is done by using module-specific broadcast addressing so as to ensure that all digitisers of a given type have the same conversion characteristics.

- Finally, interrupts are enabled and the global “Busy” signal is removed from the trigger electronics.

A valid event trigger in the experiment is assumed to occur at time $t_0 = 0$. It generates a LAM interrupt from Camac, and among other actions this causes execution of EVENT_ISR as the central part of the subdetector’s “interrupt service routine”. A timing diagram of the various actions is shown in Figure 4. The main steps relevant for the discussion here are the following.

1. Execution of EVENT_ISR begins at $t_1 \approx 100 \mu\text{s}$. Some registers are read which characterise the trigger type. Then, commands from VMEbus are issued: firstly, to enable the “cable-port write” mode of the Memory 223B for acquiring data from Fastbus; secondly, to load the memory start-address register of the Sequencer 225B with the location of the sequencer’s command list that is to be executed.
2. As soon as the Fastbus ADCs or TDCs have completed their conversion cycles, which in our application is at $t_{21} = 320 \mu\text{s}$ and $t_{22} = 420 \mu\text{s}$, respectively, each of the two Sequencers 225B receives a “Go” signal. The trailing edge of such a pulse causes the module to switch to its “list-processing” mode. A command list, specific to the readout of Fastbus ADCs or TDCs under SMI 1821 mastership, is executed by the Sequencer’s state machine. In detail this means that, under signal-handshake control between the Sequencer 225B and the SMI 1821, one command every 500 ns may be passed to the I/O port accessing the SMI 1821 host registers. The lists that are used at this point typically comprise not more than 20 elements.
 - (a) The internal data bus of the SMI 1821 is configured for pedestal subtraction and zero suppression (ADC readout) or pass-through mode (TDC readout).
 - (b) A call is made to the SMI 1821 microcode labelled “hardware block-transfer”. This code performs ADC- or TDC-specific broadcast addressing, it decodes the T-pin pattern returned by the Fastbus modules, and it loops through all non-empty digitisers in order to process their data through the SMI 1821 pipeline and finally into the VMEbus Memory 223B. Such data transfers occur at both the leading and the trailing edges of the Fastbus DS-DK protocol signals (double-edge), which results in readout frequencies up to 10 MHz for ADCs and about 6 MHz for TDCs, corresponding respectively to 100 ns or 170 ns per long-word.
 - (c) The Sequencer 225B monitors progress of the described Fastbus crate readout. To this end, it checks the SMI 1821 “Active” status, and it waits until the latter signals the end of its microcode execution, hence completion of Fastbus readout.
 - (d) At the end of the Sequencer 225B list execution all Fastbus signal assertion is cleared.
3. The Sequencer 225B “Wait” status is checked under software control while the state machine is processing its command list according to (a)–(d) above. The duration of “Wait” is 170 μs for ADC readout and about 40 μs for TDC readout, where the latter is shorter because of on-board zero suppression. At $t_3 \approx 500 \mu\text{s}$ one therefore knows that the two Memories 223B contain all data words from Fastbus ADCs

and TDCs. VMEbus commands to these modules are issued: firstly, to disable the “cable-port write” mode; secondly, to fetch the contents of the respective memory address counter.

4. The DMA controller in the FIC is configured for the correct addresses of data source and destination. Subsequent DMA transfers copy the data blocks from either one of the Memories 223B to the SPIDER circular buffer, which takes about $180 \mu\text{s}$ in each case. The entire readout of both Fastbus segments is completed at $t_4 \approx 880 \mu\text{s}$.
5. After MWPC hit-pattern readout, at the end of the EVENT_ISR routine, a number of clean-up operations are performed. In particular, a “Clear” pulse is sent to both CAT 1810. The LAM condition is reset, which also removes “Busy” from the trigger logic. At $t_5 \approx 1.4 \text{ ms}$, the subdetector’s readout system is prepared to take the next event, provided that the other VALET-Plus front-end computers have also removed their “Busy” signals.

The conditions described above refer to “typical” events, where the average amount of tracking-chamber information written to tape comprises about 70 ADC words and 70 TDC words spread over many Fastbus modules. It is worth noting that the total transfer time characterising our new Fastbus–VMEbus link, measured from the Sequencer 225B “Go” signal until the end of Memory 223B block-read, is only 250 to $380 \mu\text{s}$ for each system (referring to TDCs and ADCs, respectively) and $560 \mu\text{s}$ for both systems together. Larger-sized events would add a few hundred ns per word to the quoted times.

The relative rate of event triggers *accepted* by the data-acquisition system can be written as

$$k_{\text{live}} = \frac{N_{\text{acc}}}{N_{\text{raw}}} = \frac{1}{1 + \tau \cdot N_{\text{raw}}},$$

where τ is the total dead-time associated with an acquired event and N_{raw} is the non-gated rate of Poisson-distributed event triggers as *generated* by the fast logic. Taking $\tau = 1.5 \text{ ms}$ for the overall event dead-time, the “live-fraction” resulting from the present running conditions of the JETSET experiment is $k_{\text{live}} = 77 \%$ for $N_{\text{raw}} = 200 \text{ Hz}$ (with essentially 100 % duty cycle of the LEAR beam). An increased luminosity with improved beam and jet intensities is envisaged for the near future, so that the experiment would benefit from the implementation of a higher-level trigger scheme. For the reactions of interest, like $\bar{p}p \rightarrow \phi\phi \rightarrow K^+K^-K^+K^-$, such a scheme may exploit information on charged-particle track multiplicities and transverse-momentum balance.

6 Summary

The VMEbus devices described in this paper have been developed with the primary purpose to provide the experimenter with a high-speed interface between front-end Fastbus systems and VMEbus-based data-acquisition computers. The work load is distributed, because our scheme incorporates separate electronic devices and cable ports for the tasks of control (Sequencer 225B) and data sink (Memory 223B). This appears to be an important feature in view of speedy data-acquisition.

Several of these Fastbus–VMEbus interfaces have been implemented in the JETSET data-acquisition system, where they play a central role for the readout of many subdetectors. The overall system utilises four VMEbus-based front-end computers, which work in

parallel on the readout and processing of subdetector data. The corresponding subevents are combined in the event-builder transputers to give a complete event. This is passed to the tape-writing fifth VMEbus computer for permanent storage.

The function and performance of the new interfaces has been described in the context of that part of the overall system, which is attached to the charged-particle tracking chambers of the JETSET experiment. After the on-line event trigger, the Sequencer 225B drives a Fastbus segment upon receipt of a strobe, and the Memory 223B latches ADC or TDC data sent from Fastbus during T-pin readout at rates up to 10 MHz. This event-by-event operation involves essentially no software overhead. In our application, the total transfer time of compacted data, measured from Fastbus digitisers' "end-of-conversion" until complete subevent buffering, takes only a few hundred μ s for about 1300 ADC or TDC channels located in one Fastbus crate.

Acknowledgements

It is our pleasure to thank Professor Erwin Rössle (Freiburg) for his continuous support. The collaboration with Staffan Ohlsson (CERN) and Paul Reimer (Urbana-Champaign) on various aspects of the JETSET data-acquisition system has been most fruitful and enjoyable. At an earlier stage of the project, valuable help has been provided by Guido Polivka (Basel) during his stay as Summer Student. The work reported here has been supported in part by the German Bundesministerium für Forschung und Technologie.

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Figure captions

1. Plan view of the JETSET experimental apparatus at LEAR. The elements are: 1 = jet-target source; 2 = jet-target sink; 3 = inner trigger scintillators; 4 = barrel and forward “straw” drift-tube chambers; 5 = silicon-pad detectors; 6 = ring-imaging Cherenkov counters; 7 = threshold Cherenkov detectors; 8 = outer trigger scintillators; 9 = electromagnetic calorimeter; 10 = γ -veto counters.
2. Block diagram of the JETSET data-acquisition system. The principal data flow is indicated by arrows. The dotted box encloses the subsystem for readout of the charged-particle tracking chambers.
3. Data-acquisition subsystem for the JETSET charged-particle tracking chambers. Explanations are given in the text.
4. Timing diagram for the interrupt service and readout of tracking subdetectors. All times are given in μs .

Figure 1.

Figure 2.

Figure 3.

Figure 4.