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**DYN1: A 66-MHz FRONT-END ANALOG MEMORY CHIP WITH
FIRST-LEVEL TRIGGER CAPTURE FOR USE IN FUTURE
HIGH-LUMINOSITY PARTICLE PHYSICS EXPERIMENTS**

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*RD2 Collaboration***Abstract**

DYN1 is a 32-channel, 128-cell analog memory with continuous write and read access. The chip amplifies the detector signals and integrates the signal currents onto capacitors within the memory during each bunch-crossing interval. Dense dynamic logic circuitry accepts multiple first-level triggers, freezes the corresponding analog data and stores their addresses in an external FIFO. The triggered data can then be read out at leisure whilst simultaneously sampling and storing new triggered events. A first-level trigger latency of up to 2 μ s is accepted at the maximum LHC clock frequency of 66 MHz. The chip shows an overall gain of 48.2 mV per 25 000 e^- . The mean channel noise is 4.5 mV and the pedestal variation from cell to cell within one channel is 1.9 mV. The total dynamic range has been measured at 4.6 V giving a resolution of 11 bits (0.05%) for the memory itself.

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1 INTRODUCTION

The front-end readout VLSI electronics currently under design for the silicon pad tracking detector proposed for the LHC [1, 2] is based upon the Hierarchical Analog Readout Processor (HARP) analog memory architecture [3, 4]. A simplified block diagram of this architecture is shown in Fig. 1. It consists of four main blocks, namely the analog memory, the memory controller, a zero suppression unit, and an ADC. The latter two blocks provide a reduction of the analog data to hit detector elements only, followed by digitization in preparation for off-chip transmission and eventual board readout. These two blocks are currently being studied in their own right and are not discussed in this paper. The first two blocks however, the analog memory and memory controller, are the main aspects of the DYN1 chip described here.

The function of these first two blocks is to sample and store detector charge during each bunch-crossing interval for a large number of channels, without any dead time. The memory has to be capable of storing all the data received during the period of time needed until the arrival of an appropriate trigger signal, i.e. the first-level trigger. The memory controller defines where in the memory new analog data are to be stored. It also associates the first-level trigger signal with the stored data corresponding to the historic event which initiated the trigger. These data are flagged and must be stored for an undetermined period of time until requested by the zero suppression unit for further processing. Transfer of the flagged analog data to the next block can then proceed independently of the write sequence and at a much reduced frequency.

2 THE DYN1 DESIGN

The main elements of the DYN1 chip are the analog memory and its associated controller. A block diagram is shown in Fig. 2. The chip has 32 input channels which can be either directly connected or capacitively coupled to the detectors. The memory itself comprises a switched capacitor array with a width equal to the number of channels and depth of 128 cells. This enables storage of all the data for up to 2 μ s at 66 MHz*) which corresponds to the working hypothesis for the first-level trigger (FLT) latency in the LHC.

The memory controller is split into two main sections: the Skip Controller and the FLT Capture Unit. The Skip Controller provides the memory with clear and write signals in real time. These clear and write signals run as a continuous loop providing a dead-time-free mode of operation. The FLT Capture Unit captures the first-level trigger and disables the necessary historic time slot from the Skip Controller write sequence, thus protecting the data stored on these capacitors from being overwritten. In order to do this the FLT Capture Unit communicates with the Skip Controller via enable 'e' lines. There is one enable line per column of the memory array, and since the Skip Controller is segmented to match directly to the array, individual segments can be included or excluded from the write sequence. When a segment is disabled the Skip Controller merely misses it out in its loop, i.e. the segment is skipped.

The enable lines also allow the encoder to provide the unique physical position of the triggered time slots. The encoder output is a 7-bit address which is generated for each frozen time slot and successively stored in a FIFO. These addresses remain in the FIFO until the

*) A bunch-crossing frequency of 40 MHz is now foreseen for LHC. This increases the memory storage time for all the incoming data to 3.2 μ s for the same number of cells.

system is ready for readout. Upon a read clock the most ancient address is popped from the FIFO and decoded back to its physical position in the memory. The corresponding column is then made available for multiplexing and serial output through a unity gain buffer. Once the read cycle is complete the enable line is reset and the column is placed back into the Skip Controller write sequence for further use.

All of the above functions are performed on the chip with the exception of the FIFO which is at present external for diagnostic reasons. Future versions of the chip, however, will incorporate the FIFO.

The layout^{*)} of the chip is shown in Fig. 3. It contains approximately 50 000 transistors and measures 8.7 mm by 6.3 mm in total. The channel-to-channel pitch is 100 μm and the column pitch is 40 μm giving a memory depth of 5.12 mm for 128 cells. The digital control logic is segmented to match exactly with the column pitch requiring a very high transistor density. Dynamic logic is used to overcome this otherwise very difficult density problem. Dynamic logic relies on storing the output potential of one gate on the parasitic input capacitance of the following gate, without the use of static feedback latches. Using this technique, one can reduce the number of transistors in the critical path significantly as compared to a static circuit and hence obtain a very dense design. An alternative approach is to share the functionality of one digital cell between two time slots. This alternative technique has also been studied within RD2 and a prototype chip, Analog Pipeline Chip (APC3), has been made and evaluated [5].

2.1 The analog channel path

The analog channel path is shown in Figs. 4(a) and 4(b). The main features of the input stage are determined by the current conveyer (ICON) [6] and its leakage current compensation circuit. Together they provide a low-impedance input node ($\sim 300 \Omega$) and robustness to detector leakage currents of more than 10 μA . This means that the detectors may be connected directly to the input of the ICON, which will be a crucial benefit when designing for a large number of channels both in terms of reduced detector cost and reduced noise coupling to the inputs.

The detector charge is transferred from the low-impedance input node to the high-impedance output node of the ICON. A current amplifier is then used as a gain stage before a write amplifier integrates the current onto a unique switched capacitor within the analog memory. This procedure has become known as CSI (charge sampling integration) [7].

During the read operation the charge stored on a given capacitor is converted to a voltage by the read amplifier. A multiplexer then serializes the discrete read amplifier outputs, producing a chain of analog values. These are then buffered by a unity gain stage before being allowed off-chip.

2.2 The Skip Controller

Figure 5 shows the block diagram of the Skip Controller. There are 128 segments in total, each dedicated to a particular column of the memory and each containing a SKPCELL and SKIPMN. The SKPCELL circuit provides the shifting and skip mechanism whilst the SKIPMN circuit controls whether the SKPCELL is in shift mode or skip mode. Figure 6

*) The chip was fabricated using the Mietec 1.5 μm bulk CMOS process.

shows the SKPCELL and Fig. 7 shows the principle of the shifting and skip mechanism in symbolic form.

Within the SKPCELL a dynamic D flip-flop provides a shift from d to q with q connected to d of the next stage. In this way a standard shift register is created. When a cell is in skip mode the pulse arriving at d passes directly to q without being shifted. The function of the register is to first discharge the capacitors in a particular column with a clear pulse followed immediately by a write pulse on the next clock cycle. The clear and write pulses are therefore in different time periods but must obey a common skip arrangement. To achieve this the SKPCELL uses two flip-flops, one providing a horizontal shift and the other providing a vertical shift. In symbolic form the diagram starts at t_0 with a clear pulse applied to column 1. After one clock period (t_1) the horizontal shift has taken the clear pulse to column 2 whilst the vertical shift has produced a write pulse in column 1. At t_2 column 3 receives a clear pulse whilst column 2 receives a write pulse. At t_3 column 5 receives the clear pulse since column 4 is in skip mode and column 3 has a write pulse. Hence the data in column 4 are completely protected from the clear or write pulses.

2.3 The FLT Capture Unit

The block diagram of the FLT Capture Unit is shown in Fig. 8. It is essentially the same type of dynamic shift register as used in the Skip Controller. Both registers have a clocked monostable at their inputs. A falling edge at ST produces a pulse of one clock period duration which is used to start the registers. Since the first-level trigger latency will remain constant one can create a delay between the Skip Controller and the FLT Capture Unit exactly equal to this latency. The FLT Capture Unit will then perform a coincidence between the first-level trigger and the position in the loop of the circulating pulse. Acting on this result, the FLTRIG cell can latch its enable line and hence put the entire column in skip mode. The FLTRIG cell is shown in Fig. 9.

Also included in the FLT Capture Unit is the DEC+RESETe cell, Fig. 10. The purpose of this cell is to decode the 7-bit address seen at the output of the FIFO, make the corresponding column available for reading, and inform the FLTRIG cell to reset the enable (e) line after reading has finished. The read sequence proceeds with the timing shown in Fig. 11. The address from the FIFO is decoded to a unique position on the rising edge of Readclock which in turn triggers a flip-flop and creates a read pulse to a particular column. The data in that column are then available for multiplexing. Once all 32 channels have been read out, a Readstop signal terminates the read pulse and instructs the FLTRIG cell to reset the enable line, and hence return the column to normal write operation.

3 RESULTS

3.1 Functional measurements

All of the measurements were performed using continuous write and read operation with a write frequency of 66 MHz and a read frequency of 2.5 MHz.

Figure 12 shows the output of three time slots when a signal was applied to one channel. Each time slot includes the serialized values of all 32 channels with the signal clearly seen as a

negative voltage excursion on one of the middle channels. The signal spans three time slots at the maximum frequency indicating total integration of the signal current within 45 ns.

One of the main features of this chip is the ability to cope with fast multiple triggers. Figure 13 shows the output when two triggers (each freezing four time slots) are applied to different sections of the memory before the system has had time to start its read operation. A signal was synchronized to coincide with the second trigger only.

In the unlikely event that many triggers coincide with one section of the memory, it is necessary to find how the system operates when many consecutive columns are placed in skip mode. The theoretical limit is defined by the LHC clock period/shift register delay in skip mode. Simulation showed the shift register cell to have a delay of < 1 ns in skip mode, predicting a maximum number of consecutive skips > 15 at 66 MHz. Measurements have subsequently been done with 15 consecutively frozen columns with no adverse effects.

3.2 Analog measurements

The analog measurements were carried out using the Gollum DAQ system [8] developed by the RD2 Collaboration. This system, which is VME-based and uses LabVIEW^{*)} software, provides a general test bench for analog memories of this nature. For these measurements, the system was used to sum the result of three time slots and also subtract any baseline common-mode interference which may affect the chip. In summing three time slots the signal-to-noise ratio was degraded by a factor $\sqrt{3}$.

Figure 14 shows the distribution obtained from a 25 000 e^- signal and the noise on the same channel. The plot shows a good separation between the signal and the noise, and the gain can be seen to be 48.2 mV per 25 000 e^- . The mean channel noise for a single time slot was measured to be 4.5 mV r.m.s.

The dynamic range for both negative and positive excursions can be seen in Figs. 15(a) and 15(b). The integral non-linearity is better than $\pm 1\%$ over the full scale of -2.8 V to 1.8 V giving 4.6 V total dynamic range. Taking 25 000 e^- to represent charge given by 1 mip, the dynamic range can alternatively be expressed as -60 mip to 36 mip giving 96 mip in total.

The pedestal non-uniformity is defined as the variation of measured values from capacitor to capacitor in one channel without any signal applied. The distribution for these values has a σ of 1.9 mV. This corresponds to a memory resolution in excess of 11 bits (0.05%).

A complete summary of these measurements is shown in Table 1.

*) LabVIEW is a registered trademark of National Instruments Corporation.

Table 1
Summary of conditions and results

Conditions	
Mode	Continuous write and read
Write frequency	66 MHz
Read frequency	2.5 MHz
Input charge for 1 mip	25 000 e ⁻
Measurements	
Gain	48.2 mV per mip
Mean channel noise	4.5 mV r.m.s.
Dynamic range	4.6 V total (96 mip)
Integral non-linearity	< $\pm 1\%$
Pedestal variation	1.9 mV (sigma)
Memory resolution	11 bits (0.05%)
Power consumption	
Analog channel path	8.9 mW per channel
Digital section	292 mW total

4 CONCLUSION

The DYN1 chip has successfully demonstrated the implementation of a dense analog memory in a single VLSI chip with dynamic digital control logic suitable for LHC. The design can be implemented into the full HARP architecture as specified earlier or alternatively could be used in its present form for analog readout of triggered time slots. Operation of the system has been demonstrated at 66 MHz with single or multiple fast triggers with up to 2 μ s trigger latency. Depending on the exact conditions in the application, improvements may still need to be made in terms of noise and power consumption and these points continue to be the subject of present studies.

Extensive work is also being carried out in cooperation with the RD9 Collaboration for the implementation of the analog memory in a radiation-hard Silicon On Insulator (SOI) process [9].

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Fig. 1 The HARP architecture

Fig. 2 Block diagram of the DYN1 chip

Fig. 3 DYN1 layout

Fig. 4(a) Block diagram to show the input stage of a single analog channel

Fig. 4(b) Block diagram to show the output stage of a single analog channel

Fig. 5 The Skip Controller

Fig. 6 The SKPCELL

Fig. 9 The FLTRIG cell

Fig. 10 The DEC+RESETe cell

Fig. 11 Timing diagram of the read sequence. The multiplexer runs at 2.5 MHz giving 12.8 μ s to read all 32 channels of a single time slot.

Fig. 12 Serialized analog output of all 32 channels in three time slots. The scale is $5\ \mu\text{s}$ per division and each scan of 32 channels takes $12.8\ \mu\text{s}$. The result of a negative signal spanning the three time slots can be seen on one of the middle channels.

Fig. 13 Demonstration of multiple trigger possibility. The figure shows the readout after two fast triggers have been applied. Four time slots were stored for each trigger. A negative signal was applied to correspond with the second trigger only. The scale is $20\ \mu\text{s}$ per division.

Fig. 14 Distribution of a 25 000 e^- negative signal and the noise without any signal

Fig. 15(a) Amplitude response for negative signals

Fig. 15(b) Amplitude response for positive signals