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Detectors for High Luminosity Particle
Physics Applications

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Development of Active Pixel Vertex Detectors for High Luminosity Particle Physics Applications *

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ABSTRACT

Pixel vertex detectors are presently under consideration for use in future heavy ion experiments and also at the future LHC and SSC[°] hadron colliders, where they may have more than 1 m² of active area, containing over 10⁸ individually - addressable pixel elements.

The readout electronics for each pixel - amplifier/shaper, comparator and storage element - may be integrated into the detector wafer itself, or be bonded to it in a "hybrid" assembly. Both hybrid and monolithic detectors are under development in parallel programs in the United States and Europe, focussed on the implementation of radiation tolerant detectors and electronics, with high speed, time-referenced, sparsified readout of only the pixels containing information for triggered events. Such "smart" or "active" readout is particularly demanding, requiring "data - driven" architectures.

The recent development and present status of these detectors is reviewed. Their implementation in future high energy physics experiments is discussed.

(1) Introduction

Candidates for vertex and tracking devices at future hadron and heavy ion colliders include gas filled wire and microstrip detectors, scintillating fibers and semiconductor devices built from silicon, gallium arsenide and possibly diamond. At small radius, requirements for extremely high spatial, momentum and multiple track resolution mandate the use of semiconductor detectors. These are being evaluated in both the 1D strip and 2D pixel geometries. While silicon microstrips will find application in the inner trackers at the next generation of colliders, pixel detectors are expected to be superior for vertexing, due to their better ability to resolve pattern recognition ambiguities in the high track multiplicity - and high radiation level - environment closer to the collider beams (§2.1), and due to their intrinsically higher radiation resistance (§2.2).

(2) Constraints on Vertex Detectors at High Luminosity Colliders

(2.1) Event Topologies at high Luminosity Hadron and Heavy Ion Colliders

At the CERN LHC, Beam Cross Overs (BCOs) will occur every 25 ns, (at SSC every 15 ns), with interesting events expected every 1000-10000 BCOs. The proton-proton inelastic cross section (about 60 mb at high energy) will give an average of 20 pile-up events per BCO at the LHC design luminosity of $1.7 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, which though separated in z due to the finite

[°] This review was written prior to the cancellation of the Superconducting Super Collider, late in 1993.

bunch lengths, will need to be disentangled from an event of interest in the same BCO. At the lower SSC design luminosity of $10^{33} \text{ cm}^{-2}\text{s}^{-1}$, pile-up will be less of a problem.

Information in the vertex detector must be "time-stamped" to a precision sufficient to identify the corresponding BCO, so that when its readout is triggered, data from only those pixels with information in the selected BCO is transferred - in less than the mean time between interesting events. In addition to the detector readout time, there is a typical expected delay (or "latency") of about $2 \mu\text{s}$ (LHC) [1] and $4 \mu\text{s}$ (SSC) while a level 1 trigger signal is formed and transmitted to initiate the readout. During a $2 \mu\text{s}$ latency at LHC, 80 more beam crossings will occur. Although data from these BCO's will carry a different time stamp to that of the event of interest, a front end selection of data from up to 1600 overlaid events (each with an average multiplicity of more than 40 tracks) may be necessary every $25 \mu\text{s}$ at LHC. An additional background close to the beams are e^+e^- pairs from bremsstrahlung photon conversion in material close to the beams, which loop in the detector magnetic field, crossing the vertex detector many times. Fortunately the trajectories of such pairs are predictable.

The ATLAS experiment at LHC [1] has a silicon pixel vertex detector as a baseline element of its inner tracker [fig (1)], consisting of two cylindrical sensitive layers at radii 11.5 and 14.5 cm, giving coverage out to ± 1.5 units of pseudorapidity. In many events of physics interest, one or more tracks must be identified within tightly collimated jets of particles. As an example [2], at a distance of 11.5 cm from the LHC beams, the mean 1σ width and population within high P_T jets are 12 mrad and 7 tracks, representing a track density of $\sim 4.5 \text{ mm}^{-2}$; a 9% local occupancy in an array of $(50 \mu\text{m} \times 400 \mu\text{m})$ pixels. For a strip detector of pitch $50 \mu\text{m}$ ($r - \phi$) and $200 \mu\text{m}$ (z) the corresponding occupancies in the orthogonal directions are 25% and 100%, giving a high probability of lost data, and a very serious ambiguity problem.

At LHC, the projected luminosity for heavy ion (Pb-Pb) collisions will be about $1.7 \cdot 10^{27} \text{ cm}^{-2}\text{s}^{-1}$. The high inelastic cross section of 5.5 b will result in a minimum bias interaction rate of about 4000 events/second, with interesting events at about 1-2 % of this rate. Average particle multiplicities per event will be about 8000. The ALICE ("A Large Ion Collider Experiment") collaboration proposes [3] to construct an inner tracking detector with an innermost pixel surface at a radius of 7.5 cm from the beams to resolve tracks in the high multiplicity events.

(2.2) Radiation Effects at the High Luminosity Colliders

The radiation dose expected in the inner layer ($r = 11.5 \text{ cm}$) of the ATLAS pixel vertex detector at an "average" LHC luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ has been estimated [4] to be about 2.5 Mrad /LHC "year" (of 10^7 sec operation). In addition to direct particle flux from beam interactions, a flux of $3 \cdot 10^{12} \text{ 1 MeV neutrons cm}^{-2}\text{yr}^{-1}$ are reflected back into the detector by the calorimeter. The total displacement damage is equivalent to a flux of $8 \cdot 10^{13} \text{ 1 MeV neutrons cm}^{-2}\text{yr}^{-1}$. By comparison, at a distance of 5 cm from the SSC beams at nominal luminosity of $10^{33} \text{ cm}^{-2}\text{s}^{-1}$, the radiation dose is estimated to be about 1 Mrad/year [5].

Minimum ionizing particles generate an average of 80 electron - hole pairs per μm of silicon traversed. In a typical silicon microstrip geometry, (width $50 \mu\text{m}$ and typical length

6 - 12 cm) an equivalent noise charge $\sim 1500 e^-$ rms is expected at the amplifier input due to the combined effects of strip capacitance and amplifier noise.

The minimum practicable thickness for silicon microstrips is generally considered to be $300 \mu\text{m}$, giving a signal to noise ratio in the range of 10 - 20. By contrast, the very small capacitance of pixel detectors (which have areas typically 200 times smaller) affords them much lower noise, and a correspondingly higher signal to noise ratio than in strips of the same thickness. With low noise electronics [$\sim 100 e^-$ rms], pixel detectors commonly deliver signal to noise ratios in excess of 100. This makes it possible to thin the pixel detector from $300 \mu\text{m}$ to, say, $150 \mu\text{m}$ to reduce its contribution to multiple Coulomb scattering. This also enhances robustness under irradiation.

Extensive studies have been made (for example ref [6]) of the behavior of silicon microstrip diodes under irradiation. The performance of silicon pin diodes becomes degraded at high radiation levels mainly as the result of two effects:

- (i) an increase of leakage current, with a corresponding reduction in signal to noise ratio:
- (ii) a change in effective doping concentration, leading to a progressively more p-type material. A progressively higher bias voltage is required to deplete the detector, which is ultimately limited by the maximum depletion voltage that can be applied without breakdown.

These effects set a limit on the operational life of a detector, dependent on its thickness, its distance from the beams and the collider luminosity. The lifetime seems also dependent on the detector temperature during the irradiation cycles, and on the storage temperature between these cycles. Thermal effects are still the subject of investigation; the optimum temperatures are not yet known, and it is too early to predict with certainty the expected lifetimes of microstrips at various distances from the SSC and LHC beams. While silicon pixel detectors are subject to the same damage processes, they are expected to be able to survive longer in a high radiation environment due to:

- (i) the smaller initial leakage current and noise afforded by their much smaller area:
- (ii) their possibility of being thinned below $300 \mu\text{m}$; halving the detector thickness reduces the required depletion voltage by a factor of four.

Close to the circulating beams however, front end electronics is equally vulnerable, whether for the readout of strips or pixels. For this reason, several radiation hard electronic technologies are being actively investigated (3.1, 3.2) for implementation at SSC and LHC.

(3) Development of Hybrid-Bonded Pixel PIN Diode Detectors and Readout Electronics

(3.1) The US Hybrid Pixel Vertex Detector Program

(3.1.1) Hughes Aircraft Co. - Berkeley Space Science Laboratory Initiative

The starting point for this collaboration was the extensive experience in the Hughes Aircraft Company of the fabrication of hybrid infrared (IR) detectors for military

applications. The collaboration during the 1980's with Berkeley Space Science Laboratory had led to the implementation of IR astronomical arrays. SLAC extended the effective collaboration in 1988, for the development of hybrid pixel arrays for high energy physics applications [5]. Figure (2) is a schematic of a hybrid pixel detector, showing the detector and electronic components and their attachment: in this case based on the Hughes 15 μm indium bump bonding process (after [7]).

During 1989-90, two chip geometries were studied: a (10×64) array of $(120 \mu\text{m} \times 120 \mu\text{m})$ pixels and a (256×256) array of $(30 \mu\text{m} \times 30 \mu\text{m})$ pixels [5,7,8,9]. Detectors were fabricated by Micron Semiconductor, and were bonded to the readout chips with an indium bump bonding process developed by Hughes. Simple readout (by Hughes), featured only on-cell charge storage, with no sparse scan or time stamping. Readout of the (10×64) array used 10 parallel analog shift registers for off-chip double correlated sampling for charge measurement. The readout of the (256×256) array was via two orthogonal 256 element analog shift registers. Table (1) shows performance data for the two arrays.

Array Geometry	(10 x 64)	(256 x 256)
Pixel Dimension	(120 μm x 120 μm)	(30 μm x 30 μm)
# R/O Nodes	10	2
Power: Read Cycle	-	-
Power: Write Cycle	10 mW	2 mW
Max Clock Speed	1 MHz	2 MHz
Noise at Room Temp	< 300 e	< 300 e

Table (1) Performance Data for the (10×64) & (256×256) arrays (after [7])

In addition, the (10×64) array exhibited a signal to noise ratio of > 100 for ^{241}Am α 's and > 35 for ^{106}Ru β 's [8,9]. In August 1990, tests of the $(30 \mu\text{m} \times 30 \mu\text{m})$ array in a 250 GeV/c π^- beam at FNAL [10], demonstrated a signal to noise ratio of about 50:1.

Progressing from the (10×64) & (256×256) arrays with their simple readout, the SLAC-Hughes-BSS collaboration started development of a smart pixel unit cell architecture to implement sparse scan and time stamping. Fig (3) shows the unit cell (after [11]) implemented in a series of Hughes pixel readout chips. Each cell contains a charge storage element, a transimpedance amplifier, a comparator that announces a pixel with a charge above threshold to row and column shift registers, and row and column addressing to read out the analog charge information from a hit pixel.

In 1991 [12] back-thinning of readout electronics from 300 μm to 50 μm (following indium bump bonding to a detector wafer) was successfully demonstrated by Hughes, leading to the prospect of hybrid pixel detectors with overall thickness similar to that of silicon microstrip detectors.

(3.1.2) The SSC Pixel Detector Development Collaboration and LBL Development of Pixel Readout Architectures for Very High Luminosity

The establishment of the SSC Pixel Detector Development Collaboration [Appendix 1: (a)] in 1990 led to the setting of design goals for a pixel detector at SSC, with the following characteristics [11]:

- (i) Peripheral architecture to selectively read only those pixels containing data, along with their 2D coordinates
- (ii) Ability to self-test and disconnect bad pixels
- (iii) peripheral logic for pixel neighbor analog readout to achieve high spatial resolution by charge interpolation
- (iv) 0.1-1 Watt/cm² power dissipation
- (v) **Self Timed** Time stamping to 16 ns resolution
- (vi) readout of charge stored and 2D addresses in 1 μ s
- (vii) maximum noise per pixel 200 electrons rms
- (viii) radiation resistance to 10 MRad
- (ix) dynamic range 500 (analog charge storage)

In 1991, a developmental readout chip (Hughes "4"; [12]) with a (64 x 32) array of (50 μ m x 150 μ m) unit cells having architecture similar to that shown in fig (3) was fabricated with the aim of realizing as many as possible of the above design goals.

Though meeting many of these goals [13], the chip exhibited significant interpixel crosstalk - via the digital signalling of hit pixels to the peripheral logic, and a time walk (difference between maximum and minimum time delay to turn on a pixel comparator) of more than 100 ns for a signal charge varying between threshold and 14 Q_{th} . A new chip (Hughes "5"), with "Hit Row" and "Hit Col" switching levels reduced to 0.1 V, and feedback capacitance reduced to 2.5 fF was developed to address these problems [14].

During 1992 [13], possible increases in the projected SSC luminosity (to 10³⁴ cm⁻²s⁻¹) and trigger level 1 latency (to 4 μ s) caused concern that such an architecture - with access relying on shift registers along both orthogonal dimensions - would be pushed very close to its operational limits.

At nominal SSC luminosity [13,15] the hit probability within a 2 cm² pixel chip 6 cm from the beam is estimated to be 9% per BCO, or 5.6 MHz. Investigation of "data - driven" architectures, requiring no centrally managed activity for the recording of primary hits, was therefore initiated at LBL. A column - based architecture is currently preferred, with one dimensional pixel communication with the periphery. In a 256 row by 64 column array, the data rate per column is 88 kHz, (340 Hz/pixel). The peripheral storage per column will be a 4- or 8-deep (depending on eventual trigger latency) FIFO storing only the time slices of BCO's corresponding to pixel hits within the column. Pixels themselves will be "smarter";

having a 2 or 3 bit memory to store a pointer to their corresponding time slice. Charge and 2-D data from pixels with a BCO pointer other than that of a level 1 trigger will not be read out. BCO pointer comparison will be destructive, resetting the pixels, but they should in any case reset themselves after a time slightly longer than the trigger 1 latency. With 4 μ s trigger 1 latency at nominal SSC luminosity, [13] a 4 deep BCO FIFO is expected to lose $< 0.01\%$ pixel hit data due to FIFO overflow, while at 10 x luminosity ($10^{34} \text{ cm}^{-2}\text{s}^{-1}$), an 8 deep FIFO would lose $< 0.5\%$ of hit data.

Column - based data driven pixel readout architecture has been investigated in a series of three custom chips (**LBL 1-3**). Other features of these chips include autonomous operation with no clocks or resets to establish the quiescent sensitive state, and signal communication to peripheral logic by currents rather than voltages to reduce crosstalk.

The **LBL-1** pixel unit cell exhibited a noise of about 50 electrons rms, and a time walk $< 38 \text{ ns}$ over an input signal range 1- 8 fC, at a (rather high) power dissipation of 120 μ W. The most serious (but not uncommon) problem was the large non-uniformity (up to 3000 e^-) seen in pixel comparator thresholds, traced to conductance variations in MOS transistors from geometric fluctuations within normally-acceptable processing limits [16]. This effect has been reduced to $< 100 e^-$ rms in **LBL- 2** through the use of a higher voltage gain at the integrator. The cell makes use of the linearity between the time over comparator threshold and the input charge [16] to give an analog charge measurement.

Fig (4) shows the measured time walk vs input charge for the unit cell of **LBL-2** [16]. Development of **LBL-2** also showed that a dramatic reduction in power consumption is possible by a relaxation of the time walk specification. This technique is of considerable interest since the time resolution (to a single BCO) may be recovered via the known correlation of time walk with input charge [17]. The next chip of the series, **LBL-3**, is designed to exploit the technique to substantially reduce power consumption. The analog region of the unit cell occupies an area of ($50 \mu\text{m} \times 150 \mu\text{m}$) in a non-radiation hard process (Hewlett-Packard 3 metal). With full array readout circuitry added, this is likely to increase to no more than ($50 \mu\text{m} \times 250 \mu\text{m}$). Radiation-hard development of the unit cell is planned for the near future.

In parallel with development at LBL of readout architecture for very high luminosities, investigation and development of the Hughes series of readout chips has continued. Recent beam tests at FNAL of a telescope of three (256×256) arrays of ($30 \mu\text{m} \times 30 \mu\text{m}$) pixels with Hughes readout and analog charge interpolation between neighboring pixels [17,18] demonstrated the outstanding spatial resolution of $\sigma = \pm 3 \mu\text{m}$ [fig (5)]. Additionally, the Hughes analog pixel unit cell has been implemented in the Hughes radiation hard SOS/CMOS process, known to be hard to at least 1 Mrad of ^{60}Co γ irradiation. The cell also continues to be a building block in a parallel program of data driven readout development [14,19,20,21] in which (unlike in the peripheral logic of Hughes chip 5), all data is pipelined off chip for downstream electronics to make the selection.

(3.2) European Hybrid Pixel Vertex Detector Program

(3.2.1) *The RD19 R&D Collaboration*

The European effort to develop "micropattern" [22,23,24] or pixel detectors for future high luminosity applications began in 1987, continued in the LAA program, with the fabrication

of a prototype chip for the readout of a ($9 \times 12 @ 200 \mu\text{m} \times 200 \mu\text{m}$) array of pixel cells [25]. The chip was implemented in the $3 \mu\text{m}$ p-well **SACMOS**¹ process; each unit cell containing a current amplifier, 10 MHz latched comparator and digital memory, but no sparsification logic or time stamping.

The chip had noise of $350 e^-$ (rms), and a power dissipation of about $30 \mu\text{W}$ per pixel element. A mean threshold non-uniformity of about 5500 e was however observed; also believed to be due to transistor geometry variations.

Pixel readout development continued within the CERN RD19 Collaboration [Appendix 1: (b)] with the development and implementation of a 1006 element ($16 \times 63 @ 500 \mu\text{m} \times 75 \mu\text{m}$) hybrid array (called "**D-OMEGA ION**") with strobed binary output [26]; [fig (6a, b)]. The readout was joined to the electronics with $28 \mu\text{m}$ solder bumps laid down using the GEC-Marconi process (§ 3.3). The chip had a noise level of $75 e^-$ rms (without the detector attached), and a power dissipation of about $25 \mu\text{W}$ per pixel element. A time walk of 50 ns was seen over an input charge range of 1- 3 fC. The mean threshold non-uniformity of about 750 e (rms) was a great improvement, but can be improved further in a $1 \mu\text{m}$ technology - eg. SACMOS $1.2 \mu\text{m}$, available soon [22].

Three of these hybrid detectors were assembled into a pixel telescope and tested in a heavy ion experiment [27] using a ^{32}S beam at OMEGA. Very encouraging results were obtained; a detection efficiency per plane of $> 99\%$, very good multitrack separation [fig (7)] with an average of 1.3 pixels per cluster (along the $75 \mu\text{m}$ direction), and a spatial resolution $25 \mu\text{m}$ (consistent with $75 \mu\text{m} / \sqrt{12}$) [fig (8)]

A few $150 \mu\text{m}$ detectors were bonded (without breakage loss) to electronic chips in the usual way, and beam tested. The results were very promising, though the comparator thresholds had to be reduced slightly to accommodate the (50%) smaller signals [22].

During 1994 the RD19 collaboration plans to contribute to the installation of three ($5 \text{ cm} \times 5 \text{ cm}$) multi-chip tiled detector arrays in the WA97 heavy ion experiment at OMEGA, in a location with a expected track density of 10 tracks per cm^2 . These will be bonded to improved "OMEGA 2" pixel chips ($64 \times 16 @ 75 \mu\text{m} \times 500 \mu\text{m}$: overall dimension $4.8 \text{ mm} \times 8 \text{ mm}$), with simple 16 column readout. These chips have a reduced time walk of 20 ns for input charge in the range $2 - 10 \times \text{threshold}$ [22].

Besides the relatively simple readout chips so far discussed, a sparse scan readout chip is presently under development [28,29]. The selective readout is shown schematically in fig (9). This makes use of a daisy chain between row and column scan lines passing only through the hit pixels, which are equipped with 1 bit digital memories. A (16×8) cell prototype (with $85 \mu\text{m} \times 280 \mu\text{m}$ pixels) has been built in $3 \mu\text{m}$ SACMOS [29]. An architecture group has been set up in RD19 to study time-stamped sparse readout, and to explore data-driven readout systems.

¹ "Self-Aligned Contact CMOS": a proprietary process of Faselec AG, Zurich,
a subsidiary company of Philips NV, Netherlands

A pixel detector has been proposed for the forward upgrade to the DELPHI microvertex detector for LEP 200 [30]. Pixel detector wafers will be arranged in a conical geometry [fig (10)] giving enhanced angular coverage between 25 and 15° of the beams. Readout chips of area 0.8-1 cm² will be bonded in two rows along a 2 cm x 6 cm high resistivity "Silicon Multichip Module" (SMM) [fig (11)] which will contain the detector diodes and all the power and signal buses necessary for the readout chips. In addition to the progress made with binary pixel cells, development of an pixel cell ("ANAPIX") with analog output is progressing within RD19. An 8-channel prototype has been bonded to a detector for evaluation. Noise is about 100 e (rms) and the output is linear up to 50,000 electrons (8 fC) [22].

The pixel vertex detector for the ATLAS experiment at LHC [1] will also use SMMs: in this case 16 chips in two rows of readout chips will be bonded on SMMs of 10 cm² area. The total detector area will be about 1 m², containing about 10⁸ pixels. A continuously sensitive readout system will transmit only the addresses of hit pixels in a BCO corresponding to a level 1 trigger. In the high luminosity LHC application, the readout electronics must be built in a technology more radiation hard than any of those so far used. The HSOI3-HD² 1.2 µm CMOS technology (which promises sufficiently high speed for LHC and survival after a total dose in excess of 10 Mrad [SiO₂], and 10¹⁴ -10¹⁵ n cm⁻²) is presently under evaluation at CERN (RD9 Collaboration) and CPPM Marseille [31]. The "deep" (1200 Å) active silicon layer of the DMILL³ SOI technology, currently under evaluation by the RD29 Collaboration [32], allows implementation of CMOS, JFET and bipolar elements for digital and analog circuitry. The process is hard to > 10 Mrad [SiO₂], and > 5.10¹⁴ n cm⁻². Pixel unit cells are under design in the HSOI3-HD and DMILL technologies at CPPM Marseille.

In addition to its use in direct particle detection, the RD19 OMEGA-ION element CMOS pixel readout chip [26] has been bump bonded to a modified, light-sensitive version of the 1006 pixel detector [33]. The quantum efficiency for the imaging of visible photons was comparable to that of a commercial photodiode, and was superior in the infra-red, a promising result.

(3.2.2) Other European Hybrid Pixel R&D

In addition to the work within RD19, a collaboration between Imperial College London, and the Rutherford Appleton Laboratory has developed 2D pixel readout electronics for use in asynchronous applications, including synchrotron X-ray detection and autoradiography.

The prototype (7 x 8 @ 300 µm x 320 µm) array [34] was implemented in 3 µm CMOS, each cell containing an amplifier/shaper, comparator and analog storage element, dissipating 220 µW/pixel. The measured amplifier noise of (140 + 0.19 fF⁻¹) electrons (rms) would give < 200 e (rms) when coupled to a typical pixel capacitance of 250 fF in this geometry.

A second version, implemented in 1.5 µm CMOS [35], was a (32 x 16 @ 200 µm x 200 µm) array; each cell containing an amplifier/shaper, comparator and 1 bit latch. Zero - suppressed readout at 10MHz is intended. Despite the suppression of the analog storage element, the power dissipation of 58 µW/pixel is still quite high, due to the high amplifier

² Silicon on Insulator Process of Thomson Composants Militaires et Spatiaux (TMS) Grenoble, France

³ DMILL ("Durci Mixte sur Isolant Logico-Linéaire") see ref [32]

gain ($75 \mu\text{V}/e^-$) needed to keep comparator threshold variations < 40 e. The measured amplifier noise is $(125 + 0.33 \text{ fF}^{-1})$ electrons (rms).

(3.3) A Review of Some Industrial Hybrid Bonding Technologies

(i) Hughes Aircraft Co. Indium Bump Process

In this process [7], developed by Hughes for the manufacture of hybrid infra-red detectors, $15 \mu\text{m}$ diameter indium bumps are separately applied to the detector diodes and readout electronic arrays. The aligned chips are then held together under pressure until the pairs of indium bumps coalesce into cold welds giving ohmic connections between each diode and its readout.

(ii) GEC-Marconi Solder Bump Process

This multistep process⁴ is being used to manufacture hybrid detectors for the RD19 collaboration [26]. A wettable layer is first deposited on the electronics, followed by the evaporation of a thick lead/tin layer. Metal in undesired locations is removed, and that remaining is then reflowed under eutectic conditions to leave an array of hemispherical solder bumps ready for bonding. A second wettable metal layer is then deposited on the detector, and the aligned detector and readout are then heated until the solder wets both pads, giving a bond. To date, more than 500,000 solder bumps (with diameters of 28 and $35 \mu\text{m}$) have been applied to RD19 detectors in this way, with very high reliability [26].

(iii) Sony-Seiko Anisotropic Conductive Film Process

In the Sony-Seiko Anisotropic Conductive Film (ACF) bonding process [36,37,38], a thin, insulating epoxy glue tape loaded with conductive particles is heated while being compressed between the two conductive surfaces to be bonded. After curing, the epoxy conducts only across the thickness of the film, and not along its length. In the Sony CP series ACF, the tape film thickness is $25 \mu\text{m}$, with a curing temperature of 150°C , and the conductive elements are $5 \mu\text{m}$ plastic balls with nickel/gold or nickel overplating. In the two versions currently available, nominal conductive particle densities are 4100 and 16000 mm^{-2} .

This technique has already been successfully to bond modelled double sided silicon microstrip detectors at $50 \mu\text{m}$ pitch. An average of 4.7 and 7 balls were seen in a ($120 \mu\text{m} \times 60 \mu\text{m}$) bond pad area for the 4100 mm^{-2} and 16000 mm^{-2} densities respectively [38]. The corresponding measured electrical connection failure rates (all causes) were 3% and 0.5%, and average electrical contact resistances were in the range 1- 6Ω ; small in comparison with the typical strip resistance of a few $\times 100 \Omega$. The technique is clearly also of interest for pixel detector hybridization.

⁴ Proprietary process of GEC-Marconi Materials Technology Centre, Caswell, Towcester, UK:
(D.J. Pedder, Plessey Research Review, 1989)

(iv) 3-M "z-Axis" Adhesive Film Process

This technique [39] is similar to the Sony-Seiko ACF process, and in common with it, is under evaluation at CPPM Marseille (RD19) for pixel detector hybridization. In this process, an epoxy carrier - randomly loaded with conductive particles - is available in 25 μm and 50 μm thicknesses in the form of sheets and 3 mm wide ribbon.

(v) Conductive Epoxy Glue Deposition by Thick Film Screen Printing

This technique, in which an array of conductive epoxy glue drops are simultaneously deposited onto a substrate via a silk screen process is under evaluation at INFN Milano for the RD19 collaboration.

(4) Monolithic Pixel Detector Developments

(4.1) Integrating Pixels and Electronics in Bulk Silicon: USA

In 1989, a group from Stanford and Hawaii Universities proposed the development of a monolithic pixel detector with integrated VLSI readout electronics [40,41,42,43]. The implementation is shown in fig (12). Onto a depleted p-type substrate, n material is diffused to make the detector diodes, and n wells are implanted for the PMOS readout electronics, covering 90% of the area. The detector array contains (30×10) pixels of $(34 \mu\text{m} \times 125 \mu\text{m})$. To minimize loss of charge, signal charges are steered between the readout electronics n wells onto low capacitance $(14 \mu\text{m})$ collection electrodes. Pixel readout is sequential by row and column shift registers operating at 8 MHz. No sparse scan is implemented.

While the fabrication of the monolithic detector is clearly complex, requiring a total of 16 masks -13 front side, 3 back side - it makes use of standard BiCMOS process steps where possible; the exception being the back side patterning, which needs one mask.

Detectors fabricated in this way have shown a signal to noise ratio greater than 80:1, and excellent spatial resolution [41,42,43]. In beam tests of a telescope of 4 detectors in a 600 GeV/c μ beam at FNAL, a spatial resolution of $\sigma = \pm 2 \mu\text{m}$ was seen along the 34 μm pixel axis (using analog charge sharing between neighboring pixels). Along the 125 μm pixel axis it was found that tracks crossing the outboard 25 μm bands of the pixels shared charge with their neighbors, allowing a spatial resolution of $\sigma = \pm 5.3 \mu\text{m}$, while in the central 75 μm of the pixels the resolution of $\sigma = \pm 22 \mu\text{m}$ was consistent with $(75 \mu\text{m} / \sqrt{12})$.

(4.2) Bond and Etch-Back SOI Developments in the USA

In this fabrication process [44], being investigated by a collaboration of UC Davis, LBL and SLAC, oxide is grown on two silicon wafers, which may be of different resistivity. These are then bonded to form a SOI sandwich containing about 1000 Å of oxide. One wafer is then substantially thinned (etched) to leave a thin silicon layer for electronics to be implanted. The other forms the detector substrate. This promising technique offers the possibility of pixel devices with total thickness of about 200 μm , with electronics having the inherent radiation tolerance advantage of thin film SOI. Test structures have been fabricated at U.C. Davis and LBL, and are currently under evaluation.

(4.3) SOI Detector - Electronics Integration in Europe (RD19)

RD19 is collaborating with IMEC, Leuven, Belgium in the development of an adapted SOI processing technology which has been applied to SOI fabricated by SIMOX, ZMR and bonded wafer techniques [24, 45,46]. In the **SIMOX** ("Separation by **I**mplantation of **O**xxygen") process, an insulating buried layer is formed by oxygen ion implantation at 500-700°C, followed by annealing at 1360°C. In **ZMR** ("Zone **M**elting & **R**ecrystallization") technique, a scanned laser beam melts silicon in small zones, which then recrystallizes on top of the oxide layer. It is expected that these SOI approaches will offer more freedom in detector geometry than the n-well electronics approach of § 4.1, and that full CMOS circuits with good radiation hardness can be built in the thin silicon layer directly above the detector.

Since SIMOX and ZMR both have high temperature process steps, with the possibility of contamination and introduction of structural defects, the two goals were to evaluate detectors in the bulk silicon, and transistors and test structures in the SOI layer. In two processing runs, repeatable detector leakage currents in the range 5 - 20 nA cm⁻² were seen from the SIMOX and ZMR processes (on 1500 Ω cm <100> Si). MOSFETs in the SOI layer had similar noise levels to MOSFETs formed in typical bulk analog processes. This work represented the first integration of SOI electronics with pin diodes on high resistivity silicon.

(4.4) Other European Monolithic Detector Developments

Monolithic pixel detector prototypes have been fabricated at IMEC, Leuven in a p- well CMOS process. In this process, p- wells to contain pixel readout electronics are implanted in n-type high resistivity silicon [47,48]. For efficient charge transfer in the p- well architecture, the electric field within the high resistivity detector substrate must be carefully screened from the potentials on components contained in the p- wells. A number of different readout building blocks, including amplifiers, comparators and shift registers have been successfully demonstrated in the technology, and a possible architecture for 2D sparse analog readout of pixel charge has been developed [47].

Other investigations of the design and performance of pixel detectors with integrated amplification and storage have been made at MPI, Munich [49]. At present however, the development of (particularly radiation - hard) front end readout electronics for silicon detectors is concentrated on implementation on more conventional lower resistivity silicon, independent of the constraints of the detector processing.

(5) Conclusions and Prospects

Active and energetic parallel programs are in place for the development of large pixel vertex detectors to operate in the extremely high luminosity environment of future high energy physics experiments. These programs are directed at the development of very radiation hard detectors and electronics, with sophisticated two-dimensional readout of only those pixels containing information arriving within triggered events of interest. With the considerable experimental and developmental base, and rapid progress already, implementation of these detectors on the timescales of the new large hadron colliders looks highly feasible.

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References

- (1) **ATLAS** Collaboration Letter of Intent, **CERN/LHCC/92-4 LHCC/I2**: (October 1,1992)
- (2) "The ATLAS Silicon Inner Tracker and Vertex Detector: Design Considerations and Related Technologies": Ed. G. Hallewell **ATLAS INDET-NO-014** (October 13,1992)
- "A Radiation Hard Detector for Tracking and Secondary Vertex Finding for the EAGLE Detector at the CERN LHC": C. Arrighi et al: **ATLAS (ex-EAGLE)-INDET-NO-009** (April 30,1992)
- (3) **ALICE** Collaboration Letter of Intent, **CERN/LHCC/93-16 LHCC/I4**: (March 1,1993)
- (4) "Radiation Doses Expected at LHC": T. Mouthuy: **ATLAS INDET-NO-012** (Sept 6, 1992)
Also revised estimates dated October 6, 1993; to be released as ATLAS INDET-note.
- (5) "Silicon PIN Diode Array Hybrids for Charge Particle Detection":
S. Shapiro et al: Nucl. Instr. & Meth. **A 275** (1989) 580
- (6) "Development of High Resolution Silicon Strip Detectors for Experiments at High Luminosity at LHC RD20 Collaboration: Status Report to CERN DRDC"
CERN/DRDC 93-30 (August 12,1993)
- (7) "Silicon PIN Diode Hybrid Array for Particle Detection: Building Blocks for Vertex Detectors at the SSC" G. Kramer et al **SLAC-PUB-4942** (May 1989)
Presented at 1989 Industrial Symposium on the Supercollider New Orleans LA (February 8-10 1989)
- (8) "Performance Measurements of Hybrid PIN Diode Arrays":
J. Jernigan et al **SLAC-PUB-5211** (May 1990)
Presented at 1990 Industrial Symposium on the Supercollider Miami Beach FL (March 14-19, 1990)
- (9) "Progress Report on the Use of Hybrid Silicon PIN Diode Arrays in High Energy Physics" S. Shapiro **SLAC-PUB-5212** (May 1990)
Presented at Vth International Conference on Instrumentation for Colliding Beam Physics, Novosibirsk, Russia (March 15-2, 1990)
- (10) "Silicon PIN Diode Array Hybrids as Building Blocks for a Vertex Detector at an Asymmetric B-Factory": S. Shapiro **SLAC-B Factory Note 57** (Sept 24,1990)
- (11) "Development of a Customized SSC Pixel Detector Readout for Vertex Tracking" O. Barkan et al **SLAC-PUB-5358** (October 1990)
Contributed to Symposium on Detector Research & Development for the SSC, Ft Worth, TX (Oct 15-18, 1990)

- (12) "Development of Pixel Detectors for SSC Vertex Tracking"
G. Kramer et al **SLAC-PUB-5518** (April 1991)
Contributed to III International Industrial Symposium on the Supercollider: Atlanta, GA (March 13-15, 1991)
- (13) "Progress Report of the Collaboration for the Development of
Pixel Vertex Detector Technology" F. Arens et al
(SSC Pixel Detector Development Collaboration: October 1,1992)
- (14) Pipeline Readout of an Array of Time Tagging Pixels based on the Hughes
Chip 5" S. Shapiro, D. Cords and S. Mani **SLAC-PUB-5916** (September 1992)
*Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High
Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)*
- (15) "SSC Pixel Array Architecture" J. Millaud et al
*Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High
Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)*
- (16) D. Nygren (LBL): Private Communication (June 1993)
also: "Pixel Vertex Detector 1993 Program Overview" Presented by D. Nygren
(LBL and SSC Pixel Detector Development Collaboration)
Presented at US Department of Energy Review, March 25, 1993
- "A Pixel Unit Cell Targeting 16 ns Time Resolution and Radiation Hardness in a Column
Readout Particle Vertex Detector" M. Wright, J. Millaud and D. Nygren
LBL 32912 and Proceedings of the International Conference on High
Energy Physics and Technology, Como Italy (June 1992)
- "SSC Pixel Unit Cell Design and Performance" M. Wright et al
*Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High
Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)*
- (17) "Converting Vice to Virtue: Can Time-Walk be Used as a measure of
Deposited Charge in Silicon Detectors," D. Nygren **LBL Internal Note** (5/17/1991)
- (18) "Preliminary Test Results from a Telescope of Hughes Pixel Arrays at FNAL"
J. Jernigan et al **SLAC-PUB-5925** (September 1992)
Presented at International Conference on B-Factories, Stanford CA (April 6-10, 1992)
- (19) S. Shapiro (SLAC): Private Communication (June 1993)
- (20) Design of a Pixel Cell Optimized for a Data Push Architecture Readout"
E. Atlas, S. Shapiro and D. Cords **SLAC Technical Note 92-2** (Dec, 1992)
- (21) Detailed Concept Review of the Analog Design of a Data Push Architecture Test Chip"
S. Shapiro, D. Cords and E. Atlas **SLAC Technical Note M351** (March 1,1993)
- (22) "Development of Silicon Micropattern Pixel Detectors": E. Heijne et al: *These Proceedings*
- (23) "Status Report and Addendum Development of Hybrid and Monolithic Silicon
Micropattern Detectors" RD19 Collaboration: **CERN DRDC/93-6** (January 10,1993)

- (24) "Development of Silicon Micropattern (Pixel) Detectors"
P. Delpierre et al: Nucl. Instr. & Meth. **A 315** (1992)133
- (25) "A 10 MHz Micropower Front end for Direct Readout of Pixel Detectors"
M. Campbell et al: Nucl. Instr. & Meth. **A 290** (1990)149
- (26) " A 1006 Element Hybrid Silicon Pixel Detector with Strobed Binary Output"
F. Anghinolfi et al: IEEE Trans Nucl Sci **NS-39** (1992) 650
- (27) "A Hybrid Silicon Pixel Telescope Tested in a heavy Ion Experiment"
H. Beker et al: Nucl. Instr. & Meth. **A332** (1993) 188
- (28) "A Sparse Scan Circuit for Pixel Detector Chips"
P. Delpierre and J.J. Jaeger: Nucl. Instr. & Meth. **A305** (1991) 627
- (29) "A Sparse Scan Circuit for Pixel Detector Readout"
J.J. Jaeger et al: IEEE Trans Nucl Sci **NS-40** (1993) 400
- (30) Proposal for the Upgrade of DELPHI in the Forward Direction
The DELPHI Collaboration: **CERN/LEPC/92-13** 16 October 1992
also **DELPHI 92-142 GEN 135** (October 16,1992)
- (31) "A Demonstrator Analog Signal Processing Circuit in a Radiation Hard
SOI - CMOS Technology" F. Anghinolfi et al: CERN DRDC R & D Proposal
CERN/DRDC/90-79 DRDC/P21 (December 11, 1990)
- (32) "A Mixed Analog-Digital Radiation Hard Technology for High Energy
Physics Electronics: DMILL" ("Durci Mixte sur Isolant Logico-Linéaire")
M. Dentan et al: CERN DRDC R & D Proposal
CERN/DRDC/92-31 DRDC/P42 (May 14, 1992)
- (33) "Imaging of Visible Photons Using Hybrid Silicon Pixel Detectors"
C. Da Via et al: *These Proceedings*
- (34) "A Prototype Pixel readout Chip for Asynchronous Detection Applications"
D. Raymond et al: Nucl. Instr. & Meth. **A310** (1991) 552
- (35) "A 2-D Amplifier Array Chip for Pixel Detector Readout"
D. Raymond et al: *These Proceedings*
- (36) "Development of Novel Architecture and Assembly Techniques for a
Detector Unit for a Silicon Microvertex Detector using the Flip-Chip Bonding
Method" Y. Saitoh et al. IEEE Trans Nucl Sci **NS-40** (1993) 233
- (37) "Development of New Assembly Techniques for a Silicon Microvertex
Detector Using the Flip - Chip Bonding Method" Y. Saitoh et al.
Proc Int. Symp. Semiconductor Tracking Detectors, Hiroshima (May 22-24, 1993)
- (38) J. Yamanaka (Seiko Instruments): Private Communication (June 1993)
- (39) 3-M 5303R Z-axis Adhesive Film Product Bulletin
3M Electronic Products Division, 6801 River Place Blvd, Austin TX 78726-9000 USA

- (40) "A Proposed VLSI Device for Particle Detection: S. Parker et al:
Nucl. Instr & Meth. A **275** (1989) 494
- (41) "Performance of a Monolithic Pixel Detector" C. Kenney et al
Proceedings of the International Conference on High Energy Physics and Technology, Como Italy (June 1992)
- (42) "Monolithic Pixel Detector Results: Tracking at 500 GeV/c" S. Parker et al
Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)
- (43) S. Parker (Univ Hawaii): Private Communication (June 1993)
- (44) "Monolithic Pixel Detector Design Based on Bond & Etch-Back SOI" S. Mani
Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)
- (45) "Detector Diodes and Test Devices Fabricated in High Resistivity SOI Wafers": L. Bosisio et al IEEE Trans Nucl Sci **NS-40** (1993) 230
- (46) "Integration of CMOS Electronics in an SOI Layer on High Resistivity Silicon Substrates" B. Dierickx et al IEEE Trans Nucl Sci **NS-40** (1993) 414
- (47) "Fully Integrated CMOS Pixel Detector for High Energy Particles"
G. Vanstraelen et al Nucl Instr & Meth **A275** (1989) 574
- (48) "Monolithic Integration of Solid State Particle Detectors and their Read-out Electronics on High Resistivity Silicon"
G. Vanstraelen: PhD Thesis, Katholieke Universiteit Leuven, (December 1990)
- (49) "Design and Performance of Semiconductor Detectors with Integrated Amplification and Charge Storage Capability" : B. Heinemann et al:
Nucl. Instr & Meth. A **305** (1991) 517

Appendix 1: Major Pixel Detector R&D Collaborations

(a) SSC Pixel Detector Development Collaboration

Adept IC Design-Lawrence Berkeley Laboratory- Berkeley Space Science
Laboratory-FNAL-U.C. Davis-Hughes Aircraft Co-U. Iowa-INFN Milano-
U. Pavia-U. Pisa-U. Oklahoma-SLAC

(b) CERN RD19 Collaboration:

Athens-Bari-Bologna-CERN-Cge de France-CPPM-EPF Lausanne-ETH Zurich-
Genova-Ljubjana-Milano-Modena-Padova-Pisa-Prague-Rome-Wuppertal-SEFT-
Canberra Semiconductor-GEC Marconi-Smart Silicon Systems

Figure Captions

Fig (1) The proposed layout of the inner detector of the ATLAS experiment for LHC. The layout includes a vertex detector containing two cylindrical pixel surfaces at radii 11.5 and 14.5 cm, with coverage to ± 1.5 units of pseudorapidity.

Fig (2) Schematic of a hybrid pixel detector, showing the detector and electronic components and their attachment: in this case based on the Hughes 15 μm indium bump bonding process.

Fig (3) Pixel unit cell architecture developed by the SLAC-Hughes-BSS collaboration, and similarly implemented in a series of Hughes pixel readout chips. Each cell contains a charge storage element, a comparator that announces a pixel with a charge above threshold to row and column shift registers, and row and column addressing to read out the analog charge from a hit pixel.

Fig (4) Measured time walk vs input charge for the unit cell of LBL-2 [16].

Fig (5) Spatial resolution of $\sigma = \pm 3 \mu\text{m}$ demonstrated in beam tests of a telescope of three (256×256) arrays of ($30 \mu\text{m} \times 30 \mu\text{m}$) pixels with Hughes readout and analog charge interpolation between neighboring pixels [16,18].

Fig (6) (a) Layout of the RD19 pixel electronic cell of ($75 \mu\text{m} \times 500 \mu\text{m}$). The pad for 28 μm solder bump bonding is at the left.
(b) Schematic of the unit cell readout circuit.

Fig (7) Multiple tracks passing through a telescope of 3 pixel chips in a heavy ion experiment. Pixel geometry is ($75 \mu\text{m} \times 500 \mu\text{m}$); total chip area is ($8 \text{ mm} \times 4.7 \text{ mm}$).

Fig (8) the Spatial resolution measurements from a telescope of three chips of ($75 \mu\text{m} \times 500 \mu\text{m}$) pixels in a heavy ion experiment. Measured spatial resolution along the pixel 75 μm direction is 25 μm (consistent with $75 \mu\text{m} / \sqrt{12}$).

Fig (9) Schematic of the sparse scan system proposed by the College de France group, and now under development in RD19. The selective readout makes use of a daisy chain between row and column scan lines passing only through the hit pixels.

Fig (10) The proposed conical geometry for pixel detectors in the upgraded DELPHI microvertex detector for LEP 200.

Fig (11) A "silicon multichip module (SMM)" in which several readout chips are bonded to a substrate containing the silicon pixel array and simple readout bussing functions. This example shows the SMM for the DELPHI pixel detector with readout chips of area 0.8 -1 cm^2 bonded in two rows. The geometry for ATLAS will be similar.

Fig (12) The Monolithic Pixel Detector and Electronics Geometry developed by the Hawaii - Stanford collaboration. Readout electronics is accommodated in n wells implanted in the p-type substrate.

Fig (1)

Fig (2)

Fig (3)

Fig (4)

Fig (5)

Fig (6a)

Fig (6b)

Fig (7)

Fig (8)

Fig (9)

Fig (10)

Fig (11)

Fig (12)