DD

CERN LIBRARIES, GENEVA

P00022842

HEPHY-PUB 603/94

March, 1994

Sw 3417

CHARGE DIVISION IN SILICON STRIP DETECTORS WITH A LARGE STRIP PITCH

W. DABROWSKI, P. GRYBOS

*Faculty of Physics and Nuclear Techniques, Academy of Mining and Metallurgy,
Cracow, Poland*

M. KRAMMER, H. PERNEGGER, D. RAKOCZY

*Institute for High Energy Physics, Austrian Academy of Sciences,
Vienna, Austria*

Abstract

The mechanism of charge division in silicon strip detectors with large strip pitch was investigated. Prototypes with different strip width were produced and parametrised. A detailed equivalent circuit of the detector and the associated electronics was modelled within SPICE. The results of the simulation are compared with measurements from a beam test.

(To be submitted to Nuclear Instruments and Methods)

1. Introduction

Silicon microstrip detectors are used in many experiments where excellent spatial resolution is needed. With a readout pitch of 50 μm a spatial resolution of a few μm has been achieved by many groups [1]. For some applications in present and future experiments such an excellent resolution is not required. In collider experiments this is the case for detectors at large radius and therefore covering large areas. The second area of interest are detectors at small angles where usually the position resolution is limited by multiple scattering due to a large amount of material crossed by the particles. For these detectors the arguments like number of electronic readout channels and the costs become more important.

A logical solution for such detectors is to increase the readout pitch and to reduce the number of electronic channels and in this way reduce costs, power dissipation, etc. For a detector with a large readout pitch and without additional intermediate strips the process of the charge sharing between two adjacent strips is effective only for the charges released in a very small central region between the strips. For most particles crossing the detector perpendicularly the charge will be collected only by one strip and the spatial resolution will be limited by the readout pitch independently whether analogue or digital readout is used. Intermediate strips inserted between the readout strips improve the charge division by the capacitive coupling and this allows to improve the spatial resolution significantly using the pulse height information. The final spatial resolution is determined by the number of intermediate strips, the interstrip capacitance and the signal-to-noise ratio.

To avoid a charge loss in the process of charge division the interstrip capacitance should be significantly larger than the capacitance to backplane. This is the case for detectors with a small pitch, e.g. 25 μm strip pitch and 50 μm readout pitch. For detectors with the strip pitch above 100 μm the capacitance to backplane becomes of the same order of magnitude as the interstrip capacitance. Therefore, a critical issue for this kind of detectors is the charge loss to the backplane capacitance for particles generating the charge under the intermediate strips. For a given strip pitch the interstrip capacitance can be adjusted in a certain range using different widths of the strip implants. However an increase of the interstrip capacitance by increasing the implant widths results in an increase of the total input capacitance seen by the preamplifier input and therefore an increase of noise. The detector layout should be optimised taking into account the charge losses as well as the signal-to-noise ratio degradation.

In this work the prototype strip detectors for the very forward tracker for the experiment DELPHI were studied. Due to constraints for the geometry and the number of readout chips per detector module the readout pitch was fixed to be about 200 μm . The aim of this study was to optimise the detector layout with respect to the interstrip

capacitance and the signal-to-noise ratio for the required spatial resolution to be below 70 μm . Prototype detectors with different strip widths were produced and parametrised. The measured parameters were used to build an electrical equivalent model of the detector which allows us to study the charge division using the SPICE package for simulation of electronic circuits. The results from SPICE were subsequently compared with the results from a beam test.

2. Detector design

The detectors were produced using 4 inch silicon wafers of 350 μm thickness from Wacker Chemitronic (FRG). The resistivity of the initial material was 6.5 $\text{k}\Omega\text{cm}$. The processing of the detectors was done at TESLA Roznov company (Czech Republic).

The active detector area is 52 x 52 mm^2 with 504 strips of 100 μm pitch. One half of the detector (252 strips) contains the strips with the implant width of 20 μm and the other half the strips with the implant width of 40 μm . The AC coupling of the strips is obtained using a 200 nm thick silicon oxide layer between the p^+ implants and the metal readout strips on top of them. The widths of the metal readout lines are the same as the widths of the implant strips, i.e. 20 μm and 40 μm respectively. The readout lines were placed only on top of every second strip. This way we obtained detectors with a readout pitch of 200 μm and with one intermediate strip between two readout strips. All the strips were biased through a FOXFET structure with the gap between drain and source of about 5 μm and the gate oxide thickness of 1 μm .

3. Leakage current and FOXFET dynamic resistance

Typical I-V characteristics of a readout strip and an intermediate strip are shown in figure 1. The current densities are low, on the level of 10^{-7} Acm^{-3} which is about the value obtained for large diodes on high resistivity silicon [2]. For the readout strips which are covered by the metal strips separated from the implants by an oxide layer, the leakage current is about 30% higher than for the intermediate strips which have no metal strips on top of them. It was observed before [3] that for AC coupled microstrip detectors the average leakage current density can be an order of magnitude higher than in large area diodes made on silicon of the same resistivity. This effect can be explained by the fact that the presence of the metal strips causes the generation of high electric fields in small regions around the implant strips in which high currents can be generated due to avalanche multiplication [4]. The difference between the readout strips (with metal strips) and intermediate strips (without metal strips) observed in our detectors is probably of the same nature, however it is much smaller than observed for other detectors.

The structure of a field effect transistor with the gate fabricated on a field oxide was chosen to bias the strips because of its simplicity. In comparison with the punch-through biasing scheme it has the advantage to allow the tuning of the dynamic resistance by the gate voltage [5]. Figure 2 shows the dynamic resistance, defined as dU_{ds}/dI_s versus the gate voltage measured at $I_s=0$ nA. For all further measurements the gate voltage was set to 0 V. For the SPICE simulations the value of 200 M Ω was assumed as the typical small signal value for the bias resistance. The offset voltage of the FOXFET was found to be $U_{ds}=5.2$ V at $U_{Gate}=0$ V.

4. Capacitances

Our goal was to identify the parameters of the detector equivalent circuit which allows us to perform the SPICE simulation of the signal processing. In the commonly used equivalent circuit for an AC coupled microstrip detector four different capacitances associated with each strip are distinguished. There are: capacitance to backplane, interstrip capacitance to first neighbours, interstrip capacitance to second neighbours and coupling capacitance between the implant and the metal strip.

The capacitance to backplane and the interstrip capacitance were measured at a frequency of 100 kHz using the HP4285A LCR meter while the detector bias was supplied by the Keithley 237 Source Measure Unit. Both instruments were controlled by a Macintosh computer. All the measurements were performed on a probe station for unbonded structures.

Both, the capacitance to backplane and the interstrip capacitance were measured for the readout strips. The same capacitance measured for the intermediate strips exhibit a frequency dependence due to the high resistance of the p^+ implants. For the readout strips the high resistance of the p^+ implants is bypassed for AC signals by the low resistance of the metal strips.

Figure 3 shows the capacitance to backplane measured for a single readout strip and plotted as $1/C^2$ versus bias voltage. The full depletion voltage obtained from this measurement is about 90 V. At a bias voltage of 100 V the capacitance to backplane is 0.33 pF/cm for both, 20 μ m and 40 μ m strips, which corresponds very well with the theoretical value for a 350 μ m thick strip structure with 100 μ m pitch.

The interstrip capacitance was measured between the readout strips for the same reason as in the case of the capacitance to backplane, i.e. a large resistance of the intermediate strips. This way the measured capacitance was equal to the sum of the series connection of two interstrip capacitances between a readout strip and an intermediate strip, and of the direct interstrip capacitance to second neighbours. Due to the particular design of our detectors (no metal strips on top of the intermediate strips) it was not possible to measure directly the interstrip capacitance to second neighbours. Analysing, however, other data

available in literature [3,6] we found that the ratio of the interstrip capacitance to second neighbours - to - the interstrip capacitance to first neighbours scales quite well with the pitch of a detector for the given gap-to-pitch ratio. The extrapolated value of this ratio for our detector was found to be about 0.1. Using this value and solving a simple equation we extracted from the measurements the capacitance to first neighbours and the capacitance to second neighbours. The total interstrip capacitance to both adjacent strips C_{tot} , being defined as $2C_{n1}+2C_{n2}$, for a 20 μm strip and a 40 μm strip is plotted in figure 4 as a function of the bias voltage. For a bias voltage of 100 V we obtained the interstrip capacitance of 0.73 pF/cm for 20 μm strips, and 1.07 pF/cm for 40 μm strips.

The coupling capacitance was evaluated in conjunction with the p^+ implant strip resistance by combining the measurements of capacitance versus frequency and the SPICE simulations. A relatively high resistance of the implant strip and the coupling capacitance between the implant strip and the metal strip form together a distributed RC line. Using a LCR meter we, in fact, replace the measured RC line by a series (series circuit mode) or parallel (parallel circuit mode) connection of an equivalent capacitance and an equivalent resistance. As the result the coupling capacitance measured by the LCR meter exhibits a frequency dependence and the obtained values of C and R are different for the series and parallel mode used in the meter. If we could measure independently the resistance of the p^+ implant strip it would be possible to evaluate the capacitance from the measurement for a single frequency. However, the design of the detector does not allow to measure directly the resistance of the implant strip because only one contact to the strip is open. Therefore we performed the measurements of the coupling capacitance versus frequency in the range from 100 Hz to 1 MHz using the HP4285A LCR meter in both, series and parallel mode. For these measurements bias line, gate of the FOXFET and backplane were grounded.

The results obtained in the series and the parallel mode for a 40 μm strip are shown in figure 5. Similar results were obtained for 20 μm strips. As one can expect for low frequencies the impedance of the coupling capacitance is large compared with the strip resistance and the measured capacitance remains frequency independent. The obtained low frequency values are: 30 pF/cm for 20 μm strips and 54 pF/cm for 40 μm strips.

To evaluate the resistance of the p^+ implant strips we simulated our measuring set-up in SPICE. The measured strip was simulated as a lumped circuit shown in figure 6. A 5.2 cm long strip was divided into 1300 cells, each consisting of a pair of resistors representing the metal strip, a pair of resistors representing the implant strip and a coupling capacitor bridging both pairs. In addition the resistance of the implant strip between the probe contact and the capacitive area was taken into account. The resistivity of the top aluminium layer was measured directly and the values of 15 Ω/cm and 7.5 Ω/cm for 20 μm strips and 40 μm strips respectively were found. Thus, taking the measured low frequency value of the coupling capacitance and the metal resistance as known parameters

of our equivalent circuit, we found the value for the implant strip resistance giving the best matching between the measurements and simulations. The curves obtained from simulations of the series and the parallel mode of the LCR meter for a 40 μm strip are shown in figure 5. A very good agreement was obtained which indicates that our model corresponds fully to the real measured structure. The values obtained this way for the implant strip resistance are 120 $\text{k}\Omega/\text{cm}$ for 20 μm strips and 60 $\text{k}\Omega/\text{cm}$ for 40 μm strips.

5. SPICE simulation of the signal processing and noise

Having identified all the components of the small signal equivalent circuit for our detectors we were able to simulate the process of the signal generation in the front-end electronics. Especially we were interested if the relatively large resistance of the implant strips and the lack of the metal strips on top of the intermediate strips has any effect on the processing of the signals generated in the area of intermediate strips and on the noise.

The equivalent circuit of the detector used for the simulations is shown in figure 7. The detector was modelled as a lumped network of R and C components including capacitance to backplane, interstrip capacitance to first neighbours, interstrip capacitance to second neighbours, resistance of the metal readout strips, resistance of the p^+ implant strips, and small signal resistance of the FOXFET. The simulations were performed for a circuit consisting of 9 strips (4 readout strips and 5 intermediate strips). In this way we could neglect the asymmetry introduced by the edges of the detector for 3 strips in the centre of the circuit. Each 5.2 cm long strip was divided into 126 identical cells.

The front-end electronics was modelled by an simplified equivalent circuit corresponding to the block diagram of the VIKING chip [7]. The diagram of the circuit is shown in figure 8. It consists of a charge-sensitive preamplifier based on a transconductance amplifier followed by the differentiating circuit and an integrator. The storage capacitor of the sample&hold circuit is included because it influences the effective time constant of the integrator. The values of components used in the feedback loop, differentiating circuit and integrator correspond to the values of components used in the VIKING chip. The cascode amplifiers used in VIKING are modelled as voltage controlled current sources with the transconductances equal to the transconductances of the appropriate transistor in the VIKING chip. The values of components used in the circuit are listed in the figure. At the input of the preamplifier two resistors are added to simulate the equivalent input series voltage noise (R_s) and the equivalent input parallel current noise (R_p). To obtain an approximate value of R_s corresponding to the noise of the real chip it was assumed that the filtering function of the circuit corresponds to a simple CR-RC shaping with the time constant $\tau = 1.5 \mu\text{s}$. Thus, the resulting value of R_s can be found

from the slope of the equivalent noise charge ENC versus input capacitance according to the formula

$$\frac{ENC}{1 \text{ pF}} = \frac{1}{q} \sqrt{\frac{4kTR_S}{\tau}} \quad (1)$$

where q is the elementary charge and $ENC/1\text{pF}=12 \text{ el/pF}$ for the VIKING chip. For the above values we obtained $R_S=510 \Omega$. The parallel resistance R_P represents the shot noise of the detector leakage current and can be found by comparison of the shot noise with the equivalent thermal noise according to equation

$$2qI_d = \frac{4kT}{R_P} \quad (2)$$

For a typical value of strip leakage current $I_d=0.2 \text{ nA}$ we obtained $R_P=255 \text{ M}\Omega$.

The front-end circuit described above was attached to each readout strip of the detector equivalent circuit and the whole system was simulated using SPICE. The signal generated in the detector by a minimum ionising particle was simulated by a current source attached to the node in the detector equivalent circuit corresponding to the point of particle incident and generating a short δ -like pulse, carrying the standard charge of 25000 electrons. As it was mentioned before, our goal was to study the mechanism of the capacitive charge division in our detectors. Therefore we simulated the response of the front-end electronics for the signal source applied: (1) to a readout strip, (2) to an intermediate strip. The simulations were performed for $20 \mu\text{m}$ strips, $40 \mu\text{m}$ strips and $60 \mu\text{m}$ strips. The predicted parameters for $60 \mu\text{m}$ strips were evaluated by scaling the measured parameters obtained for $20 \mu\text{m}$ and $40 \mu\text{m}$. The results are shown in figure 9. As one could expect, for the signal generated in the area of the readout strip no difference was observed for different widths of the strips. When the signal source is attached to the intermediate strip we observe approximately one third of the signal on each of the adjacent strips and some further degradation of the signals for narrower strips. This is due to the fact that for the signal generated in an intermediate strip the effective coupling capacitance is formed by the series connection of the interstrip capacitance and the coupling capacitance of the readout strip. Because the interstrip capacitance is small, only a fraction of the signal is transferred to the preamplifier and the other fraction is lost to the backplane capacitance. To verify if there is any effect caused by the lack of metal strips on top of the intermediate strips, which bypasses the high resistivity of the implant, we repeated simulations for the model including these metal strips while the interstrip capacitance was kept unchanged. No significant difference in the results given by those two models was found. Of course, in a real structure the metal strips placed on top of the intermediate strips will increase the interstrip capacitance. However, the same effect can be achieved by increasing the implant widths.

From the point of view of signal processing wider strips, giving larger interstrip capacitance, should be recommended. On the other hand, however, the interstrip capacitance is the dominating component of the total capacitance at the preamplifier input and determines the resulting noise of the system. To study this effect a noise analysis was performed in SPICE for our system. Applying a full equivalent circuit for the strip detector we could take into account some second order effects in the noise analysis, i.e. the thermal noise generated by the resistance of the implant and metal strips and the effect of noise injection to the given channel through the interstrip capacitance from preamplifiers attached to the adjacent channels. The summary of the signal and noise analysis is given in table 1. Contradictory effects of the interstrip capacitance on the noise and signal coupling are clearly visible in the table. Notice that in the simulation a low noise front end electronics was used, so the effect of noise increase due to the increase of the interstrip capacitance is relatively small. For any faster front-end electronics this effect will be more significant as the slope of noise per input capacitance will be larger.

6. Comparison with test beam results

Finally the detectors were assembled with the front-end readout electronics and used in the beam test [8] at the CERN PS accelerator using a proton and pion beam of energy equal to 7 GeV/c. The set-up consisted of 3 strip detectors mounted with parallel strip orientation on a platform. The beam direction was perpendicular to the detector surface. For triggering a telescope of 3 scintillators with the effective trigger area of $4 \times 8 \text{ mm}^2$ was used. All measurements were performed with a detector bias of 80 V. The signals from each detector were readout by 2 VIKING chips, each containing 128 channels [7], which were glued on ceramic hybrids. The hybrids were glued directly onto the surface of the detectors. Each hybrid was connected to a so-called repeater board which supplied the necessary control and clock signals for the VIKING chip and amplified the analogue output signals. The output signals were digitised and processed using a SIROCCO FB module [9].

In the analysis of the ADC data the signal correction is done for the pedestals and the DC-level shift common for all channels. Next, the following cluster finding algorithm was applied: (1) for each strip the signal-to-noise ratio (S/N) is calculated, (2) a cluster is defined as a series of adjacent strips in which each strip has S/N higher than 2.5, (3) the S/N ratio for the cluster is defined as the sum of S/N ratios of all strips in the cluster, (4) the cluster is accepted in the analysis if the cluster S/N ratio is higher than 6. Saturated and noisy channels were excluded from the analysis.

Figure 10 shows the measured cluster signal distributions for hits on the readout strips (a), and for hits on the intermediate strips (b). The distributions obtained for

20 μm strips (solid lines) and 40 μm strips (dashed lines) can be compared directly on each plot. For hits on a readout strip the distributions show no significant difference between 20 μm and 40 μm strips, as predicted by the simulation. The signal distribution measured on intermediate strips of 40 μm width is shifted towards higher signals compared to the distribution measured for 20 μm intermediate strips.

All measured distributions follow well the Landau distribution (fit overlaid in figure 10). For comparison of the obtained results with the simulations we took the most probable values of the cluster signals. The ratios of the cluster signal for hits on an intermediate strip to the cluster signal for hits on a readout strip obtained from measurements and simulations are compared in table 2. Clearly the same tendency - a decrease in the charge loss for intermediate strips with increasing strip width - is seen in both simulation and beam test. The difference of about 10% may be explained by the simplifications in the models used for simulation.

At this point we would like to emphasise that in our beam test a low noise but relatively slow front end electronics was used, so the effect of noise increase due to the increase of the interstrip capacitance is relatively small. For a fast front end electronics like that required for the LHC pp experiments the slope of noise per input capacitance will be larger, in the range of 60-80 eI/pF, and any increase of the interstrip capacitance will have a significant impact on the S/N ratio and on the efficiency of the system. Given the fact that the expected S/N ratio is only about 20 for detectors optimised for a low interstrip capacitance, the noise level may become a real limitation for the charge division readout in silicon trackers for LHC experiments.

Acknowledgements

This work was partially supported by The Polish State Committee for Scientific Research (Project no 209069101 and no 2P30206205). We would like to thank the Austrian Academy of Sciences for the support of P.Grybos during his stay in Vienna.

References

- [1] N.Bingefors et al., NIM A328 (1993) 447
A.Adam et al., DESY 93-159, INFN/AE-93/21
C.Adolphsen et al., SLAC-PUB-5443 (1991), submitted to NIM A
- [2] K.Gill et al., NIM A322 (1992), 177
- [3] A.Holmes-Siedle et al., CERN Preprint, CERN-PPE/93-137
- [4] E.H.Nicollian and J.R.Brews, MOS Physics and Technology,
Wiley Interscience 1982, p.7
- [5] P.P.Allport et al., NIM A310 (1991) 155.
- [6] G. Hall et al., NIM A326 (1993), 228
- [7] O.Toker et al., NIM A340 (1994), 572
- [8] DELPHI internal report, to be published
- [9] N.Bingefors and M.Burns, DELPHI 88-48 TRACK 48, 1988

Table 1
Simulated signal and noise for different strip widths

Strip width	Output noise [mV]	Signal generated in the intermediate strip		Signal generated in the readout strip	
		Output signal [mV]	SNR	Output signal [mV]	SNR
20 μm	0.63	18.2	29.0	57.4	91.2
40 μm	0.66	20.6	31.4	57.6	87.6
60 μm	0.68	21.8	32.1	57.8	84.9

Table 2
Cluster signal ratio of intermediate to readout strip. Comparison between simulation
and beam test.

Strip width	20 μm	40 μm	60 μm
Simulation	0.64	0.72	0.75
Beamtest	0.58	0.64	x

Figure captions

Fig.1. Leakage current versus bias voltage for 5.2 cm long strips (measured at 22 °C).

Fig.2. Small signal FOXFET resistance as a function of gate voltage (at $I_{ds}=0$ nA).

Fig.3. Capacitance of a single strip to backplane plotted as $1/C^2$ versus bias voltage.

Fig.4. Total interstrip capacitance versus bias voltage for 20 μm and 40 μm strips.

Fig.5. Coupling capacitance for 40 μm strips as a function of frequency measured in the series mode (C_s) and the parallel mode (C_p). Continuous lines were obtained from SPICE simulations.

Fig.6. Model used for the simulation of coupling capacitance.

Fig.7. Full equivalent circuit of a microstrip detector used for the SPICE simulations.

- a) Cross section perpendicular to strips.
- b) Cross section along strips.

Fig.8. Simplified equivalent circuit of the front-end electronics based on the VIKING chip.

Fig.9. Pulse shapes obtained from simulations for the signal generated in a readout strip and in an intermediate strip of 40 μm width (a),
and in an intermediate strip for 20 μm , 40 μm and 60 μm width (b).

Fig.10. Signal distributions (ADC counts) measured on readout and intermediate strips with 20 μm and 40 μm strip width (Landau fit overlaid).

Fig. 1

Fig. 2

Capacitance to backplane

Fig. 3

Total interstrip capacitance

Fig. 4

Fig. 5

Coupling capacitance

Fig. 6

Fig. 7

Fig. 8

a.)

b.)

Pulse shapes obtained from simulation

Fig. 9

Signal distribution

Fig. 10