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FLASH ADC BASED DIGITIZER

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Abstract

We describe the design and performance of an 8-bit Flash ADC based readout system developed for use on the cathode pads of the DELPHI High Density Projection Chamber (HPC). A dynamic range of 800:1 is obtained at input frequencies of 15 MHz using a bilinear voltage divider reference chain. Performance characteristics of the digitizing circuits for a CAMAC version of this readout system are presented. The design of a FASTBUS version is presented.

Introduction

The DELPHI central region electromagnetic calorimeter, the High-Density Projection Chamber (HPC),¹ is a fine-grained gas sampling calorimeter which uses the principle of time projection to obtain three-dimensional localization of the energy deposition within it. A series of proportional tubes with U-shaped cross-sections are used to amplify the drifted charge. The signals induced on the cathodes of these tubes are collected on a series of pads. The final system will instrument 128 readout pads in each of 144 HPC modules, for a total of 18,432 readout channels. Thus we will collect digitized charge information in $\sim 4.7 \times 10^6$ spatial cells. The HPC is scheduled for installation at the Large Electron Positron Collider (LEP) in 1988.

Several factors constrain the design of digitizing readout electronics for the HPC. (1) Since in any given event only a small fraction of the spatial cells are populated with charge information, we must incorporate hardware zero suppression circuitry into the readout electronics. (2) In order to enhance the HPC's ability to resolve single photons from π^0 's, we must sample the collected charge 256 times per event over the 90 cm drift length of the modules. The LEP beam crossing rate then requires that digitization of charge deposited by the particles traversing this detector occur at a frequency of about 15 MHz. (3) A study of the charge deposited in the HPC by pions and electrons indicates that in order to permit both a reasonable sampling of single minimum ionizing particles and of showers of energies $\gtrsim 20$ GeV

without appreciable saturation, a dynamic range of $\sim 800:1$ is required.²

We have been able to meet these design criteria, using a newly available 8-bit Flash ADC (Thomson TS 8308/TS 8328).³ We have designed, tested and built prototype readout systems for the HPC. The requisite dynamic range is achieved using a bilinear conversion curve over a total range of 4.0 V. Four reference voltages applied to the FADC are adjusted to yield 5.0 mV/count for the first 64 counts and 20.0 mV/count over the rest of the range. This gives about 9.5 bits of equivalent resolution in the region of single minimum ionizing particles. Under these conditions, the measured analog bandwidth of the digitizer circuit is 7.5 MHz.

The output of the Flash ADC is stored in a ($2K \times 8$ -bit) cache memory. In our FASTBUS design, eight such channels are multiplexed through a single zero-suppression circuit and stored in a four event deep buffer memory. This Front End Buffer (FEB) consists of two $8K \times 8$ -bit CMOS memory chips. For time slices containing non-zero data, the output of the zero-suppression circuitry consists of 8-bits of digitized charge data (which we store in one of these chips) and 8-bits of address information to locate the data within the 256 time slices (which are stored in the second chip). Thus not all of this memory is filled. Each single width FASTBUS module contains four of these units for a total of 32 channels per module.

CAMAC Design

In order to test the properties of the FADC, we constructed 56 channels of the readout electronics using the 24-pin version of this device (Thomson TS 8308). In figure 1a we show a baby board consisting of the FADC, a $2K \times 8$ -bit CMOS cache memory, an op amp which supplies the reference voltages for four tap points on the internal FADC divider chain, the read/write control for the cache memory, and gates to supply clock and chip enable signals. Four of these baby boards mount on a single CAMAC module as shown in figure 1b.

Figure 1 - 4-Channel CAMAC Board Design

(a) Baby Board design using the 24-pin FADC.

(b) CAMAC Mother Board for testing the FADCs.

Figure 2 - Logic Diagram for the CAMAC FADC Board.

Figure 2 is block diagram of this module. In our application the analog and digital supply voltages for the FADC are fixed at +6.5 Volts. This is well above the manufacturer's maximum specified voltage of +5.25V. The upper reference voltage of the FADC is held at +4.0 volts and lower reference voltage is held at ground. Internally the Thomson TS 8308 contains a linear resistor network delivering 256 reference voltages distributed linearly between these two external reference voltages. However, pin access is also available to the quarter, half, and three-quarter reference points. To achieve the requisite bilinear operation the quarter tap point is adjusted to +320 mV. We find the linearity over the upper three-quarters of reference chain is substantially improved by adjusting the voltages at the two remaining tap points. Thus in figure 1a, there are five potentiometers mounted on the baby board. Four of these are used to adjust the input levels of operational amplifiers used in the unity-gain mode to control the voltage at the 1/4, 1/2, 3/4, reference points as well as the upper reference voltage. The fifth is used to adjust the lower reference voltage to ground.

The input signal is sampled at 15 MHz and stored in a $2K \times 8$ -bit static RAM cache memory. We have obtained satisfactory performance with 35 nsec access-time RAMs (Cypress⁴ CY7C128-35 and Toshiba⁵ TMM2018D-35) but find the data is distorted if we attempt to use 45 nsec RAMs (Toshiba⁵ TMM2018D-45). Since the zero-suppression logic had been tested elsewhere,² it was not implemented on these boards. However, the data words are expanded to 16-bits to allow for each pulse height to be associated with a clock count before being output to the CAMAC dataway.

In figure 3, we present a typical plot of counts versus input voltage obtained with these boards by averaging 256 input samples at a series of fixed d.c. input levels. The bilinear performance is readily observed with a breakpoint at 64 counts (320mV). In order to obtain this curve the potentiometers at the lower, upper and 64-count tap points were adjusted to 0.000, 4.000, and 0.320 volts respectively, while the remaining two tap points were adjusted to give the

ADC
Counts

Figure 3 - ADC counts versus input level for a series of fixed d.c. inputs.

best linearity. The two slopes are measured to be 5.0 mV/count over the lower portion of the curve, and 19.4 mV/count over the upper portion. A detailed study of the differential linearity yields a deviation of $< \pm 1$ count from perfect linearity. After optimizing these curves, we examined the behavior of the units for other input signals.

In figure 4, we show the typical response to a sawtooth input. The input waveform rises from -400 mV to 4.4V, exceeding the digitization range of the FADC, and has a period of about 15 μ sec. No missing codes are observed. By varying the position of this sawtooth within the FADC scan, we also find no coupling of the clock signal with the response to the sawtooth. The break in the slope of the digitized sawtooth is due to the bilinear response of the FADC.

Figure 4 - ADC counts versus time slice for a sawtooth input.

In figure 5, we show the response to a sine-wave of frequency about 3.5 MHz. Since the clocking frequency is close to an integral multiple of the input frequency, we obtain a "beat-frequency" pattern

ADC
Counts

Figure 5 - ADC counts versus time sample for ~ 3.5 MHz sine-wave input.

as shown. The asymmetric nature of the sine-wave envelop of this pattern is a result of our bilinear biasing of the FADC. Again no missing codes are observed. By increasing the frequency of the input

sine-wave we find the maximum analog bandwidth of our digitizing circuitry is 7.5 MHz.

Performance of the CAMAC Digitizers

Forty-eight channels of the CAMAC FADC digitizers were tested at CERN on a prototype HPC module. This module was constructed using a Pb-wire technique and has been described elsewhere.¹ It consists of 19 radiation lengths of lead composed of converters of effective thickness $0.475X_0$ separated by 40 gas sampling slots, each with a drift length of 66 cm. For the purposes of these tests 48 cathode pads covering the full depth of the calorimeter module were instrumented with a hybrid-circuit preamplifier. Twisted pair cabling was used to carry the output signal of the preamplifiers to pulse shaping circuits. The pulse shaping circuits broaden a narrow pulse to about 120 nsec (FWHM) so that when sampled at 15 MHz no information is lost. In addition pole-zero cancellation circuitry similar to that used on TPCs is incorporated to cancel the $1/T$ tail inherent in proportional chamber signals.

For each cathode pad, our digitizers provide pulse height versus drift time information. During these tests the HPC module was filled with a gas mixture of 80% Ar-20% CH_4 and had a magnetic field of

Figure 6 - Charge versus depth within the HPC for each of 48 Cathode Pads.
(a) A 35 GeV electron incident. (b) A 20 GeV positive pion incident.

1.0 Tesla applied parallel to the drift direction. An electric field of ~ 100 V/cm was also applied along the drift direction. Under these conditions a constant drift velocity of ~ 5 cm/ μ sec is obtained. In figures 6a and 6b we show the 48 pulse height versus drift length plots obtained for an incident 35 GeV electron (figure 7a) and an incident 20 GeV π^+ (7b). The position of a given histogram approximates the two dimensional location of the corresponding cathode pad. In this sense we have a three-dimensional representation of the charge deposited within the HPC. As shown in the figures, we clearly distinguish between the development of an electromagnetic shower, with its charge build-up in the longitudinal and transverse direction, and a non-interacting pion. (The vertical scales of the pion and electron events are not the same and the scales within the same figure have not been corrected for the different number of sampling slots covered by a given cathode pad.)

FASTBUS Design

In figure 7, we show a block diagram of a FASTBUS design with 32 channels mounted on a single 7-layer board. Aside from the increased number of channels, this layout differs from the CAMAC design by the inclusion of the zero-suppression circuitry and the four-event deep FEB. These additional circuits are replicated four times on the board; eight FADC/cache memory units are multiplexed into one zero-suppression/FEB unit. Storage of the data within the cache memory takes place 17 μ sec after input; storage in the FEB takes place 500 μ sec after input. Coupling to the FASTBUS is achieved using a TTL slave coupler developed at CERN.⁶ This board acts as a FASTBUS slave unit.

Detailed layout of this multilayer board indicated that we had to reduce the size of the FADC/cache memory units if we were to have 32 input-channels per board. Therefore we constructed a

Figure 7 - Logic Diagram for the FASTBUS FADC board.

Figure 8 - Baby Board for use in the FASTBUS design using the 20-pin FADC.

prototype FASTBUS version using a commercially available 5-layer Kluge board,⁷ and the 20-pin version of the FADC (TS8328). The Kluge board acts as a mother-board housing the control logic, zero-suppression logic and FEBs for all 32 channels. In figure 8, we show a redesigned baby-board which mounts on this mother-board. Of the four pins no longer available, one has no connection, one is the overflow bit, and one validates the data on the overflow bit. The fourth missing pin allows one to choose on which clock transition (rising edge or falling edge) the input data is sampled. In the 20-pin version we are constrained to use the rising edge. Since our design makes no use of the overflow bit, there is no loss of function in going to the smaller package.

The performance of these 20-pin FADC circuits has been studied in our laboratory and is comparable to that described earlier for the 24-pin version. The circuits are quiet, even at the sensitive end of the conversion scale. The noise level on a single d.c. level scan is < 5 mV. The digitized d.c. level is stable to within 2 mV for periods of 24 hours or more.

In the Kluge board design the FASTBUS coupler is mounted on a separate board and the two boards communicate via two ribbon cables. In the final design the coupler circuitry is on the same board as the digitizing electronics.

Summary

We have successfully designed and tested digitizing readout electronics for the DELPHI HPC using an 8-bit FADC operated in a multilinear mode. Both minimum ionizing particles and electromagnetic showers have been reconstructed using these electronics. A monolithic 7-layer FASTBUS board, which has 32 digitizer channels, zero-suppression and a four-event buffer memory has been laid out and a production test run of 20 boards (640 channels) is now scheduled. This pre-production run will enable us to make a crate level test of these digitizers on full-size HPC modules next spring.

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References

- [1] E. I. Rosenberg, "The DELPHI High Density Projection Chamber", Proceeding of the Gas Sampling Calorimetry Workshop II, Fermilab, Batavia, IL, (1985) p. 450 and references therein.
- [2] H. B. Crawley et al., IEEE Trans. Nucl. Sci. NS-33, 888 (1986).
- [3] Thomson Semiconducteurs, 43 Avenue De L'Europe, 78140 Velizy-Villacoubley, France.
- [4] Cypress Semiconductor Corporation, 3901 North First Street, San Jose, CA 945134.
- [5] Toshiba America, Inc. 2692 Dow Avenue, Tustin, CA 92680.
- [6] G. Frémont, "A FASTBUS Prototyping Card Incorporating a Comprehensive TTL Slave Coupler", CERN-EP, July 1986.
- [7] Kinetic Systems Corporation, 11 Maryknoll Drive, Lockport, IL 60441.