Development of a highly selective muon trigger exploiting the high spatial resolution of monitored drift-tube chambers for the ATLAS experiment at the HL-LHC

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Abstract

The High-Luminosity LHC will provide the unique opportunity to explore the nature of physics beyond the Standard Model. Highly selective first level triggers are essential for the physics programme of the ATLAS experiment at the HL-LHC, where the instantaneous luminosity will exceed the LHC design luminosity by almost an order of magnitude. The ATLAS first level muon trigger rate is dominated by low momentum muons, selected due to the moderate momentum resolution of the current system. This first level trigger limitation can be overcome by including data from the precision muon drift tube (MDT) chambers. This requires the fast continuous transfer of the MDT hits to the off-detector trigger logic and a fast track reconstruction algorithm performed in the trigger logic. The feasibility of this approach was studied with LHC collision data and simulated data. Two main options for the hardware implementation will be studied with demonstrators: an FPGA based option with an embedded ARM microprocessor and an associate memory chip base option. In this note the basic MDT trigger concept and the design of a demonstrator for the two hardware options are presented.

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1. The MDT trigger concept

Highly selective low- p_T muon triggers are mandatory for the exploitation of the physics potential of the High-Luminosity Large Hadron Collider (HL-LHC). At the LHC the ATLAS experiment[1] uses coincidences of hits in fast trigger chambers, resistive-plate chambers (RPC)s in the barrel part ($|\eta| < 1.05$) of its muon spectrometer and thin-gap chambers (TGC) in the end caps ($1.05 < |\eta| < 2.4$). The spatial resolution of the trigger chambers allows for a rough estimate of the muon transverse momentum p_T . However, as the inclusive muon cross section is steeply falling with p_T , an improved momentum resolution at trigger level leads to a significant reduction of the single muon trigger rates at p_T thresholds around 20 GeV.

The ATLAS experiment plans two upgrades of its muon system to optimize the performance of its muon trigger at the HL-LHC [2, 3]:

1. The installation of a layer of triplets of thin-gap resistive plate chambers (RPC) in the inner layer of the barrel part of the muon spectrometer to increase the acceptance of the barrel muon trigger system from 78% to 96%.
2. The use of precision muon drift-tube (MDT) chamber data in the first level muon trigger to improve the muon momentum resolution for the sharpening of the muon trigger turn-on curve and to reject triggers from accidental coincidences in the trigger chambers system.

The rejection power for subthreshold muons by an MDT based trigger was studied with simulated data for a trigger threshold of $p_T > 20$ GeV. Figure 1 shows the efficiency of the planned first-level muon trigger using both the RPC and TGC trigger chambers and the precision MDT chambers normalized to the efficiency of a trigger system which uses only the RPC and TGC data. The MDT trigger rejects most of the triggers for muons with a p_T below the 20 GeV threshold and accepts all the muons with a p_T above the threshold. The MDT trigger reduces the trigger rate from about 100 kHz to about 25 kHz.

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Figure 1: Efficiency of the ATLAS single muon trigger using the data of the RPC and TGC trigger detectors and the precision MDT chambers normalized to the efficiency of the RPC and TGC only trigger system. [3]

2. MDT trigger data flow

In order to minimize the muon trigger latency all MDT hits will be streamed off the MDT chambers via gigabit links to off-detector MDT trigger processor ATCA blades. The MDT data of one trigger sector will be processed on one blade. The muon spectrometer consists of 16 barrel sectors and 16 end-cap sectors in each hemisphere so that 64 MDT trigger processor blades will be used in the muon trigger system.

On the MDT trigger blade the MDT hits are buffered. When the blade receives a trigger from the RPC or TGC trigger chamber system, the MDT hits will be matched to the spatial region and the pp collision time of this trigger. The times of the matched hits are then converted into drift radii which are used to reconstruct straight track segments in each MDT chamber in the trigger region. If segments in three chambers have been reconstructed one can compute the sagitta, i.e. the deviation of the segment position in the middle chamber from the straight-line interconnection of the segment positions in the inner and outer chamber. The sagitta allows for the p_T measurement with about 4% resolution which is close to the offline p_T resolution of the muon spectrometer. If only segments in two chambers have been found one can take the difference of the directions of the segments in these chambers as a measure for the deflection of the muon in the magnetic field of the muon spectrometer and reach a p_T resolution of about 8%. The p_T measurement of the MDT trigger processor is then used for the first-level muon trigger decision. The overall latency of the first-level muon trigger is found to be less than 4.2 μ s. [3]

3. MDT trigger demonstrator ATCA blade

An MDT trigger demonstrator blade is in preparation for the end of 2018. It consists of an ATCA carrier card which houses a powerful XILINX Ultrascale FPGA for the hit matching and the calculation of drift radii (see Fig. 2). The hardware for the segment reconstruction and p_T calculation will sit on a daughter board. This design has been chosen to be able to study and compare two different hardware options for the segment reconstruction: pattern recognition and segment fitting on an FPGA; pattern recognition on an associative memory chip and segment fitting on an FPGA.

In both cases the ARM microprocessor embedded into a XILINX Zynq FPGA will be used for the p_T computation. In the first approach the MDT trigger processor can be built out of commercial components. Because of the availability of all components this is the baseline option. The second approach intends to share the associative memory ASIC with the inner detector track trigger system. The hardware demonstrator will allow for a comparison of both approaches in terms of trigger efficiency, trigger latency, and power consumption.

Figure 2: Schematic drawing of the MDT trigger processor blade which consists of an ATCA main board which houses an FPGA for the hit matching and a daughter board for the segment reconstruction and p_T calculation.[3]

Two different segment reconstruction algorithms have been proposed for the baseline hardware option. A straight line is defined by two parameters: a position and a direction. In the so-called “Legendre transform method” [4] one scans over both the position and the direction parameter around the seed values from the RPC and TGC system to determine the segment parameters best compatible with the drift radii of the MDT hits. This method does not require the calculation of the exact position of the hits along the perimeter of the drift circle nor involve linear fits. In the other method, the so-called “compact segment finder” [5] the direction parameter is given by the sector-logic seed value and the scan is performed only over the position parameter to identify the MDT hits belonging to a segment. The precise values of the segment parameters are obtained by a least square fit to these MDT hits. While the Legendre transform method aims at minimum latency at the price of a lot of FPGA resources, the compact segment finder is optimized for minimum FPGA resource usage taking into account a slightly higher latency and provides a segment quality estimator by the χ^2 of the least-square minimization.

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