Module and System test Development for the Phase-2 ATLAS ITk Pixel Upgrade

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Abstract

In the high-luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of ITk will consist of a pixel detector, with an active area of about 14 m². In order to cope with the changing requirements in terms of radiation hardness, power dissipation and production yield, several different silicon sensor technologies will be employed in the five barrel and end-cap layers. With the arrival of the first readout chip prototype, the RD53A chip, the development of hybrid detector modules is starting to address numerous production issues, understanding of which will be crucial for the final design and production of the ITk pixel detector modules. In addition, the new powering scheme is serial which introduces further challenges. A large prototyping program on system test level is ongoing. Components for larger structures with multiple modules, based on the FE-I4 front-end chip, which is currently used in the Pixel detector, were produced and are in assembly and evaluation. The paper will present the latest results from the assembly and characterization of prototype modules as well as the latest evaluation and results of thermo-mechanical prototypes and fully electrical prototypes.

Keywords: Detector, Module, System Test, ATLAS, Upgrade

1. Introduction

The Phase-II Upgrade for the ATLAS [1] detector at the Large Hadron Collider (LHC) at CERN takes place in 2024-26 when LHC enters the high-luminosity era. The machine will deliver a 5-7 times higher instantaneous luminosity of up to $7.5 \cdot 10^{34} \frac{1}{\text{cm}^2\text{s}}$, resulting in about 200 proton-proton interactions per bunch crossing. The increased instantaneous luminosity leads to a higher particle fluence and with this a much higher particle density in the detector systems. The detector components need to withstand a particle fluence of $2 \cdot 10^{16} \frac{1\text{MeVn}_{\text{eq}}}{\text{cm}^2\text{s}}$ and radiation levels up to 10 MGy. Because the current components of the ATLAS inner detector will not withstand this harsh environment, the old inner detector will be replaced by a

new all silicon Inner Tracker (ITk) in long shutdown LS3 around 2025, called Phase-II upgrade.

2. The ATLAS Pixel Detector Upgrade

2.1. ITk Layout

The ITk consists of an outer strip part and an inner pixel part [2], [3]. Overall, each crossing particle creates 13 hits in ITk to be recorded and used for particle tracking. The ITk layout can be seen in Figure 1. The Pixel part of the ITk consists of five layers and can be grouped into three parts. The inner system built up from the inner two layers will be exchangeable to overcome the radiation hardness limit of the installed electronics, which is guaranteed to withstand a radiation level of up to 5 MGy. The barrel section of the outer three layers is named Outer Barrel and the Outer End-cap is formed by the ring part of the outer three layers. All electronics and mechanics need to withstand a

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Figure 1: ITk layout. Depicted is a quarter section of the ITk detector. In blue the strip part is visible, while the red part is the pixel detector [2].

harsh irradiation environment. In Figure 2 the expected fluences are shown.

Figure 2: Simulated fluences for the ATLAS ITk detector [2].

2.2. The ITk module and its components

Each layer holds a number of hybrid Pixel modules, consisting of a silicon sensor and front-end ASICs mounted to each other by bump bonding. To cope with the higher particle occupancy to be expected the granularity of the pixel detector is increased by reducing the sensor pixel size from $50 \times 250 \mu\text{m}^2$ used in the current innermost layer of the ATLAS Pixel detector to be $50 \times 50 \mu\text{m}^2$ or $25 \times 100 \mu\text{m}^2$ in ITk. The final pixel size choice is currently under discussion.

The sensor type being used depends on the layer. While in the innermost layer (layer 0) 3D sensors with a bulk thickness of $100 \mu\text{m}$ will be installed, the other layers will be equipped with planer sili-

Figure 3: Quad ship FE-I4 module for test system usage.

con sensors of either $100 \mu\text{m}$ in layer 1 or $150 \mu\text{m}$ thickness in all the other layers.

The front-end ASIC is designed by the RD53 collaboration and will be realized in 65 nm technology [4]. It provides 153600 pixels arranged in 400 rows and 384 columns. A current prototype, the RD53A chip, is being used to demonstrate the feasibility of realizing the ATLAS ITk Pixel detector. To be able to read out the much higher amount of data recorded in the front-end ASICs, the readout bandwidth of the RD53 ASICs will be 5.12 Gbps organized in four lanes operating at 1.28 Gbps.

There will be two different module sizes: Single chip modules for the innermost layer and quad chip modules for all other layers. Three single chip modules will be grouped together for powering and clock and command. A quad chip module is shown in Figure 3.

2.3. Serial Powering

The powering of the about 9500 ITk Pixel modules will be done using serial powering [5], [6]. A number of modules will be powered within the same serial powering (SP) chain. A common power line supplies a constant current to the SP chain and each module creates the internally needed voltages from this using an internal shunt low drop out regulator (shuntLDO) [7]. As a consequence each of the modules inside an SP chain operates at a different potential, which requires AC-coupling of each communication line. The sensor bias voltage is supplied in parallel to a couple of modules inside an SP chain and shares its return line. Therefore, each sensors bias voltage is referenced to the local module ground.

This powering concept is new and needs careful evaluation and testing in terms of operation of the modules and impact of disturbances on the performance of the detector modules. Several demonstrator setups have been built to investigate the serial powering operation in detail.

Figure 4: Electrical test structure with seven FE-I4 quad chip modules mounted to a carbon support structure.

3. Prototypes and Demonstrator Setups

To demonstrate and verify the cooling capability of the local support structures, thermal prototypes are used. Heaters have been glued to local support structures and the temperature while being powered and cooled were measured. The results are still being analyzed but indicate the expected cooling behavior.

3.1. FE-I4 based Electrical Demonstrators

For the Outer Barrel and the Outer End-cap test setups with up to 13 FE-I4 ([8]) quad chip module have been built. Because the RD53A modules are still in production, the test setups were based on the former front-end ASIC, the FE-I4, which is used in the current ATLAS pixel detector and provides a shuntLDO for serial powering. Studies of the powering strategy and the module behavior within an SP chain have been performed. Different sources of disturbances have been investigated and their impact on module performance was measured. Figure 4 shows the electrical 7-cell setup operated at CERN, while in the UK a 13 module setup has been set up.

Figure 5: Noise measurement for the modules on the 7-cell structure. Module are of lower quality for testing purposes. Therefore some ASICs are not working or show a higher noise behavior

The measure for good operation is the module performance in threshold and noise. Differences due to in-coupled disturbances from either noisy modules or noise induced by busy bus lines on the connection flex circuit have been investigated.

Figure 6: Threshold measurements for modules on demonstrator under different test scenarios.

Figure 7: Noise behavior of modules on a demonstrator in different configurations.

The first larger scale prototype which has been built is the 7-cell structure. Because this setup served also for module loading tests, only modules which have a reduced performance have been used. A measurement of the noise after loading onto the support structure is shown in Figure 5. Most working ASICs show a homogeneous noise behavior as expected. The module performance has been first measured without any disturbance and then with either an artificial noisy ASIC on one module or a very busy communication bus on the connection flex. None of the disturbances had any effect on threshold and noise of the measure modules as can be seen in Figures 6 and 7.

For the End-cap prototype comparable measurements have been performed and again the noise has been used as indicator of mis-behavior, Figure 8 shows that the noise in all the different configurations and measurements is comparable and therefore no impact of any disturbance could be identi-

Figure 8: Measure noise of module on the End-cap prototype structure. All measurements show a good agreement and no external disturbance has a negative impact on the module performance.

fied. This in summary shows a very stable operation of modules being mounted on a local support structure and powered in a serial powering chain.

4. Further Large Scale Prototypes

All the current large scale prototype setups are based on the old FE-I4 ASIC. In the middle of 2019, modules made from the RD53A prototype ASIC are expected. These will be used to construct several further larger scale setups for different purposes.

As the RD53A ASIC has a different shuntLDO, which is a revised and updated version of the one in FE-I4, the serial powering can be tested in a more realistic scenario. It is expected that there are many things to discover and learn about this powering scheme still. Operating up to 16 RD53A modules in a chain will be a very important milestone for this powering scheme implementation.

Furthermore, reading out RD53A modules is very different from FE-I4 modules and requires a read-out system close to the final one. Therefore, read-out of multiple modules from an SP chain at high bandwidth is to be prepared and studied with the upcoming test systems.

Powering and readout tests can be done using a very generic setup independent from the local support species. Nevertheless, there are prototype setups with loaded local supports foreseen for each of the sub-parts of the ITk Pixel detector to gain experience with module building, shipping, loading, and operation. Also the whole logistics chain for the final production will be tested and optimized in this context. Figure 9 shows prototype construction for the End-cap ring system.

Figure 9: Prototype construction for the End-cap ring. Modules are mounted to a carbon support ring. Up to 13 modules will be placed on a double-sided half-ring.

5. Conclusion

Measurements on several prototype setup for the ATLAS ITk Pixel detector show a stable performance of the prototype modules in serial powering operation. Test of module building and the logistic chain needed during production has been examined and optimized. Further demonstrator setups constructed from the next front-end ASIC prototype (RD53A) are foreseen for mid of 2019, which is the first step from R&D into production phase.

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