ATLAS LAr Calorimeter Performance in LHC Run 2 and Electronics Upgrades for next Runs

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Abstract

Liquid argon (LAr) sampling calorimeters are employed by ATLAS for all electromagnetic calorimetry in the pseudo-rapidity region $|\eta| < 3.2$, and for hadronic and forward calorimetry in the region from $|\eta| = 1.5$ to $|\eta| = 4.9$. In the LHC Run 2 about 150 fb^{-1} of data at a center-of-mass energy of 13 TeV have been recorded. The well calibrated and highly granular LAr Calorimeter reached its design values both in energy measurement as well as in direction resolution. Electronics developments are pursued for the trigger readout of the ATLAS LAr Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period between December 2018 and early 2021. Trigger signals with finer spatial granularity and higher precision are needed in order to improve the identification efficiencies of electrons, photons, taus, jets and missing energy, at high background rejection rates, already at the Level-1 trigger. Following new TDAQ buffering requirements and high expected radiation doses in the pileup conditions of the high-luminosity LHC, the LAr Calorimeter electronics will be further upgraded (Phase-II) to readout the full 182,500 calorimeter cells at 40 MHz with 16 bit dynamic range. Developments of low-power preamplifiers and shapers to meet these requirements are ongoing in 130 nm CMOS. In order to digitize the analogue signals on two gains after shaping, radiation-hard, low-power 40 MHz 14-bit ADCs are developed using a SAR architecture in 65 nm CMOS. This contribution gives an overview of the detector operation, changes in the monitoring and data quality procedures, to cope with increased pileup, as well as the achieved performance. Results of ASIC developments including quality assurance and quality control (QA/QC) and radiation hardness evaluations, performances of the pre-production boards and results of the system integration tests, progress of QA/QC of final production boards are presented along with the overall system design for the Phase-I upgrade. Results of tests of the first prototypes of front-end components are presented, along with design studies on the performance of the off-detector readout system for the Phase-II upgrade.

1. The ATLAS LAr Calorimeter and Run 2 Performance

The liquid argon calorimeter (LAr) is an ATLAS [1] sub-detector responsible for reconstructing the energy of physics objects such as jets, electrons, photons, and taus, as well as measuring missing transverse energy (MET). It is a sampling calorimeter that uses liquid argon as its active medium. It covers up to 4.9 in $|\eta|$, and has 182,500 channels collecting signals from the full detector. There are 1,524 Front End Boards (FEBs) that read out the electromagnetic shower signals deposited in the detector, provide amplification, shaping, and gain selection. Signals are then stored in analog memory on the FEBs while summed signals from each of the four sampling layers of the calorimeter (Presampler, Front, Middle, and Back layers) are sent to the lowest level trigger in ATLAS (L1 calorimeter trigger, or L1Calo) for a readout decision. If a Level 1 accept is sent, signals are digitized on the FEBs and sent off the detector via optical links.

Nearly all physics analyses using ATLAS data depend on some subset of energy measurements provided by the LAr calorimeter, therefore good energy resolution and high data taking efficiency are crucial. LAr achieved a data quality efficiency

of over 99% each year during the period of the Run 2 data taking. Each year, there were fractions of percents of data lost due to problems such as FEB desynchronization, high voltage (HV) trips, and noise bursts in the detector occurring when no energy deposits are expected. This small amount of data rejected by LAr is vetoed based on the duration of the effect.

Shorter effects (lasting typically on the order of milliseconds) are rejected using a time-window veto with several milliseconds buffer before and after the effect. As seen in Figure 1, these come from issues such as FEB desynchronization, high voltage trips, holes in coverage, and noise. For longer lasting effects, a full luminosity block is rejected (typically around 1 minute). Sources of this type of veto are presented in Figure 1 and are comprised mainly of noise bursts.

The extremely high efficiency and excellent performance of LAr is achieved through the combination of a hardworking operation team, smoothly running monitoring tools that allow for quick detection of any data quality or hardware issues, and several online software applications that automatically detect and solve issues in real time. One example of such an application is the LAr Trigger Tower Noise Killer (LTTNK). The LTTNK monitors trigger tower rates, specifically looking for rates that are too high for the Level 1 calorimeter trigger (L1Calo) to deal with. If such a rate is detected, the LTTNK disables each cell in

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Figure 1: Percentage of luminosity vetoed due to minute-length veto periods (upper) and sub-minute veto periods (lower) per year in Run 2. Different colors represent different occurrences affecting data quality [2].

the trigger tower sequentially, rechecking the tower rate, until it finds the culprit cell and the rate returns to normal.

2. LAr Phase-I Upgrades

During Long Shutdown 2, the LHC will be upgraded in preparation for Run 3. The luminosity delivered in Run 3 will be significantly higher than in Run 2, with an average number of interactions per bunch crossing (average pileup) of roughly 2.5 times the average in Run 2. This poses a challenge to ATLAS data collection. The higher pileup conditions in Run 3 will degrade particle isolation and resolution, which would lead to a lower trigger efficiency. Furthermore, due to hardware constraints, the L1 trigger rate must be kept at around 100kHz. This rate could be maintained by increasing energy thresholds on L1 trigger objects; however, this is extremely undesirable due to the consequences it will have on physics analyses, especially those that depend on low p_T objects. Instead, the L1 trigger in ATLAS will be upgraded, using more offline-like algorithms at the lowest level to improve efficiency against the harsher LHC conditions [3].

The upgraded L1 system will implement feature extractor (FEX) modules that use topological shower shape estimators to improve discrimination between physics objects such as electrons and jets. The electron feature extractor (eFEX) module will identify isolated electron, photon, and tau candidates, while the jet feature extractor (jFEX) module will identify jet candidates and calculate E_T and missing E_T for each bunch crossing. The new shower shape variable definitions, as defined in Ref. [3], are given below. The formation of these variables relies on digitized signals from Super Cells in the LAr calorimeter, which are formed by $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ groups of cells in the Presampler and Back layers, and $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ groups in the Front and Middle layers.

- R_η - The transverse energy measured in a 3×2 group of Super Cells in $\Delta\eta \times \Delta\phi$ centered around the highest-energy cell in the Middle layer divided by the transverse energy of a 7×2 group centered around the same cell.
- f_3 - Ratio of transverse energy in a $\Delta\eta \times \Delta\phi$ area of 0.2×0.2 in the Back EM layer to that deposited in all three layers for one EM cluster.
- $w_{\eta,2}$ - The spread of a shower in the Middle EM layer in a 3×2 Super Cell region.

Figure 2: Shower shape variable $w_{\eta,2}$ for jets and electrons (upper) and impact on L1 trigger rates as a function of L1 EM E_T cut for 95% electron efficiency working point (lower) [3].

Discrimination power between jets and electrons for one of the variables as well as the impact on the L1 trigger rates as a function of L1 EM E_T cut (for 95% electron efficiency working point) can be seen in Figure 2. Forming these new shower shape discriminators requires access to finer granularity, digitized information from the LAr calorimeter. Instead of sending summed layer information from Trigger Towers, which are formed by $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ cells summed across layers, in Run 3 LAr will send information from Super Cells, which are defined previously. Smaller segmentation in $\Delta\eta \times \Delta\phi$ as well as

the preservation of layer information will provide an increase of about a factor of 10 in calorimeter information granularity sent to the L1 trigger. This change in segmentation is depicted in Figure 3.

Figure 3: Energy deposited from an electron with $E_T = 70$ GeV in a single Trigger Tower in red, as seen by the current Level 1 Calorimeter trigger (left) and the same energy deposition as seen by the upgraded trigger electronics (right). [3].

In order to read out and digitize finer granularity information, the LAr trigger read-out path must be upgraded [4]. During the LS2, 124 new LAr Trigger Digitizer Boards (LTDBs) will be installed in the front end crates, as well as new Layer Sum Boards (LSBs) and a new baseplane in each crate. The legacy trigger read-out path will be preserved during these upgrades, thus the LTDBs will form the legacy layer sum signals in addition to the digitized signals from the Super Cells. The LTDBs use commercial, off-the-shelf components for the analog section that first shapes the signals and selects the appropriate gain to utilize the full ADC, as well as performing the signal sums that are then sent to the Tower Builder Boards to preserve the legacy trigger readout system. Signals are then digitized at a rate of 40 MHz by ADCs that are implemented as custom ASICs in 130nm CMOS with a 4-bit pipeline and 8-bit SAR. A two-channel serializer, the LOCx2, implemented in 250 nm silicon-on-sapphire CMOS technology, multiplexes and serializes the signals before they are sent off-detector via optical transmitters.

Off-detector, the LDPS receives the digitized signals, and transmits E_T and missing E_T calculations to L1Calo. The LDPS is comprised of 31 LAr Digital Processing Blades (LDPBs) which are housed in 3 ATCA crates that allow for efficient handling of the large expected data volume. Each blade is comprised of an ATCA carrier board with four advanced mezzanine cards, each of which is built around one high-bandwidth FPGA.

In 2015, two demonstrator boards were installed in-situ in the LAr calorimeter EM barrel A-side and run parasitically in order to validate the design and demonstrate the feasibility of the upgrade system. Two LTDBs, each reading out 320 Super Cells, digitized Super Cell signals which were then read out but two LDPB prototype boards. This system was upgraded in 2018 with a newer LTDB prototype. Energy measurements calculated from Super Cells compared to that of the main readout, as well as calibration pulse shapes from each of the four sampling layers read out by the demonstrator system, can be seen in figure Figure 4.

As of the start of LS2, installation has begun, starting with

Figure 4: Scatter plot showing energy of cells from the main readout vs. Demonstrator Super Cell energy (upper) and calibration pulse shapes in each of the four sampling layers read out by the Demonstrator (lower) [5].

the EM Endcap Front End Crates, where all FEBs and boards have been removed to allow for the installation of the new baseplanes.

3. LAr Phase-II Upgrades

After Run 3, the LHC will shut down again to start upgrades for the High Luminosity LHC (HL-LHC). The challenges faced by ATLAS in this phase of LHC running will be even greater than those faced in Run 3. The total luminosity delivered over the 12 year period is expected to reach up to 4000 fb^{-1} with an average pileup of up to 200 - between 5 and 7 times that of Run 2. To avoid degraded trigger performance, the whole ATLAS trigger system will be upgraded [6].

A Level 0 (L0) trigger based off of the existing L1 trigger will be introduced, as well a new Global Trigger which will implement more offline-like algorithms to improve performance against pileup. The L0 accept rate will be between 1 and 4 MHz with latencies of $10 \mu\text{s}$ and $35 \mu\text{s}$ for the L0 and L1 triggers, respectively. To be compatible with the new ATLAS trigger and data readout system, the full LAr electronics readout must be replaced [7].

The LAr Phase-I and Phase-II upgrades have been planned as a staged upgrade, meaning that the upgrades done in preparation for Run 3 will be fully compatible with those done in

preparation for the HL-LHC. This second stage includes the instalment of 1524 new Front End Boards (FEB2s), 130 new Calibration boards, new front end powering, and a new off-detector readout consisting of 190 LAr Signal Processors (LASPs) and 18 LAr Timing System blades (LATS). R&D efforts are underway for the electronics upgrades with many efforts building upon developments for Phase-I.

Each new FEB2 will read out 128 calorimeter channels and digitize the full detector granularity at the bunch crossing rate. The analog section of each FEB2 consists of a pre-amplifier and shaper implemented in a single ASIC. A first version of this ASIC, the LAUROC0, was tested successfully and two new versions, the ALFE and LAUROC1 were submitted in late 2018 with test board fabrication following shortly after. The LAUROC1 consists of a 4-channel preamplifier+shaper, all with two gains, while the ALFE has two channels, each with two gains. First tests were promising, showing low noise, low power consumption, and good linearity. The test board for the LAUROC1 and the submitted design of the ALFE can be seen in Figure 5.

Figure 5: LAUROC1 test board (left) and ALFE design (right).

Digitization is done by a 14-bit dynamic range ADC with two gain scales which operates at 40 million samples per second and is radiation tolerant beyond 4000 fb^{-1} . There are several options being considered for this ADC. The baseline option is a fully custom ADC design in 65 nm CMOS technology from TSMC. To reach 14-bits, it uses a Dynamic Range Enhancer (DRE) with 4x internal gain, and a 12-bit pipeline Successive Approximation Register (SAR) ADC. It has low power consumption of between 15-20 mW and ENOB of > 11.2 bits. Two other options, a semi-custom IP-block design and a COTS option, are also being considered. The block diagram for the custom ADC option (the COLUTA) as well as a testboard for the chip are shown in Figure 6. After digitization, signals are sent off-detector via optical links using an lpGBT protocol.

Figure 6: Block diagram for fully custom ADC option, COLUTA (left) and picture of the testboard (right).

The off-detector LATS will distribute trigger, timing, and

control information as well as send configuration signals to the Calibration boards and FEB2s. Though its conceptual design is still in progress, the LATS will consist of 18 ATCA blades, each with 16 timing and control FPGAs and one main FPGA. The LASPs will replace the readout drivers currently receiving signals off-detector. Each LASP will receive digitized data from four FEBs, then apply digital filtering and buffer the data while awaiting a trigger decision. LASP test board development is currently underway, as are transceiver tests.

4. Conclusion

LAr performed excellently in Run 2, maintaining a very high data taking efficiency of over 99% each year. As conditions at the LHC become more challenging in Run 3 and the HL-LHC, ATLAS and LAr will make upgrades in order to maintain this excellent performance. Phase-I upgrades are already underway. Replacement of the baseplanes in each Front End Crate has begun, and is followed by the reinstallation of the main data readout electronics as well as the legacy trigger read-out and the new Super Cell readout electronics. Installation is going smoothly and is on schedule. A significant amount of R&D work has been done in preparation for the Phase-II upgrades, during which the main data readout path will be updated, along with the calibration boards and front end powering. These upgrades are fully compatible with the Phase-I upgrades, and good progress is being made.

5. Acknowledgements

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