A FET BASED FREQUENCY AND DUTY FACTOR AGILE 6 kV PULSE GENERATOR

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SCAN/9408179

Abstract

A pulse generator has been developed which has many potential applications. The pulse generator consists of a high-voltage modulator incorporating two stacked Field-Effect Transistor switches operating in a "push-pull" mode. A continuous 1 kV to 6 kV pulse train has been obtained with a prototype pulse generator over a frequency range from 1 Hz to 20 kHz. Pulse widths in the range from 250 ns to 1 s have been achieved with rise and fall times of 30 ns into a capacitive load of 26 pF. A 3 kHz, 5 kV version of this pulse generator has been installed and tested in the 300 keV injection line for the 500 MeV TRIUMF cyclotron. The circuit performance was evaluated with the aid of PSpice in the design stage and confirmed by measurements in the prototype. Results of measurements and simulations are presented.

Introduction

The Ion Source Injection System (ISIS) at TRIUMF requires a variable duty factor beam chopper for tuning purposes[1]. Specifications for the ISIS beam chopper call for a 5 kV voltage pulse, a pulse duration continuously variable in the range from 333 ns to 1 ms, a repetition rate continuously variable between 1.0 kHz and 3.0 kHz, and rise and fall times (10 % $\rightarrow$ 90 %) not to exceed 43.4 ns.

A prototype 1 MHz pulse generator was designed and built for the now defunct KAON Factory. Unipolar 7 kV pulses were generated and stored on a 50 Ω coaxial cable: the 1 MHz pulses were shaped using two 150 kW tetrodes[2]. However the rise and fall times ($\sim$ 100 ns) were limited by the excessive stray capacitance associated with the tetrodes. A single-tetrode bipolar 15 kV version[3] was tested, and rise and fall times of less than 40 ns were achieved. There is a potential application at TRIUMF for a 15 kV unipolar pulse generator, operating at approximately 1 MHz (continuous), to change the pulse structure of the 500 MeV proton beam[4]. A FET based pulse generator, which would have a much reduced stray capacitance compared with tetrodes, would permit the storage of unipolar pulses on a coaxial cable without excessive power drain, while maintaining good rise times.

Design

A solid state switch consisting of two stacks of high voltage FETs, operating in "push-pull" mode, has been designed, built and successfully tested. The design of these switches is based on a stacked FET switch developed at Saskatchewan Accelerator Laboratory (SAL)[5]. However the design has been modified considerably[1].

The beam chopper consists of three stages to convert a TTL timing signal to a 6 kV pulse. The first stage converts the TTL signal to 60 V; the second stage converts the 60 V signal to $\pm$ 250 V; and the final stage generates a +6 kV pulse. The second and final stages are edge triggered. The three stages of the pulse generator can act to sharpen the edges from the previous stage, so that the final stage turns on and off cleanly.

The two stacks of the final stage of the prototype pulse generator each consist of 7 modules (Fig. 1). The 7 modules of the pull-up stack are labelled UP1 through to UP7 in Fig. 1, corresponding to the +6 kV DC end of the stack, and the output end, respectively. The modular design is convenient from a maintenance viewpoint and can be expanded for higher voltage applications.

The 7 modules of the pull-down stack are labelled DN1 through to DN7 (Fig. 1), corresponding to the ground end of the stack, and the output end, respectively. Fig. 1 shows 14 resistors whose value is 29 Ω : these resistors interconnect the source (OUT-) of one stage with the drain (OUT+) of the adjacent stage. The purpose of these resistors is to limit the peak drain current through the power FET's to within rated value, for example in the event of a fault condition in which the pull-up and pull-down stack are momentarily turned on together.

The details of switch modules UP1 through to UP7 and DN1 through to DN7 are shown in Fig. 2. The gate drive circuit (Fig. 2) is based on a standard high noise immunity HEXFET driver circuit [6]. However this circuit [6] does not work reliably with sub micro-second pulses, due to the long recovery time ($\sim$ 100 ns data-sheet value) of the intrinsic reverse P-N junction diode of the IRFD110 FET (anode of the intrinsic diode is the source, and cathode is the drain). A diode (1N4148), which has a short recovery time ($\sim$ 4 ns data-sheet value), is connected in series with the drain of each of the IRFD110 FETs: this diode is connected in the opposite polarity to the intrinsic body diode, hence preventing the body diode from conducting when the IRFD110 is reverse biased (Fig. 2). Another 1N4148 is connected in parallel with the IRFD110/1N4148 series arrangement (Fig. 2). The combination of the two diodes essentially bypasses the intrinsic diode of the IRFD110, and replaces it with more ideal components.

The high-power FET utilized in each module of the power modulator is the APT1004RBN[7]. At 25°C the APT1004 FET is rated at 1 kV, a pulsed drain current of 17.6 A (at a 10 % duty factor), and a power dissipation of 150 W. The APT1004 FETs procured are all from one "lot": this ensures that the APT1004 FET's in the stacks, together with the spare APT1004's, have similar characteristics (e.g. similar turn on/off delays[5]).

The APT1004 FET has an appreciable (27 nC maximum data-sheet value) 'Miller' (gate-drain) charge[7]. In order to achieve the specified rise and fall times it is necessary to charge and discharge, respectively, the reverse transfer capacitance rapidly. In order to achieve rise and fall times of 30 ns, a significant gate current ($\sim$ 2 A peak) is required: however the resulting gate-source voltage rating of the APT1004 ($\pm$ 30 V) and the IRFD110 FETs ($\pm$ 20 V) could be exceeded.

Back-to-back zener diodes are connected in parallel with the secondary winding of the pulse-transformer (Fig. 2) to limit the maximum gate-source voltage of the FETs. Two parallel sets of back-to-back zeners are utilized in order to reduce the transient impedance, and thus further limit the maximum gate-source voltage of the IRFD110 and APT1004 FETs. The breakdown voltage

The size and geometry of the metal cabinet which houses the FET stacks is chosen such that the parasitic capacitance from each module to ground is a small fraction of the drain-source capacitance. For example the 'high-voltage' drain-source capacitance of each of the seven APT1004 FETs in a stack is approximately 90 pF and the parasitic capacitance from drain to ground is approximately 4 pF per module ($k=0.044$). The resultant drain-source voltage at the 'pulsed' end of the FET stack could be more than 2 times larger in magnitude than that of the 'DC' end of the

stack, during a transient, if corrective measures are not taken[9]. The severity of the voltage transients in the stack are reduced by connecting a fast-grading capacitor (C_{fg}) between the drain and source of the APT1004 FET at several modules of each stack. Analytical equations have been derived to calculate the values of fast-grading capacitors which would give ideal voltage distribution in the stacks[9]:

$$C_{fg(n)} = C_{m(1)} \sum_{i=1}^{n-1} i k \quad (8)$$

where: $C_{fg(n)}$ is the value of the fast-grading capacitor required to be connected between the drain and source of the APT1004 of module 'n'; and $C_{m(1)}$ is the [linearized] drain-source capacitance of the APT1004. No fast-grading capacitor would be connected across module 1.

In order to avoid excessive drain current in the APT1004 FET during turn-on it is necessary to connect a fast-grading resistor (R_{fg}) in series with each fast-grading capacitor. The value of this resistor (330 Ω) is a compromise between a 'small' value so as not to unduly 'undo' the beneficial effect of the fast-grading capacitors, and a 'large' value to limit inrush current into the APT1004 FETs during turn-on.

The fast-grading capacitor and resistor are connected on the back-plane, and not on the PCB cards. This ensures that, although the value of the fast-grading capacitor varies down the stack, the PCB cards in the two stacks are all identical. The nominal value of the fast-grading components utilized are shown on Fig. 1. Modules UP1, UP2, DN1, and DN2 do not require fast-grading components. The nominal values of the fast grading capacitors used varies from 68 pF at the deflector plate end of the stack to 10 pF across modules UP3 and DN3 (see Fig. 1).

A resistor connected between the drain and source of the APT1004 FET (Fig 2) ensures that the DC voltage grading down the stack of FETs is adequate. A grading resistor of value 340 k Ω (two parallel 680 k Ω resistors, each of 2 W) provides adequate current (~ 2 mA) for LEDs, which are connected in series with the DC grading resistors for diagnostic purposes (Fig. 2). If an APT1004 FET fails to a short circuit (the usual mode of failure) there is negligible voltage across the associated DC grading resistor, and hence the LED does not light. Provision has also been made on the PCB cards for high-speed fibre optic transmitters which can be used for diagnostic purposes. If these high-speed transmitters are used it will be necessary to increase the LED current to 3 mA. Hence provision has been made for a third, parallel, 680 k Ω resistor to be mounted on the PCB card.

Measurements

Fig. 3 shows the measured voltage distribution in the pull-down stack. The DC high-voltage was set to 5.5 kV, and the nominal pulse width was 400 ns at 2.5 kHz. As expected the maximum transient voltage (915 V), immediately following turn-off of the pull-down stack, occurs across the APT1004 FET in module DN7.

The deflector plate voltage for operation at 5 kV is shown in Fig. 4, at 2.5 kHz, and a nominal pulse width of 399.75 μ s. The rise and fall time of the pulse voltage is 30 ns and is virtually independent of repetition rate or pulse-width, while operating in the frequency range 1 Hz to 20 kHz (pulse lengths from 250 ns to 1 s)[9]. Similarly the rise and fall time is virtually independent of the DC high voltage in the range 1 kV to 6 kV[9].

The current in each FET stack was determined, while operating at 5 kV with 400 ns wide pulses, by measuring the voltage drop across the 29 Ω resistors (Fig 1). A current waveform for the pull-down stack is shown in Fig. 5: the peak current of 9.5 A is well within the rating of the APT1004[7]. Integrating the measured current through the source of module DN1, with respect to time, gives a charge of 277 nC and 65 nC associated with the first and second pulses of current (Fig. 5), respectively. Similarly the

Figure 3: Voltage distribution in pull-down stack

charge associated with the corresponding current pulses through module UP7 is 148 nC and 269 nC. In both cases the first pulse of current is associated with the turn-off of the pull-up stack and the turn-on of the pull-down stack. Similarly the second current pulse is associated with the turn-off of the pull-down stack and the turn-on of the pull-up stack.

As expected the 269 nC associated with module DN1, when the pull-down stack turns-on, is very similar to the 277 nC associated with module UP7, when the pull-up stack turns-on. A charge of 129 nC (277 nC - 148 nC) is associated with charging the deflector plate assembly and connections to 5 kV. This implies a load capacitance of approximately 26 pF. This capacitance value agrees well with a measured value of 25.5 pF obtained using a vector impedance meter at 1 MHz[9].

The effective parasitic capacitance to ground can be estimated as follows: first assume that a charge of 83 nC (148 nC - 65 nC) is required to charge the parasitic capacitance to ground of each module (C_m). Also assume each module has the same value for C_m , and neglect the voltage mal-distribution down the stack. Hence the calculated value for C_m is 4.1 pF. In turn the linearized drain-source capacitance of each APT1004, during pulsing, is 91 pF.

The pulse generator has been tested at up to 20 kHz with pulsed voltages up to 6 kV. The FET stacks are capable of being operated at frequencies considerably higher than 20 kHz. However the rms current through the fast grading components and the 29 Ω current limiting resistors is proportional to frequency. At 5.5 kV and 20 kHz the 2 W fast-grading resistors associated with modules DN7 and UP7 dissipate approximately 1 W, and each of the 29 Ω current limiting resistors dissipate approximately 1.5 W. For operation at higher repetition rates more substantial grading and limiting components will be required.

Figure 4: Pulse voltage; frequency=2.5 kHz, width=399.75 μ s

Figure 5: Current in source of module DN1

The first and second stages have been operated at 60 V and ± 250 V, respectively, at 1 MHz. The second stage consists of two circuit cards which are identical to the cards in the high voltage stacks, thus confirming that the basic design is inherently capable of operation at 1 MHz.

PSpice Calculations

A PSpice[10] model was developed for the APT1004 FET based on the manufacturers specifications[7, 9]. A model for the Amidon FT240-43 ferrite, including losses was also developed[9, 8]. The full circuit shown in Fig. 1, together with parasitics, was analyzed over several cycles of operation. Fig. 6 shows the predicted gate-source voltage for the APT1004 FETs in the pull-down stack. The predicted dissipation for 1 MHz operation for an APT1004 is approximately 140 W, and occurs in module UP7: the dissipation in the APT1004 FET in module UP1 is only 50 W. Future calorimetric measurements are planned to determine the actual power dissipation in each of the APT1004 FETs.

PSpice has also been used to predict the dissipation in the pulse transformers, the zener diodes and the IRFD110 FETs. The predicted losses in each of the FT240-43 cores at 1 MHz is approximately 6 W. The ferrite losses have the effect of reducing the gate drive for a given drive on the primary of the pulse-transformer. A lower loss ferrite, such as CMD5005[11], would be preferable for high frequency applications: CMD5005 would dissipate less than 2 W per ferrite core at 1 MHz. The predicted power dissipation in each zener diode and each IRFD110 FET, at 1 MHz, is approximately 0.8 W and 0.6 W, respectively: the corresponding data-sheet values are 0.4 W and 1 W. Hence the zener diode assembly would need to be modified for reliable operation at 1 MHz.

The PSpice predictions confirmed that fast-grading capacitor values based on Eqn. 8, which linearizes the drain-source capacitance, result in greatly improved voltage grading in the stack.

Future Development

Future development of the design of the FET pulse generator is being considered as part of an accelerator upgrade[4], which requires a pulsed beam from the cyclotron with a period of 1 μ s or more. This could be accomplished with one set of 1 m long deflector plates mounted in the cyclotron at the extraction radius and pulsed at a continuous repetition rate of 1 MHz with 30 kV pulses. Alternately one could envision two sets of 1 m long deflector plates energized with 15 kV pulses. The 15 kV stacked FET option seems to be a realistic goal. This mainly involves increasing the rating of resistors and capacitors and using lower loss ferrites for the pulse transformers. However plans call for further reducing the parasitic capacitance from each module to ground, which in turn will allow the values of the fast-grading capacitors to be reduced. This will reduce the stresses on the fast-grading circuits.

Figure 6: Predicted gate-source voltages for APT1004 FETs in pull-down stack

Conclusion

An economical, frequency and duty factor agile, pulse generator has been designed, built and tested at TRIUMF. The prototype pulse generator has been tested at a pulse voltage of 6 kV, and over a frequency range of less than 1 Hz up to 20 kHz. Pulse widths from 250 ns to 1 s have also been demonstrated. Rise and fall times of 30 ns have been achieved. Measurements on the basic 1 kV FET modules operating at 1 MHz, as well as PSpice calculations on the power dissipation in each FET, confirm that a 1 MHz, high voltage version is feasible.

Acknowledgements

The authors acknowledge D. Bishop and M. Good whose attention to detail was invaluable during the prototyping and testing.

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