Introduction

- The commercial off-the-shelf components (COTS), especially FPGAs, have been considered for experiments in harsh environments with radiation background:
  - Space experiments (e.g. ISS);
  - Accelerator experiments (e.g. LHC at CERN);
- The FPGAs are viable replacement solutions for Application Specific Integrated Circuits (ASICs) due to their:
  - low cost;
  - high logic density;
  - low non-recurring engineering costs (NRE);
- Though using FPGAs in such applications has several advantages, these devices are sensitive to radiation induced effects:
  - Single Event Effects (SEEs);
  - Cumulative effects (Total Ionizing Dose—TID and Displacement Damage—DD);

<table>
<thead>
<tr>
<th>TID [krad]</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MeV n_{eq} [cm^{-2}]</td>
<td>3 · 10^{12}</td>
</tr>
<tr>
<td>Hadrons &gt; 20 MeV [cm^{-2}]</td>
<td>1.2 · 10^{12}</td>
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Test Beam Results

- The smallest device from Xilinx’s KINTEX-7 family has been tested, XC7K70T-FBG484C:
  - manufactured on 28 nm HKMG technology node based on TMSC high performance and low power process (HPL);
  - 82 k user Flip-Flops, 4.86 Mb of Block RAM (BRAM), 300 I/Os, 18.8 Mb of configuration memory (CRAM);
- Different particle beams were used to measure the device radiation tolerance:
  - 35 MeV and 200 MeV protons; (Julich F2 and PSI);
  - Ions with a broad range of Linear Energy Transfer (LET): from 1.3 to 32.4 MeV · cm^{-2}/mg; (Louvain CRC and Legnaro LNL);
  - 8-50 keV X-ray photons; (Padova University);
  - Mixed field of particles from 24 GeV protons on a Copper target at CHARM CERN.
- Several resources were tested: CRAM, BRAM, user flip-flops (with TMR) and the IO Blocks (Ring Oscillators);
- A custom DAQ system has been designed to monitor the device operation and its electrical parameters;

Proton and X-Ray results

- 35 MeV protons (200 Krad/DUT, 3 DUTs): (5 % fluence error)
- SEU cross-sections: 4.9 · 10^{-15} cm^{2}/bit for CRAM and 6.9 · 10^{-15} cm^{2}/bit for BRAM;
- IO blocks SEU cross-section: 2.22 · 10^{-12} cm^{2}/device.
- 200 MeV protons (500 Krad/DUT, 3 DUTs):
  - CRAM SEU cross-section: 3.6 · 10^{-15} cm^{2}/bit; (10-15 % fluence error)
- 50 keV X-Rays: no effects were seen in any of the FPGA resources.

Ion SEE results

- Thresholds: SEL at around 15 MeV · cm^{-2}/mg LET and CRAM SEL: below 1.3 MeV · cm^{-2}/mg LET;
- SEFI events seen at a LET of 32 MeV · cm^{-2}/mg;
- CRAM SEU cross-sections: 0.47 · 10^{-14} cm^{2}/bit at 1.3 MeV · cm^{-2}/mg LET and 0.26 · 10^{-14} cm^{2}/bit at 32 MeV · cm^{-2}/mg LET;
- IO blocks SEU cross-section at LET of 8.59 MeV · cm^{-2}/mg: 0.6 · 10^{-12} cm^{2}/device;
- High current states were observed in the core power rail, recovered with full reconfiguration;
- Micro-latchups, 100 mA current jumps, were seen in the VCCAUX power rail were seen, recovered only with power cycle.

CHARM results

- 4 DUTs were exposed in the same time up to a TID of 34.27 Krad (Si), with a 35 % measurement error;
- LHCb-RICH firmware was used with the SEM IP CORE embedded as an error mitigation technique for CRAM (2 DUTs);
- SEU cross-sections: 10^{-17} cm^{2}/DUT for CRAM and 0.31 · 10^{-10} cm^{2}/DUT for user logic; (40 % fluence error);
- Very low number of CRAM critical bits: ~ 6000 bits out of 18884576 bits (CRAM size).

Operation in the LHCb Environment

- Assuming 7000 hours of operation in the Phase I of the LHCb Upgrade, 50 fb^{-1} total luminosity, we expect:
  - 20 to 40 SEUs in critical configuration memory locations per hour in all FPGAs; (3000 FPGAs)
  - Total SEU rate is expected to be 30 K SEUs/hour/LHCb-RICH;
  - ~ 30 SEUs per hour in the I/O blocks of all FPGAs due to CRAM corruption (512 K input pins and 84 K output pins);
- Most of SEUs will not affect the user logic, but a very small fraction can induce high current events which can disturb the FPGA operation or affect the information flow;
- The mitigation will be done online with partial/full reconfiguration or offline by masking the corrupted FPGAs.

Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments
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Romanian LHCb Group

LHCb detector

LHCb Upgrade Phase I

During the second LHC long shutdown, started in 2019, the LHCb detector will be upgraded to operate at a higher luminosity,

- SRAM-based FPGAs (KINTEX-7) will be used in the digital readout boards of the LHCb RICH sub-detectors;
- Microsemi’s antifuse FPGAs are the backup solution;
- An irradiation testing campaign has been implemented to establish the radiation tolerance of both devices.

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