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Single Event Upsets in the ATLAS IBL Frontend ASICs at the Large Hadron Collider at CERN

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ABSTRACT: ATLAS is one of the four major experiments at the Large Hadron Collider at CERN. The tracking performance of the ATLAS detector relies critically on its 4-layer Pixel detector, located at the core the ATLAS tracker. During operation at instantaneous luminosities of up to $2.1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ the frontend chips of the ATLAS innermost pixel layer experienced single event upsets affecting their global registers as well as the settings for the individual pixels, causing, amongst other things, loss of occupancy, noisy pixels, and silent pixels. A quantitative analysis of the single event upsets as well as the operational issues and mitigation techniques are presented.

KEYWORDS: Pixelated detectors and associated VLSI electronics, Particle tracking detectors (Solid-state detectors), Radiation damage to electronic components

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1 Introduction

The Large Hadron Collider (LHC) delivered in 2015-2018 the total of 156 fb^{-1} integrated luminosity to the ATLAS detector [1] with 13 TeV pp collisions. Up to 0.77 fb^{-1} luminosity was delivered per LHC fill with the maximum of $2.1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ peak stable beam luminosity. The ATLAS pixel detector [2] operated in a extremely high-radiation environment, in particular the innermost Insertable B-Layer (IBL) [3] located at $R = 3.3 \text{ cm}$. In these conditions the IBL was exposed to $92.5 \times 10^{11} \text{ hadrons cm}^{-2}/\text{fb}^{-1}$ with $E > 20 \text{ MeV}$ according to PYTHIA [4]/FLUKA [5] simulations. The energy deposited by the interactions of these hadrons results in the Single Event Upsets (SEU) of the memory states in front-end pixel chips.

2 The design and tests of the SEU tolerant memory

The IBL pixel front end chip FE-I4B [6] in 130 nm technology was designed with SEU-hard configuration memories. Inside the pixels, Dual Interlocked Cell (DICE) [7] latches were used. DICE latches have redundant storage nodes and restore the cell original state when an SEU error is induced in a single node. The SEU immunity is lost only if two sensitive nodes change their states by single particle impact. The tolerance to SEU is increased by using an Hardened By Design (HBD) approach: spatial separation of critical nodes, isolated wells, guard rings and interleaving of cells. The Global Registers (GR) memories, located in the End of Column Area (ECA) outside of the pixel matrix region, are further protected by triple DICE latches with the addition of a simple majority logic. Such triplication is not possible inside the pixel due to the space constraints. The SEU tolerance of FE-I4B chips was tested in the 24 GeV proton beam [8] at CERN PS with typical intensity of $0.5\text{-}1.5 \times 10^{11} \text{ protons cm}^{-2}/\text{spill}$. The measured SEU cross-section for the single DICE latch (Enable bit, $0 \rightarrow 1$ transition in the pixel cell) is $1.1 \times 10^{-15} \text{ cm}^{-2}$ [9].

Figure 1. Fraction of number of pixels, initially disabled at the beginning of the LHC Fill 6356, that start to fire after certain luminosity has been recorded. Shown for four different FE-I4B front ends placed on various IBL 3D modules as a function of the integrated luminosity of the LHC fill [10].

3 Measurements of the SEU during ATLAS operations

3.1 Local pixel configuration memory measurements

The pixel local configuration consists of 13 bits in each pixel: Enable, TDAC (thresholds 5 bits), Injection Caps choice (2 bits), HitBus, FDAC (feedback current 4 bits). Typical symptoms of the SEU in the pixel local configuration are silent pixels, broken clusters and noisy pixels. SEU flip $1 \rightarrow 0$ of the “Enable” pixel bit results in having a “Quiet” pixel. During the 2016 LHC run (no auto-reconfiguration used) we observed a linear rise of the number of “Quiet” pixels throughout periods when beam was on. After the auto-reconfiguration actions were introduced during the 2017 run, we observed a rate of “Quiet” pixels decreased significantly in the middle of the fill following these actions. We dispose of several methods for measuring SEU during the LHC fill. The first method consists in setting at the start of the fill the “Enable” bit of all pixels to zero, i.e. disabling all the pixels of a given chip and measuring the number of active pixels during the fill. Figure 1 shows the fraction of pixels, initially disabled at the beginning of the LHC fill, that change their states and are enabled when traversed by a recoil with big charge deposition [10].

The second method consists in reading back the content of the pixel local configuration memory and comparing the values to the initial settings. In Fig. 2 (a) the rates of bit flips are shown for different FE-I4B chips with default Shift Register value of one. In this case $0 \rightarrow 1$ flips in pixel memory are much more frequent than $1 \rightarrow 0$ flips. These asymmetries were predicted by DICE latch simulations [11]. DICE latch Single Event Effects (SEEs) are dominated by Single Event Transient effects (SET or glitches), which create fake LOAD signals. $0 \rightarrow 1$ flips in pixel memory

Figure 2. In figure (a), the Shift Register (SR) was set to 1, and $0 \rightarrow 1$ flips dominate due to the SET on the LOAD line, while low rate $1 \rightarrow 0$ flips are due to real memory SEU. In figure (b), the Shift Register was set to 0, and $1 \rightarrow 0$ flips dominate. The values of the Shift Register are refreshed several times during the fill [10].

are dominant when the SR is loaded with 1, and $1 \rightarrow 0$ flips are dominant when SR is loaded with 0 as shown in Fig. 2 (b). The extrapolation of the measurement of the SEU rate with 24 GeV protons at CERN PS is shown with a blue line in Fig. 2 (b). During the CERN PS measurement, the value of the SR was not refreshed, which may explain the higher rate of bit flips due to SET contributions. Figure 2 (a) and (b) present different chips at slightly different locations, so part of the difference may come from chip-to-chip process variations, tuning, and particle flow differences.

Simulations of SET effects in DICE memories [11] demonstrate that most of the SET on the LOAD line are produced by heavy ionizing particles simultaneously crossing the pair of LOAD signals driving transistors. Unfortunately, in the current implementation of the DICE latch in FE-I4B, two transistors driving LOAD signals are close to each other. In the same simulations, it was shown that one can considerably reduce these glitches by increasing the distance between two LOAD signal transistors.

In the same fill, the average rate of the SEU/SET bit flips in pixel memory was studied as a function of the bit number (0-12). In Fig. 3 (a), the Shift Register was set to 1, and $0 \rightarrow 1$ flips dominate due to the SET on the LOAD line, while low rate $1 \rightarrow 0$ flips are due to real memory SEU. In Fig. 3 (b), the Shift Register is set to 0, and $1 \rightarrow 0$ flips dominate. The rate of bit flips is rather uniform for most of the bits. However, the flips in bit-8 (HitBus) are twice as frequent, probably due to specific layout of that memory bit. The extrapolation of the measurement of the

Figure 3. Average rate of SEU/SET bit flips in pixel memory of FE-I4B per fb^{-1} in LHC fill 7334, as a function of bit number (0-12). In figure (a), the Shift Register was set to 1, and $0 \rightarrow 1$ flips dominate due to the glitches on the LOAD line, while low rate $1 \rightarrow 0$ flips are due to real memory SEU. In figure (b), the Shift Register was set to 0, and $1 \rightarrow 0$ flips dominate [10].

SEU rate with 24 GeV protons at CERN PS is shown with a blue line in Fig. 3 (b).

The third method for studying FE-I4B SEU is the counting of the evolution of the number of noisy pixels during the fill. If the TDAC Most Significant Bit (MSB) flips from $0 \rightarrow 1$ due to a SEU, we expect the appearance of “Noisy” pixels due to the lowering of the threshold. Low values of TDAC correspond to high thresholds. Figure 4 shows the fraction of pixel hits with high noise as a function of pixel initial TDAC during empty bunches of the typical LHC fill 6343 with integrated luminosity of 0.48 fb^{-1} [10]. Strong suppression of the noise for $\text{TDAC} > 15$ proves that the biggest fraction of the noise happens after the SEU flip $0 \rightarrow 1$ of MSB of TDAC, which sharply reduces the pixel threshold. So the appearance of the noisy pixels in IBL is explained by SEU in TDAC MSB flip $0 \rightarrow 1$. No correlation of the noise with FDAC values was observed.

3.2 Global register configuration read-back measurements

GR corruption has a potential big impact on module operation: change of the low voltage consumption, silent modules, desynchronized modules. A module becoming silent is often correlated with the change of the module consumption. In Fig. 5, the cumulative fraction of SEU/SET bit flips in the Global Configuration Memory of FE-I4B is shown as a function of integrated luminosity in LHC fill 7333. The high rate of $0 \rightarrow 1$ flips is probably due to SET on the LOAD line with register value 1. The pattern 0xFFFF was loaded last into the register. The values of the register

Figure 4. Fraction of pixel hits with high noise as a function of pixel's initial TDAC value during empty bunches of the typical LHC Fill 6343. Strong suppression of the noise for TDAC > 15 proves that the biggest fraction of the noise happens after an SEU flip 0→1 of MSB of TDAC, which sharply reduces the pixel threshold. In this fill the pixels with more than 200 hits are defined as noisy [10].

Figure 5. Cumulative fraction of SEU/SET bit flips in the Global Configuration Memory (GCM) of FE-I4B as a function of integrated luminosity in LHC fill 7333 [10].

are refreshed several times during the fill. No $1 \rightarrow 0$ transitions were observed during the fill. This is due to the triply redundant memory design, which suppresses very efficiently real SEU.

3.3 Recovery of bits flipped by SEE

Refreshing of the GR during Event Counters Reset (ECR, ATLAS wide common signal to reset the event counters periodically every 5 seconds) was introduced during the 2017 run. This refreshing restores proper functioning of the module and strongly reduces the rate of the module errors. Unfortunately, there is not enough time in the ECR time window to reconfigure all local pixel

Figure 6. The noise occupancy in IBL 3D modules as a function of integrated luminosity with and without the mechanism of pixel register reconfiguration at ECR [12].

memory. The solution was to refresh three bits of one pixel double column at each ECR. In this way, any local pixel memory bit was refreshed every ~ 11 minutes. This method was tested during a few LHC fills in 2018. Figure 6 shows the noise occupancy (the number of hits per pixel per event) in IBL 3D modules as a function of integrated luminosity with and without the mechanism of pixel register reconfiguration at ECR timing. Figure 6 is made from the calibration PixelNoise stream, where data are taken with isolated and unpaired bunches. The data points include vertical bars showing statistical errors, but they are hardly visible. Without the mechanism of pixel register reconfiguration, SEUs cause an increase in the noise occupancy during the run. When the reconfiguration mechanism is adopted, the noise decreases as a function of integrated luminosity. The reason for these effects is that the reconfiguration is performed every 11 minutes for the same pixel registers, but the time required to accumulate the same amount of integrated luminosity becomes longer during the run due to the decrease of instantaneous luminosity.

4 Conclusion

The ATLAS Pixel detector with the IBL at $R = 3.3$ cm is operated efficiently at high luminosity with the expected level of SEUs. SEUs in the global and local pixel configuration memories were observed during LHC fills and have several consequences: steps in low voltage consumptions, module desynchronization, dead modules, quiet pixels, broken clusters, noisy pixels etc. The level of SEUs observed during LHC fills is consistent with the previous tests in 24 GeV proton beam. By read-back measurements and simulations it was shown that glitches on the LOAD line of the DICE latch dominate the memory flips and create the apparent asymmetries in $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions. Global configuration SEUs were mitigated in 2017 by refreshing the global memory during ECR every 5 seconds without any additional dead time. It was demonstrated in test runs in 2018 that gradual refreshing of local pixel memory during ECR dramatically reduces the number of noisy and quiet pixels and broken clusters.

We plan to introduce the gradual refreshing of local pixel configurations during ECR in 2021 in LHC Run 3 in order to reduce the number of noisy and quiet pixels and improve the performance for future increase of the LHC luminosity.

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