HGCROC radiation hardness testing

Student: Oleksii Kurdysh
Supervisors: Bora Akgun, Pieter Everaerts

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1 Introduction

Europe’s top priority should be the exploitation of the full potential of the LHC, including the high-luminosity upgrade of the machine and detectors with a view to collecting ten times more data than in the initial design, by around 2030 [1]. The High Luminosity LHC (HL-LHC) operational phase is scheduled to commence in the last quarter of 2026. The luminosity will increase by a factor of ten. The instantaneous luminosity will be more or less constant (levelled) at $5 \cdot 10^{34} \, \text{cm}^{-2} \text{s}^{-1}$. The corresponding number of collisions (pileup) per bunch crossing will be 140-200 [2]. So pileup will increase by a factor of ten compared to CMS Run 1 (Fig.1).

![Figure 1: Visualisation of pileup events for Run 1 and HL-LHC.](image)

The existing CMS endcap calorimeter cannot cope with expected radiation and any replacement for it must have the ability to withstand integrated radiation levels that are ten times higher than anticipated in the original CMS design. Simulations using FLUKA (Fig.2) indicates that the highest fluence is around $10^{16} \, \text{neq/cm}^2$ and the highest dose is around 2 MGy. Of course, the electronics must work in such conditions throughout the lifetime of the detector. This was the scope of my project.

![Figure 2: FLUKA results of the expected HL-LHC radiation levels.](image)

2 HGCROC

The current endcap calorimeter will be replaced by the High Granularity Calorimeter (HGCAL) for the HL-LHC. The proposed design uses silicon sensors as active material in the high radiation regions. The pads of the silicon sensors are connected to the input of the front-end ASIC (Application-Specific Integrated Circuit), High Granularity Calorimeter Read Out Chip (HGCROC), shown in Fig.3, which measures the accumulated charge and the time of arrival at 40 MHz frequency.

This ASIC is regarded to have following properties:
3 HGCROC radiation tests

To test ASIC radiation tolerance, several Total Irradiation Dose (TID) tests were performed/planned:

1. One test in December 2018 and one in July 2019 with the first prototype version of the ASIC (HGCROCv1) (my second week at CERN)

2. Another test in October 2019 with the second prototype version of the ASIC (HGCROCv2)

So my task was to help and analyze results from the test in July and based on these results, prepare for and participate in the test in October.

4 July 2019 radiation test

4.1 Test setup

The HGCROCv1 ASIC was irradiated with an X-ray source. The distance from the X-ray source to ASIC was chosen to get uniform dose across the ASIC area (15 x 7 mm). The ASIC was mounted on a board that was designed for characterization and irradiation testing. The power is supplied directly to the board using 3 separate channels for the digital(1.2V), analog(1.5V) and board(3.3V)
power. We can also measure voltages and currents on the specific power domains of the ASIC using a multimeter. We used a Keithley scanner card for this, which allowed us to flip between measurements. The board was connected to a commercial Xilinx KCU105 FPGA board via FMC connector, which was used to control the ASIC and get the data out (Fig. 4).

Figure 4: The July 2019 test setup. Glass over the ASIC was removed during irradiation.

The ASIC and the board were placed directly under the X-ray source inside X-ray box, shown in Fig. 5. The KCU105 FPGA board was inside X-ray box, but placed aside and shielded. Three power supplies, external clock and oscilloscope were placed outside of the X-ray box.

Figure 5: The X-ray box.

4.2 Irradiation profile

The irradiation profile is shown in Fig. 6. We started quite fast but slowed down since we expected failure. During the previous test (January 2019), PLL (phase locked loop) failed at 35 Mrad. Once PLL failed, we went to high dose rates to reach maximum dose.
4.3 Test results

1. The analog circuit works after the full irradiation (as checked by taking pedestal measurements).

2. The PLL supposed to lock at 160Mhz and to do that it has to be able to at least reach this frequency. ASIC can’t work without clock. One of the goals of July 2019 test was to repeat PLL failure at 35Mrad, study the failure mechanism and test radiation effects on other parts of the ASIC. The PLL Oscillator output frequency versus TID is shown in Fig.7.

The PLL Oscillator output frequency versus TID is shown in Fig.7. The PLL required to lock at 160 MHz.

The PLL failed two times. First time – temporary – at 33 Mrad. Frequency drops to 147 Mhz, as shown in Fig.7. We immediately saw that the PLL starts degrading during irradiation and then did not reach 160
MHz after 33 MRad. At that moment, we also realized that the voltage at the input of the PLL was actually below its specifications due to power loss on the test board. So we increased the input voltage slightly and this allowed the PLL to lock again. Frequency is then 165 Mhz, as shown in Fig.7. After this degradation continued and at 38 Mrad PLL was fully lost as frequency dropped below 150 Mhz, as also shown in Fig.7. Since we wanted to test other ASIC functionalities, after 38 Mrad we bypassed the PLL and used an external clock instead.

5 HGCROCv2

Second version of the ASIC became available in the summer, first tests performed with it. New functionalities added, this version is closer to final. Things changed in HGCROCv2 ASIC [4]:

- The PLL has its own power domain.
- Two halves have different Analog-to-Digital Converter (ADC). In fact ASIC is two ASICs “glued” together. One of the parts have experimental ADC architecture, other half has a "standard" ADC.
- The state of the different components of the ASIC like preamplifier, Time-over-Threshold(TOT) discriminator etc, can be monitored.
- Digital part was fully redesigned.

6 Preparation for October X-ray irradiation tests

6.1 Pyrame

It would be great to have a common framework to control the hardware like the power supply, multimeter(+scannercard) and ASIC DAQ. Pyrame [3] was investigated as possible a software framework for the ROC testing. The Pyrame software modules to control the AimTTI TSX1820P power supply, Keithley 2000 multimeter and scannercard, shown in Fig.8, were created. The power supply and multimeter+scannercard were used during the July radiation test, controlled by python scripts. The goal was to make this process more automated. In the end we discovered that DAQ would take considerable effort to integrate into Pyrame, we discarded the possibility of using this framework.

Figure 8: Hardware for which Pyrame software modules were created.
6.2 Stability

During the July test we saw weird jumps in voltage measurements, as shown in Fig.9 of magnitude 0.01V. We wanted to check if they were caused by measurement itself?

![Figure 9: Unexpected voltage jumps.](image)

The measurement was performed by a Keithley 2000 scannercard. To test this simple voltage divider was assembled, as shown in Fig.10(a), voltage measured on it during long periods of time, without irradiation. All 10 channels were used and all of them showed similar behavior, as shown in Fig.10(b). The code was written in a way to avoid measuring before previous measurement was done (possible source of the problem). Software used is python wrapper for SCPI commands, communication with instrument done via Prologix GPIB-Ethernet adapter. It can be seen that maximum measurement jump was 0.0002 V, orders of magnitude lower than what we saw during irradiation. During next radiation test, if we see jumps, we will know that this not because of the measurement itself.

![Figure 10: The divider for stability measurement and result of the measurement.](image)

6.3 HGCROCv2 characterization

Before using the new hardware that will be used to irradiate we want to understand how it works without radiation.
6.3.1 Test setup

To do this we used the setup shown in Fig.11.

![Figure 11: The HGCROCV2 characterization setup.](image)

This time ASIC is not placed directly on the ASIC board, it is installed on a mezzanine card which is placed on the carrier board. In this way one ASIC board can be used with multiple ASICs (but one at the time). ASIC/ASIC board now requires only one 3.3V power supply (normal power consumption is 2.57W (depends on the firmware and the ASIC)). ASIC board now have two Kiethley connectors (instead of 1) to probe some of the signals. The ASIC board again is connected a to commercial Xilinx KCU105 FPGA board, used to control the ASIC and get data out.

6.3.2 The Probe_DC measurement

In HGCROCV2 it is possible to see the state of different components of the ASIC. Reference voltages provided in ASIC documentation to do this. Monitoring done by setting two Probe_DC registers to values that correspond to certain parts of the ASIC (for both halves of the ASIC). Then certain value is readout on Probe_DC pin on ASIC carrier board, it can be compared with the references provided in the documentation. The results are shown in Fig.12.
6.3.3 The pedestal measurements

The pedestals are the values you readout without any signal supplied. It’s like a background. It is one of the indicators of the ASIC’s performance and one of the measurements done during irradiation test. We want to know pedestals before irradiation, shown in Fig.13, during, and after irradiation.

It is clearly visible that pedestals are different for two halves. The pedestals are readout through ADC, and ADCs are different in different halves.

For convenience we want to equalize pedestals. To do this HGCROCV2 ASIC have two options: global and local pedestal adjustment. Global means that there is 10b register we can set to a certain value, and we expect pedestal values change by the same amount for all channels. Local means there is 5bit register we can set to a certain value, we can select a channel and expect that only this channel will change. The results of local 5bit tuning are shown in Fig.14.

Each line corresponds to a certain channel. X-axis – the value we set to local tuning register, y-axis – pedestal value in ADC counts. Here we can see again that two halves behave differently: initial point and rate at which ADC counts change depends on the tuning value, final point is different, as shown in
Figure 13: The pedestal values for different channels before irradiation in units of 10bit ADC (max value 1023).

Figure 14: The results of channel-wise pedestal 5bit adjustment.

Notice the jumps to zero that happen at 5bit tune value ‘15’. This issue is investigated by the ASIC designers. Also notice that amount of channels that drops to 0 is different for two halves.

Results of global pedestal tuning shown in Fig.15. Same characteristics as for channel-wise tuning. Initial pedestal value is different because default 10b register values is not zero. Fig.16 shows how pedestals change with global pedestal adjustment. Each line corresponds to a different 10b tuning value. It is visible that all channels step same between different 10b values.

Also notice the behavior of special channels, shown in Fig.14 (right plot). During the test we noticed that common mode and calibration channels are not changed by pedestal tuning, it turned out that software had to be adjusted to also allow to tune these channels. This has been fixed by now but the problem was discovered thanks to these cross-checks.
6.3.4 The DAC linearity

The ASIC has internal charge injection functionality (CalibDac). The results of the injection can be monitored by internal ADC or analog pin on ASIC board. We wanted to see how linear calibdac is, in analog way. To connect internal calibdac to external pin on board, we need to close two switches by setting IntCtest and ExtCest bits to 1, as shown in Fig.17. We measured output on the carrier board with Keithley 2000 scannercard. The results of the linear fit for two halves are:

\[
K_{i n\_ C t e s t\_ R} = 0.00036422 \cdot calibDac + 0.04901994 \\
K_{i n\_ C t e s t\_ L} = 0.00036149 \cdot calibDac + 0.04737581
\]

Figure 18 shows the residues from linear fit, where we can see that left part of the ASIC has a jump from linearity at 1024 (11b calibdac max value is 2047), which ASIC designers investigate. We can also see that there are smaller jumps at \(2^n\) values, which is usual for things controlled in binary. We can also see that two halves behave differently before 1024 jump, but similar after 1024 (with some offset).

7 Conclusion

During my internship here I contributed to HGCROCv1 radiation test. Wrote software and assembled hardware module to control/read out power supplies and multimeter(+scannercard), investigated stability problem appeared during the July radiation test using it. I also participated in characterization of HGCROCv2 before upcoming radiation (hardware assembly and software to probe the state of different components of the ASIC, such as internal charge injection linearity check, pedestal tuning).
Figure 16: Change of pedestal values with respect to pedestal value with 10 bit tuning value=0.

Figure 17: The CalibDac switch.

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References


Figure 18: The CalibDac linear fit residue for two halves.

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[4] HGCROC2/2A Datasheet