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Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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ABSTRACT: Following new TDAQ buffering and rate requirements and high expected radiation doses in the pileup conditions of the high-luminosity LHC, the ATLAS Liquid Argon Calorimeter electronics will be upgraded to readout the 182,500 calorimeter cells at 40 MHz with 16 bit dynamic range.

The triangular calorimeter signals are amplified and shaped by the analogue electronics over a dynamic range of 16 bits, with low noise and excellent linearity. Developments of low-power preamplifiers and shapers to meet these requirements are ongoing in CMOS 130 nm. In order to digitize the analogue signals on two gains after shaping, radiation-hard, low-power 40 MHz 14-bit ADCs are developed using a SAR architecture in 65 nm CMOS. Characterization of the first prototypes of the frontend components show good promise to fulfill all the requirements. The signals will be sent at 40 MHz to the off-detector electronics, that will make use of FPGAs connected through high-speed links to perform energy and time reconstruction through the application of corrections and digital filtering. Reduced data are sent with low latency to the first level trigger, while the full data are buffered until the reception of trigger accept signals. The data-processing, control and timing functions will be realized by dedicated boards connected through ATCA crates. Results of tests of the first prototypes of front-end components will be presented, along with design studies on the performance of the off-detector readout system.

KEYWORDS: Calorimeters, Front-end electronics for detector readout, Modular electronics

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Contents

1	Introduction	1
2	On-detector electronics	1
2.1	Front-end boards	2
2.1.1	Analog readout	2
2.1.2	Digitisation	2
2.1.3	Integration	2
2.2	Calibration board	3
3	Off-detector electronics	3
3.1	LASP	3
3.2	LATS	4
4	Conclusions	4

1 Introduction

The High Luminosity upgrade of the Large Hadron Collider (HL-LHC) is expected to be completed in 2026. It will allow the machine to reach ultimate instantaneous luminosity of $7.5 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$, corresponding approximately to 200 inelastic proton-proton collisions per bunch crossing. The total integrated luminosity over the period of HL-LHC data-taking is expected to be up to 4ab^{-1} .

To cope with these challenging requirements ATLAS trigger and data acquisition (TDAQ) system will need to be upgraded [1] to a baseline architecture with as single-level (Level 0) hardware trigger of maximum rate of 1 MHz and $10 \mu\text{s}$ latency (currently it has maximum rate of 100 kHz and $2.5 \mu\text{s}$ latency). As a backup, each system and sub-system are required to be capable to evolve to a dual-level hardware architecture with a Level-0 (Level-1) trigger rate up to 2-4 MHz (600–800 kHz) and $10 \mu\text{s}$ ($35 \mu\text{s}$) latency. The result of the hardware trigger decision are distributed to all detectors, which then transmit their data to the DAQ system.

The upgrade of the current Liquid Argon (LAr) readout electronics architecture [2] to a new free-running scheme [3] in which all calorimeter data are sent off-detector is necessary to meet these requirements. In both TDAQ configurations, the Level-0 trigger will receive information at low latency with coarse granularity, which corresponds to the Phase-I SuperCell readout [4].

2 On-detector electronics

The upgraded on-detector electronics will comprise 1524 new Front-end Boards (FEB2: 128 channels each) and 130 new Calibration Boards.

2.1 Front-end boards

FEB2 boards will provide input line termination, amplification, shaping, digitisation of the signals prior to transmitting them to the off-detector electronics. They are required to have radiation-tolerance to 180 kRad. They contain three key ASICs: PreAmplifier/shaper (PA/S), Analog to Digital Converter (ADC) and serialiser. Digitisation on the FEB2s by a 2-gain readout and 14-bit ADC for 16-17 bit dynamic range is targeted in order to keep electroweak physics signals in the same gain range.

2.1.1 Analog readout

Preamplification and shaping are implemented on a single ASIC. Two prototype designs have been developed and tested in parallel. The latest version for both is implemented in 130 nm CMOS, one in a four-channel configuration with line termination to cover both $25\ \Omega/10\ \text{mA}$ and $50\ \Omega/2\ \text{mA}$ detector impedances and the other in a two-channel configuration with only $25\ \Omega/10\ \text{mA}$ line termination. Both prototypes show good integral non-linearity (INL) below 0.2% for the full dynamic range and equivalent noise current (ENI) within the requirements. The four-channel prototype has also successfully passed total ionising dose (TID) tests up to 5 MRad. Next version prototypes for both designs with full functionality were submitted for production at the end of 2019.

There is also a dedicated ASIC for the hadronic endcap calorimeter (HEC), in which the PA/S ASIC needs to be replaced with a Preshaper because the HEC incorporates GaAs ASICs on detector in cryostats that include inverting amplifiers plus first stage of summing. A first prototype was submitted for fabrication in September 2019.

2.1.2 Digitisation

For HL-LHC each cell needs to be digitised at the bunch crossing rate (40 MHz). Each ADC ASIC will digitize data for both gains of four calorimeter channels with 14-bit dynamic range and greater than 11.2 bit precision, resulting in output digital data streams of 640 Mbps.

The baseline approach is a 65 nm CMOS full-custom development (COLUTA). The third pre-prototype with full density (8 ADC channels) and full functionality (including on-chip bandgap and voltage references, clock distribution, etc.) is in fabrication. Two configurations are being implemented: 4 channels with a Dynamic Range Enhancer (DRE) block with internal $1 \times /4 \times$ gain and 4 channels with a more conventional single-stage MDAC. It is followed by a 12-bit successive approximation register (SAR) ADC, and an additional DRE block to resolve the upper 2 bits and reach the 14-bit specification. The simulated performance of effective number of bits (ENOB) is greater than 11.3 for DRE and 12.2 for MDAC.

Given the challenging specification requirements, there are two alternative options for ADC ASIC: one is an ‘IP Block’ approach, using 12-bit 160 Mega-samples per second (MSPS) analog block in 65 nm CMOS developed for the CMS experiment [5], followed by digital processing to achieve 14-bit at 40 MSPS and the other is COTS ADC (which has much higher cost). The final decision on which option to retain is expected in 2020.

2.1.3 Integration

Integration of these ASICs into a first test-board is also ongoing. It contains a 4 channel-preprototype of PA/S, COLUTA ADC and first prototype of lpGBT. The full readout chain is tested and working.

Early performance results are encouraging with energy resolution below 0.04% (requirement is 0.25%) and time resolution on the order of 17 ps. Other studies of the noise, cross-talk, etc. have also been performed and are all in agreement with requirements.

2.2 Calibration board

Calibration boards are used to inject precise calibration signals directly in the LAr calorimeter cells. The pulse dynamic range needs to extend up to 7.5 V, for which standard CMOS technologies can not be used, and an alternative HV-CMOS is required. Other requirements are consistent with those of the current boards with integral non-linearity below 0.1%, uniformity between channels below 0.25% and calibration pulse rise time faster than 1 ns. Radiation tolerance to 180 kRad is also required. Two main components are a high-frequency (HF) switch and a 16-bit DAC.

A test switch chip in HV-CMOS technology (XFAB 180 nm) was produced in 2018. The test results show good INL of about 0.2% for high injected charge (current greater than 1 mA) and that the maximum of the peak is stable with time. Irradiation tests, up to 5 MRad, have also been performed and no visible degradation is observed.

A second pre-prototype of the calibration board ASIC (CLAROC) implementing both HF switch and DAC was produced in the end of 2019. It contains a 4-channel switch with currents of up to 320 mA per single channel and one DAC for four channels, which provides 40 mA (13 bit) current with additional 320 mA (3 bits) provided by $8\times$ gain current mirror. This ASIC is being integrated on a CLAROC test-board with test on functionality of the ASIC, radiation tolerance, etc. to be performed in 2020.

3 Off-detector electronics

The off-detector electronics system consists of two main components a LAr Signal Processor (LASP) and a LAr Timing System (LATS).

3.1 LASP

The general functionalities of the LASP system are to receive digitised waveforms, perform gain selection, apply digital filtering to compute energy and signal time in each of the LAr detector cells, buffer data until a trigger decision is received and transmit relevant data to TDAQ system. The baseline hardware implementation of the LASP system is based on a single monolithic main blade in a full-size Advanced Telecommunications Computing Architecture (ATCA) format with one or two processing units (FPGA) and a rear transition module (RTM) with one controller processing unit. In the baseline configuration there will be 190 boards of each type.

The main blade aims to use two INTEL Stratix 10 FPGAs. Two possible versions, System-on-Chip (SX) or large and fast memory (MX), are under evaluation in a test-board. Each FPGA will receive data from two front-end-boards (FEB2) by means of 88 optical transceivers operating at 10.24 Gbps. The test board schematics is completed and routing started. The main challenges are ATCA power consumption and cooling for which studies are ongoing. Detailed simulations of the power distribution were performed with Sigrity and thermal effects on the board with Ansys Icepack to ensure that its power consumption and cooling remain within the ATCA shelf capabilities.

An RTM board will carry control and input/output processing units (XILINX Zynq+) and a set of output optical transceivers to send data to TDAQ and hardware trigger systems:

- at most 4 to send data to TDAQ through FELIX at 10.24 Gbps;
- at most 4 to send data to Global Event Trigger Processors at about 25 Gbps;
- at most 19 to send full granularity forward calorimeter data to hardware trigger system at about 25 Gbps;
- at most 30 to send data to Phase-I hardware trigger system modules at 10.24 Gbps.

Board schematics is completed and routing started.

Phase I experience shows that firmware complexity is often underestimated, so already now there is a lot of development effort on the LASP firmware. The basic framework has been set up based on that for Phase-I (with improvements). Coding guidelines and work flow are done and continuous integration, automated simulation, unit tests and compilation are implemented. Work is currently ongoing on interface definitions between modules, again profiting from Phase-I experience. Several technical projects started, such as lpGBT protocol and interface, 25 Gbps link tests with firefly transceivers, new firmware algorithms for signal processing with improved pileup reduction.

3.2 LATS

A separate set of electronic boards will be dedicated to distribution of the clock, trigger and control signals (TTC), sent from the Central Trigger Processor through the Local Trigger Interfaces, to the LAr FEB2 and calibration boards. The main challenge of this part of the system is to ensure precise timing distribution to those 1654 boards with at least two-fold redundancy at minimal cost. The basic board design is based on a matrix of primary functions (FPGA/optics). About 16 low or mid-range FPGAs such as INTEL Cyclone 10 per board are being considered, which would allow performing the task with about 20 ATCA boards, maintaining high-density/low cost design approach. This would require 192 links from on-detector boards to LATS at 10.24 Gbps and 192 links from LATS to on-detector boards at 2.56 Gbps. Tests with FPGA development kit are ongoing to study optical link protocol (lpGBT), TTC clock extraction, data synchronisation, etc.

4 Conclusions

Development of the new ATLAS LAr calorimeter readout electronics for HL-LHC is progressing well for all necessary components. More information can be found in Ref. [3].

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