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KEK Preprint 94-36
June 1994
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SCAN-9410393

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*Presented at the 1994 Symposium on Radiation Measurements and Applications,
The Univ. of Michigan, Ann Arbor, U.S.A., May 16-19, 1994
and
will be published in Nucl. Instrum. Meth., A.*

National Laboratory for High Energy Physics, 1994

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Design considerations for MOS pixel for single-sided two-dimensional detector*

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April 11, 1994

Abstract

We describe a theoretical study of a single-sided two-dimensional read-out pixel structure to be used as a high resolution tracking detector. This pixel, located on the ohmic side of a depleted p-i-n diode, consists of a n-well and a double drain pMOS transistor in the n-well. The outputs from the drain nodes of the pMOS pixels are ganged together to make a strip-like structure. The pixel detector with such transistors has superior characteristics to double-sided strip detectors currently used in high energy physics experiments. It has a built-in amplification action, resulting in high signal-to-noise detection of charged particles. The electronic noise charge is about 388 electrons for 256 pixels ganged together in a line. It has an advantage of a two-dimensional read-out configuration on a single-sided device. Simpler and cheaper fabrication technology can be used to process such a structure on wafers with diameters exceeding the traditional dimension of 4 inches. The structure and electronic properties of the pixel detector are described together with descriptions of signal processing, amplification, noise and linearity in terms of fabrication parameters.

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*To be presented at 1994 Symposium on Radiation Measurements and Applications, May 16-19, 1994, held at The University of Michigan
The proceedings will appear in a special issue of Nucl. Instr. & Meth. section A

1 Introduction

The KEK B-factory experiment [1] [2] proposes to use for vertex detection a double-sided strip-type detector at the initial operation stage. Unfortunately such a structure requires a complicated double-sided process and has inferior Signal-to-Noise ratio for long strips. In order to overcome these problems we are developing, for future upgrades, a pMOS pixel-type detector which is a two-dimensional single-sided device. This has superior characteristics over the double-sided strip-type detector such as:

1. a very high signal-to-noise ratio due to a built-in amplification from the pMOS transistor and small detector capacitance.
2. an ability to gang together the outputs from the drain nodes of the pMOS pixel to make a strip-like read-out structure. Since the pixel employs double-drain pMOS transistor, a two-dimensional read-out configuration is realised.
3. since the fabrication technology is compatible with a single-sided process, the ability to use wafers larger than the 4 inch wafers currently used for double-sided detectors.

The p-i-n diode detectors with amplification capability are proposed in terms of a bipolar transistor action by S. Hata [4] or R. Horisberger [5], in terms of JFET action by S. Kavadias et al. [6] or P. Klein et al. [7], and in terms of MOS transistor action by J. Kemmer et al. [8] [9]. For the B-factory experiment we have chosen to employ a MOS type pixel using only the MOS operation concept. In the Kemmer's MOS design, electrons are attracted on to the potential minimum in the high resistivity bulk just underneath the MOS gate electrode, while in our design the potential minimum spreads over the highly doped n-well region. The discussion is separated into three parts. In section 2 we describe basic parameters of the pMOS transistor and pMOS pixel. Section 3 deals with signal processing for the pixel detector in terms of equivalent noise charge and integral non-linearity. In section 4 the fabrication of the pixel detector is described.

2 pMOS pixel detector

2.1 pMOS pixel structure

The cross sectional view of the pMOS pixel is shown in Figure 1. In $300\mu m$ thick n-type silicon substrate, a n^+ area is implanted on the top, and a p^+ area is implanted on the back side. A p-i-n diode structure is then fabricated. On the ohmic side, the pixel is composed of a n^+ -doped area which also acts as a n-well where the double-drain pMOS transistor is implanted. The transistor comprises three p^+ implanted regions: the source in the middle and the two drains on each side. A higher n^{++} region is implanted into the n-well providing the n-well contact for biasing. The pixel is separated from adjacent pixels with LOCOS¹ and p^+ stopper underneath the LOCOS. The pMOS pixels are ganged via both drain nodes, providing a two-dimensional strip-like read-out configuration. The design parameters for the pMOS pixel are listed in Table 1. For simplicity of the discussion, pMOS pixel study is presented for the case of a single-drain structure. In terms of operation principle there is no difference between a transistor with one or several drains.

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¹LOCOS stands for LOCal Oxidation of Silicon

Operation principle

The detector bias voltage is applied to the back side p^+ implantation while the n-well is grounded through the bias resistor R_B . As in strip-like detectors, within the resulting depleted junction the crossing charged particles are detected. The signal charge (Q_0) deposited in the substrate is accumulated on the n-well, and decays through the bias resistor. The accumulated charge provides a voltage shift in the n-well (V_{sub}), which modulates the drain current of the pMOS transistor operating in the saturation region. The drain current is then differentiated through the R_0C_0 network before being fed into the preamplifier.

Leakage current

The leakage current I_L of the reversed biased p-i-n diode is given by $I_L = i_L(W_{well})^2$ with i_L given by [11]:

$$i_L = \frac{1}{2}q \frac{n_i}{\tau_0} d \quad (1)$$

where $n_i = 1 \cdot 10^{10} \text{cm}^{-3}$ is the intrinsic concentration in silicon, $\tau_0 = 2.5 \cdot 10^{-3} \text{s}$ the carrier life time, and $d = 300 \mu\text{m}$ the detector thickness. A typical value of the leakage current will be $i_L = 10 \text{nA/cm}^2$, so that for a $100 \mu\text{m}$ by $100 \mu\text{m}$ n-well area, $I_L = 1 \text{pA}$ per pixel.

2.2 pMOS pixel transconductances

Transconductance

When the pMOS transistor is operating in the saturation region, the drain current I_d is written as:

$$I_d = \frac{1}{2} \frac{W}{L} \mu_s C_{ox} (V_{GS} - V_{TH})^2 \quad (2)$$

where W and L are the gate width and length, $\mu_s = 120 \text{cm}^2/\text{Vsec}$ the effective surface carrier mobility, V_{GS} the source-to-gate voltage, and V_{th} the threshold voltage. C_{ox} is the gate capacitance per unit area given by:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} \quad (3)$$

where t_{ox} is the oxide thickness, $\epsilon_0 = 8.854 \cdot 10^{-14} \text{F/cm}$ the permittivity in vacuum, and $\epsilon_{ox} = 3.9$, the dielectric constant of the oxide (SiO_2). The gate capacitance of the pMOS transistor is given by $C_G = WLC_{ox}$. The substrate bias voltage V_{sub} in the n-well due to crossing particles modulates the drain current I_d through V_{th} as:

$$V_{th} = 2\phi_{Fn} - \frac{qN_D L_D}{C_{ox}} \sqrt{\frac{2q|2\phi_{Fn} - V_{sub}|}{kT}} \quad (4)$$

where q is the electronic charge, k the Boltzmann constant, T the absolute temperature in Kelvin², N_D the n-well doping concentration, L_D the Debye length defined as:

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²At 300°K $kT/q = 25 \text{mV}$

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon_{si} kT}{q^2 N_D}} \quad (5)$$

and ϕ_{Fn} the Fermi potential in the n-well substrate:

$$\phi_{Fn} = -\frac{kT}{q} \ln \frac{N_D}{n_i} \quad (6)$$

with $\epsilon_{si} = 11.9$ the dielectric constant of silicon.

The "front-side transconductance" g_m for a input signal on the pMOS transistor gate is defined as:

$$g_m = \frac{dI_d}{dV_{GS}} = \sqrt{2 \frac{W}{L} \mu_s C_{ox} I_d} \quad (7)$$

"Back"-Transconductance

And the "back-side transconductance" g_{sub} , or drain current sensitivity for a input signal on the n-well is described as:

$$g_{sub} = \frac{dI_d}{dV_{sub}} = -g_m \frac{dV_{th}}{dV_{sub}} \quad (8)$$

It is apparent that the back side transconductance is proportional to the front side transconductance. The ratio g_{sub}/g_m :

$$\frac{g_{sub}}{g_m} = -\frac{dV_{th}}{dV_{sub}} = \frac{q N_D L_D}{2 C_{ox}} \sqrt{\frac{2q}{kT |2\phi_{Fn} - V_{sub}|}} \quad (9)$$

shows the detector sensitivity to crossing particles. It is essential to reduce the electronic noise coming from the front side and to amplify the input signal induced on the back side, i.e. g_{sub}/g_m should be as large as possible. It is apparent from the above equation that the back side sensitivity is inversly proportional to C_{ox} and therefore proportional to t_{ox} . In order to increase the ratio g_{sub}/g_m a thick gate oxide is required. Typically $t_{ox} = 540nm$ can be achieved by processing the gate oxide together with the LOCOS, as explain in the fabrication section.

2.3 Capacitances

The pMOS pixel detector capacitance C_B associated with the n-well is a major contribution to the noise estimation described in section 3. Since in the pMOS pixel application case the well-to-drain junction is reverse biased, and has a wide depletion layer, its junction capacitance is small, ($< 10\%$ of C_B) and therefore can be neglected. C_B can be split into three parts: well-to-back side capacitance (C_D), well-to-source capacitance (C_J), and well-to-channel capacitance (C_S), which gives:

$$C_B = C_D + C_J + C_S \quad (10)$$

C_D , well-to-back side capacitance

The detector capacitance per pixel when the p-i-n diode is full depleted, C_D is given by:

$$C_D = \epsilon_0 \epsilon_{si} \frac{A_d}{d} \quad (11)$$

where A_d is the pixel area and d the detector thickness.

C_J , well-to-source capacitance

The depletion width d_{j0} of the zero-biased n-well/ p^+ source junction is given by:

$$d_{j0} = \sqrt{\frac{2\epsilon_0\epsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D} V_{bi}} \quad (12)$$

where N_A is the doping concentration of the source region, and V_{bi} is the built-in potential of the pn junction defined as:

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \quad (13)$$

The zero-biased junction capacitance is given by

$$C_J = \epsilon_0\epsilon_{si} \frac{A_J}{d_{j0}} \quad (14)$$

where A_J is the source area.

C_S , well-to-channel capacitance

The junction capacitance between the p^+ channel and the n-well is given by C_S . The channel potential is the surface potential of the pMOS conduction channel $\phi_s = 2\phi_{Fn}$. The potential on the n-well is V_{sub} . Therefore the depletion width d_{sub} of this junction is described as:

$$d_{sub} = L_D \sqrt{\frac{2q|\phi_s - V_{sub}|}{kT}} \quad (15)$$

The well-to-channel capacitance over the whole gate region is given by:

$$C_S = \epsilon_0\epsilon_{si} \frac{WL}{d_{sub}}. \quad (16)$$

V_{sub} is taken to be equal to zero for this calculation.

The total capacitance with respect to the n-well concentration is shown in Figure 2. It increases monotonically with increased n-well doping concentration. We expect that there should be some optimum n-well doping concentration with respect to signal-to-noise ratio. This will be discussed in section 3. The derived parameters of the pMOS pixel calculated for the typical design parameters values: $t_{ox} = 540nm$ and $N_D = 1 \cdot 10^{16}cm^{-3}$, are summarized in Table 2.

3 Signal Processing

Figure 3 gives a schematic of the pMOS pixel equivalent circuit and subsidiary passive components. The p-i-n diode is reverse biased with $V_{bias} < 0V$ applied on the p^+ back side, while the n-well is grounded through the bias resistance $R_B = 10G\Omega$. The pMOS transistor is under a strong inversion condition with $V_{GS} < V_{th} < 0V$ applied to the gate. The pMOS transistor polarization $V_{DS} < 0V$ is applied to the drain. The output signal from the drain node is differentiated through the $R_0C_0 = 1M\Omega \times 0.15pF$. Parameters for a proposed signal processing pMOS pixel circuit are shown in Table 3.

3.1 Charge amplification

When a minimum ionizing particle penetrates through the detector, an impluse charge (Q_0) is deposited in the substrate and then decays through the bias resistance. The potential V_{sub} which appears on the n-well is written in terms of time domain t or in terms of angular frequency ω :

$$V_{sub} = \frac{Q_0}{C_B} \exp(-t/R_B C_B) \rightarrow \frac{Q_0}{C_B} \frac{1}{j\omega + 1/(R_B C_B)} \quad (17)$$

The current pulse which appears on the drain node, in addition to the DC component of the drain current $I_{d(dc)}$ given in Eq. (2), is given by:

$$I_d = I_{d(DC)} + g_{sub} V_{sub} \quad (18)$$

where g_{sub} is the back transconductance of the pMOS pixel for an input signal on the n-well node, defined in Eq. (8).

On the drain node, the current is differentiated with a time constant $t_0 = R_0 C_0$ leading to the output signal:

$$I_{out} = \frac{Q_0 g_{sub}}{C_B} \frac{j\omega}{(j\omega + 1/(R_B C_B))(j\omega + 1/t_0)} \quad (19)$$

In order to see an output signal, we choose the time constant of the differentiation network $t_0 = 150nsec$ to be much shorter than the decay time of the n-well $\tau = R_B C_B \approx 500\mu sec$. The output signal becomes $I_{out} = Q_0 G(\omega)$ where

$$G(\omega) = \frac{g_{sub}}{C_B} \frac{1}{j\omega + 1/t_0} \quad (20)$$

is the Fourier transform of the pMOS pixel charge amplification gain Q_{out}/Q_0 . From the definition of the Fourier transform the total output charge is given by:

$$Q_{out} = \frac{Q_0 g_{sub} t_0}{C_B} \quad (21)$$

The charge amplification gain is proportional to the back transconductance. Figure 4 shows the charge amplification gain in terms of the n-well doping concentration and the gate oxide thickness. From Eq. (9) and Figure 4 it is apparent than a higher n-well doping concentration and/or a thicker gate oxide gives a higher charge amplification, provided that the quiescent drain current is kept constant.

3.2 Noise analysis

Noise generators

The equivalent circuit of the p-MOS pixel with the noise generators is shown in Figure 5.

Pixel equivalent noise generators:

The detector leakage current per pixel I_L and the bias resistance R_B generate parallel noise i_n^2 's characterized by $2qI_L$ and $4kT/R_B$. The front and back transconductances generate series noise v_n^2 's characterized by $8kT/3g_m$ and $8kT/3g_{sub}$ respectively, [11] [10]. The parallel noise measured at the pixel output will be:

$$i_{n1}^2 = N_p \left\{ \frac{8kT}{3} \frac{g_m + g_{sub}}{g_{sub}^2} w^2 C_B^2 + \left(2qI_L + \frac{4kT}{R_B} \right) \right\} |G(w)|^2 \quad (22)$$

where N_p is the number of pixels ganged together and $G(w)$ the Fourier transform of the charge amplification gain given in Eq. (20).

Additional noise generators:

The DC drain current I_d and the resistance of the differentiation network R_0 generate parallel noise i_n^2 's characterized by $2qI_d$ and $4kT/R_0$ respectively. The preamplifier input FET transconductance $g_M = 1.5mS$ generates serie noise v_n^2 's characterized by $8kT/3g_M$. Their noise contribution is expressed as:

$$i_{n2}^2 = N_p \left\{ \frac{8kT}{3} \frac{1}{g_M} \frac{C_0^2 w^2}{1 + w^2 C_0^2 R_0^2} + \left(2qI_d + \frac{4kT}{R_0} \right) \frac{R_0^2 C_0^2 w^2}{1 + w^2 R_0^2 C_0^2} \right\} \quad (23)$$

which can be rewritten as:

$$i_{n2}^2 = N_p \left\{ \frac{8kT}{3} \frac{1}{g_M R_0^2} + \left(2qI_d + \frac{4kT}{R_0} \right) \right\} \frac{C_B^2 w^2}{g_{sub}^2} |G(w)|^2 \quad (24)$$

The total equivalent noise generator for the pMOS pixel at the preamplifier input is given by:

$$i_n^2 = i_{n1}^2 + i_{n2}^2 \quad (25)$$

which can be expressed as:

$$|i_n^2| = I_n^2 |G(w)|^2 \quad (26)$$

where I_n^2 the input noise power per pixel is given by:

$$I_n^2 = N_p (s_n^2 C_B^2 w^2 + p_n^2) \quad (27)$$

where

$$s_n^2 = \left\{ \frac{8kT}{3} (g_m + g_{sub} + \frac{1}{g_M R_0^2}) + \left(2qI_d + \frac{4kT}{R_0} \right) \right\} \frac{1}{g_{sub}^2} \quad (28)$$

and

$$p_n^2 = 2qI_L + \frac{4kT}{R_B} \quad (29)$$

Electronic Noise Charge

The p-MOS pixel can be regarded as a noise generator, $I_n^2 |G(w)|^2$, feeding into the preamplifier. The electronic noise charge at the preamplifier input is estimated by [12] as:

$$enc^2 = \frac{1}{2} \int_{-\infty}^{+\infty} I_n^2 |G(w)|^2 |H(w)|^2 df \quad (30)$$

where f is the frequency variable and $H(w)$ the filtering function of the preamplifier. The characteristics of the preamplifier used for the B-factory micro-vertex detectors have been given elsewhere [10]. Its filtering function has a double correlated sampling scheme defined by:

$$H(w) = \frac{1 - \exp(-jw\tau_s)}{\tau_a N_R} \frac{1}{jw} \frac{1}{jw + 1/\tau_a} \quad (31)$$

where $\tau_a = 150\text{ns}$ is the preamplifier's rise time, $\tau_s = 1\mu\text{s}$ the sampling interval, and N_R is the normalization constant for $G(w)H(w)$ described below.

Assuming that a unit charge is injected at $t = 0$, we should observe a peak at $t = \tau_s$. The peak amplitude of the preamplifier output is normalized as:

$$1 = \int_0^{\tau_s} g(t)h(\tau_s - t)dt \quad (32)$$

where $g(t)$ and $h(t)$ are time-domain presentations of $G(w)$ and $H(w)$, respectively. The integration of Eq.(32) gives:

$$N_R = \frac{g_{sub}}{C_B} \{t_0(1 - \exp(-\tau_s/t_0)) - \tau_a \exp(-\tau_s/\tau_a)\} \quad (33)$$

The electronic noise charge from Eq.(30) is written as:

$$enc^2 = \frac{1}{2} \frac{N_p s_n^2 g_{sub}^2}{\tau_a^2 N_R^2} F_1 + \frac{1}{2} \frac{N_p p_n^2 g_{sub}^2}{\tau_a^2 N_R^2 C_B^2} F_2 \quad (34)$$

where F_1 and F_2 are the integrals used to evaluate the electronic noise charge and are given by:

$$F_1 = \int_{-\infty}^{+\infty} \frac{1 - \exp(-jw\tau_s)}{(w^2 + 1/t_0^2)(w^2 + 1/\tau_a^2)} df \quad (35)$$

and

$$F_2 = \int_{-\infty}^{+\infty} \frac{1 - \exp(-jw\tau_s)}{w^2(w^2 + 1/t_0^2)(w^2 + 1/\tau_a^2)} df \quad (36)$$

These integrals evaluate to:

$$F_1 = \frac{t_0^2 \tau_a^2}{t_0^2 - \tau_a^2} \{t_0(1 - \exp(-\tau_s/t_0)) - \tau_a(1 - \exp(-\tau_s/\tau_a))\} \quad (37)$$

and

$$F_2 = 2\tau_s t_0^2 \tau_a^2 + \frac{\tau_a^2 t_0^2}{t_0^2 - \tau_a^2} \{\tau_a^3(1 - \exp(-\tau_s/\tau_a)) - t_0^3(1 - \exp(-\tau_s/t_0))\} \quad (38)$$

Under the assumption that t_0 and τ_a have approximately the same value, and τ_s is larger enough than τ_a , N_R , F_1 and F_2 can be reduced to

$$N_R \rightarrow \frac{g_{sub} \tau_a}{C_B} \quad (39)$$

$$F_1 \rightarrow \frac{1}{2} \tau_a^3 \quad (40)$$

$$F_2 \rightarrow \tau_s \tau_a^4 \quad (41)$$

The electronic noise charge per pixel is eventually approximated by:

$$enc^2 \rightarrow s_n^2 C_B^2 \frac{1}{4\tau_a} + p_n^2 \tau_s \quad (42)$$

For N_p pixels ganged together in a line, the electronic noise charge is calculated as $\sqrt{(N_p)enc}/\text{pixel}$. The electronic noise charge due to a single pixel can be as low as 24 electrons. The total detector capacitance for a strip made of 256 pixels is $256 \times C_B \approx 6.2\text{pF}$. And the corresponding electronic noise charge is about 388 electrons. Figure 6 shows electronic noise charge in terms of oxide thickness and n-well doping concentration and shows that the optimum n-well doping concentration was about $1 \cdot 10^{17}\text{cm}^{-3}$. The concentration of $1 \cdot 10^{16}\text{cm}^{-3}$ was chosen to keep the integral non-linearity better than 10%. The linearity issue is discussed in the next section.

3.3 Linearity

Dynamic range or integral non-linearity is another concern of the signal processing. Since the transconductance of the pMOS transistor is affected by the signal itself, the integral non-linearity has to be compromised with the charge gain and/or the electronic noise charge. The deviation from linear response can be described as:

$$\eta = \frac{I_d(Q_0) - I_d(DC)}{I_d(24000q) - I_d(DC)} \quad (43)$$

where $Q_0 = 24000q$ compares with the signal resulting from a minimum ionizing particle penetrating through a $300\mu m$ depletion width. The maximum and/or minimum of η over $Q_0=0$ to $24000q$ gives a measure of the integral non-linearity. As shown in Figure 7 the integral non-linearity was worse for thicker t_{ox} and denser N_D , while thicker oxide and denser n-well doping concentration favoured the charge amplification gain.

4 Fabrication

6k2cm $\rightarrow$ Table 4 shows the list of the process steps used for the fabrication of the pMOS pixel. The fabrication is realised on 4 inch diameter and $300\mu m$ thick wafer. To reduce the bias voltage value required to fully deplete the detector, a high resistivity n-type silicon substrate is used, with a resistivity of about $6k\Omega\cdot cm$. As it has been described in section 2, in order to increase the detector back sensitivity, the pMOS transistor used in the pixel has a thick gate oxide. The standard MOS technology uses thin gate oxide of about 42nm, while the oxide layer in the pMOS pixel case is at least 300nm thick. To obtain such a thickness, the oxide is grown together with the LOCOS process step. Within the prototype fabrication, process variations are realised, leading to 3 different oxide thicknesses: $t_{ox} = 330nm$ or $540nm$ or $1100nm$, and 2 different n-well doping concentrations: $N_D = 5 \cdot 10^{15}cm^{-3}$ or $1 \cdot 10^{16}cm^{-3}$. This will allow us to check the pMOS pixel characteristics in terms of fabrication parameters.

Prototypes of the pMOS pixel have been fabricated by Seiko Instruments Inc. The prototypes include several types of test device which will be used to check the pMOS pixel properties. Single pMOS pixels equipped with single-drain and double-drain pMOS transistor will be used to measure the different pMOS pixel characteristics such as charge amplification, back side sensitivity, and response to signal input on the n-well. Geometry variation of the gate width and length are included in these prototypes. Structures having 3×3 pixel configurations have also been drawn, in order to check the position resolution of the pMOS pixel.

5 Summary

A theoretical picture of a pMOS pixel detector was described in terms of pixel's configuration, transistor operation, and signal processing. It was demonstrated that we could use practical fabrication parameters which are still compatible with common MOS fabrication technology. Due to an amplification action of the pMOS transistor, the electronic noise charge was 388 electrons or less for 256 pixels ganged together. It was apparent that there was an optimum value of N_D in terms of equivalent noise charge. Optimization between charge amplification gain and the integral non-linearity was another factor in determining fabrication parameters.

An experimental fabrication procedure is in progress to confirm theoretical calculations and to fix design parameters for a real pixel detector.

Acknowledgements

We would like to acknowledge the encouragement of the directors H. Sugawara, Y. Kimura, S. Iwata, F. Takasaki, M. Kobayashi and K. Nakai. The present work is based on the B-factory silicon detector group: Y. Higashi, M. Ikeda, S. Koike, H. Ozaki, M. Tanaka, T. Tsuboyama, S. Okuno, S. Mori, K. Yusa, J. Haba, H. Hanai, D. Tatsumi, K. Adachi, T. Kawasaki, Y. Nagashima, C. Fukunaga, T. Matsushita, H. Miyata, and K. Miyano. The following people at Seiko Instruments Inc. are assisting the prototype fabrication: H. Takeuchi, M. Mandai, O. Koseki, T. Yoshino, H. Kanazawa, J. Yamanaka, S. Miyahara, and K. Kamiya.

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Parameter	Definition	Value
d	detector thickness	$300\mu m$
A_d	pixel area	$200\mu m$ by $200\mu m$
W_{well}	n-well area	$100\mu m$ by $100\mu m$
N_D	n^+ n-well concentration	$5 \cdot 10^{15} cm^{-3}$ $1 \cdot 10^{16} cm^{-3} (typ)$
N_A	p^+ Source and Drain concentration	$5 \cdot 10^{19} cm^{-3}$
A_J	source area	$4\mu m \times 4\mu m$
W/L	gate size	$4\mu m/4\mu m$
t_{ox}	gate oxide thickness	$330nm$ $540nm (typ)$ $1100nm$

Table 1: Design parameters for the pMOS pixel

Parameter	Definition	Value
C_{ox}	oxide capacitance	$63.9aF/\mu m^2$
C_G	4/4 gate oxide capacitance	$1.02fF$
C_D	detector capacitance	$14.0fF$
C_J	well-to-source capacitance	$4.85fF$
C_S	well-to-channel capacitance	$5.56fF$
C_B	total capacitance $= C_D + C_J + C_S$	$24.4fF$
ϕ_{Fn}	Fermi potential of the n-well	$-0.35V$
L_D	Debye length	$41.3nm$
V_{bi}	source-well built-in potential	$0.92V$
V_{TH}	Threshold voltage	$-8.27V$
V_{GS}	gate bias voltage	$-9.0V$
$I_d(DC)$	drain current	$200nA$
I_L	leakage current	$1pA/pixel$
g_m	"front" transconductance	$0.56\mu S$
g_{sub}	"back" transconductance	$3.03\mu S$

Table 2: Summary of derived parameters, calculated for the typical design parameters values: $t_{ox} = 540nm$ and $N_D = 1 \cdot 10^{16} cm^{-3}$

R_B	well bias resistance	$10G\Omega$
$\tau = R_B C_B$	decay time in the well	$250\mu s$
C_0	capacitance of differentiation network	$0.15pF$
R_0	resistance of differentiation network	$1M\Omega$
$t_0 = R_0 C_0$	differentiation time constant	$150ns$
τ_a	amplifier's rise time	$150ns$
τ_s	sampling interval	$1\mu s$
g_M	amplifier transconductance	$1.5mS$
N_p	number of pixels ganged	256
V_{DS}	drain bias voltage	$-5V$
V_S	source bias voltage	$0V$
V_{well}	n-well bias voltage	$0V$
V_{Bias}	back side bias voltage	$-80V$
	small signal charge gain	18.6
η	integral non-linearity	11.2%
enc	Electronic Noise Charge	388electrons

Table 3: Parameters of pMOS pixel connection circuit during signal processing

Process step	$\Rightarrow$ making	typical value
Phosphorus Ion implantation	$\Rightarrow$ n-well	$N_D = 5 \cdot 10^{15} cm^{-3}$ $1 \cdot 10^{16} cm^{-3} (typ)$
Boron Ion Implantation	$\Rightarrow P^+$ stopper isolation between pixels	$P^{++} = 7 \cdot 10^{18} cm^{-3}$
LOCOS Oxidation	$\Rightarrow$ LOCOS & gate oxide	$t_{ox} = 330nm$ $540nm (typ)$ $1100nm$
Polysilcon deposition	$\Rightarrow$ gate	350nm thick
Boron Ion implantation	$\Rightarrow$ drain & source	$N_A = 5 \cdot 10^{19} cm^{-3}$
Boron Ion implantation	$\Rightarrow$ back side implantation	$P^+ = 5 \cdot 10^{19} cm^{-3}$
Phosphorus Ion Implantation	$\Rightarrow$ n-well contact	$N^{++} = 1 \cdot 10^{21} cm^{-3}$
Contact etching	$\Rightarrow$ drain, source, n-well & back side contacts	
Aluminum deposition	metal connections	$1.0\mu m$ thick
Passivation	$\Rightarrow$ pads opening	

Table 4: Process sequences for the pMOS pixel fabrication

Figure captions

Figure 1 A simplified structure of the pMOS pixel.

Figure 2 Total capacitance versus n-well doping concentration.

Figure 3 Schematic equivalent circuit of the pMOS pixel for signal processing.

Figure 4 Charge amplification gain with n-well concentration and oxide thickness dependence.

Figure 5 Equivalent circuit with p-MOS pixel noise generators. The pixel structure itself generates the following noise: due to bias resistance R_B , $i_n^2 = \frac{4kT}{R_B}$; due to the leakage current I_L , $i_n^2 = 2qI_L$; due to front transconductance g_m , $v_n^2 = \frac{8kT}{3g_m}$; and due to back transconductance g_{sub} , $v_n^2 = \frac{8kT}{3g_{sub}}$. The differentiation network (R_0C_0) generates noise: due to the drain current Id_{DC} , $i_n^2 = 2qId_{DC}$; and due to the resistance R_0 , $i_n^2 = \frac{4kT}{R_0}$.

Figure 6 Electronic Noise Charge with n-well concentration and oxide thickness dependence.

Figure 7 Integral non-linearity with n-well concentration and oxide thickness dependence.

Figure 1:

Figure 2:

Figure 3:

Figure 4:

Figure 5:

Figure 6:

Figure 7: