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Abstract

A fast time-to-digital converter with a 5 ns step was designed and tested by utilizing a user-programmable gate array. The stabilities against temperature and supply voltage variation were measured. A module was built with this TDC, and was successfully used in the first-level trigger system of the ZEUS detector to reject proton-beam induced background events.

1 Introduction

In high-energy physics experiments, it is frequently required to separate two classes of events with a several nanosecond time difference during an early stage of the trigger. A conventional way is to make a tight coincidence between the signal and a reference signal with a very narrow gate width. Stable operation of such a narrow gate coincidence is, however, not so easy.

An alternative solution is to measure the time difference directly with a time-to-digital converter(TDC) and to set a threshold on the converted time. A requirement on the TDC in that operation is a fast conversion time in order to keep the deadtime at a minimum. Once a sufficient resolution is achieved for discriminating the time difference, the conversion coefficient of the TDC does not

necessarily have to be high, since the primary purpose is to set a threshold at a certain point, not to obtain the time spectrum.

We have constructed such a TDC by building a pipeline in one chip of a commercially available C-MOS gate array: the XC3020 of XILINX[1]. Since the gate array is user-programmable, the development cost was very minimal. We have found the time resolution to be better than 1 nano second and applicable for discriminating a time difference of several nano seconds. The stability against temperature and supply voltage variation was sufficiently good.

A module was produced with these TDC chips and installed in the first-level trigger system of the ZEUS experiment[2] at HERA. The module was used to separate an approximately 20ns time difference measured by plastic scintillation counters between the beam-gas backgrounds and a true ep collision.

2 Operation Principle

The principle mechanism of the TDC is shown in Figure 1. The signal to be measured (TDC-start) is connected to a delay line with 13 taps. At each tap, a rising-edge trigger D-type flipflop (DFF) is connected. The clock signal of the 13 DFFs are connected together to a reference timing signal (TDC-stop). At the rising edge of the reference signal, each DFF records the level of each output tap, and thus records the level of the signal at different times. The rising-edge detection circuit, which follows the DFF arrays, converts the signal pattern to the edge position. The information is converted to a 4-bit digit with a priority encoder. There is one extra bit used to identify multiple hits, which is high if more than one rising edge are detected.

The delay between 2 DFFs corresponds to the conversion coefficient of the TDC. The resolution is determined mainly from the clock timing resolution of the DFFs, which is proportional to the data setup and hold time. In spite of the fact that this value for CMOS-type ICs is typically more than several nano-seconds, we can expect a much better resolution when all of circuits are built in one chip.

The total length of the delay line determines the time range of the TDC, which is limited to be less than 100 ns in this TDC scheme. It is, however, sufficiently long to discriminate a time difference of several nano seconds. Moreover, by adding storage memories to the output and by feeding a periodic signal for the TDC-stop, it is possible to construct a deadtime-free long-range pipeline TDC, since the cycle of the stop signal can be shorter than the total delay length in the delay line.

We installed the circuits on a user-programmable gate array, an XC3020 of XILINX[1]. The XC3020 has 8×8 configurable logic blocks (CLBs) and 58 input output blocks (IOBs) inside. A CLB has 2 DFFs and 2 memory lookup tables (MLTs) which can be programmed to any logic. The IOB serves as an interface to the outside of the IC, and can be programmed as an input and/or an output. The CLBs and IOBs can be connected very flexibly by activating connections between the blocks and previously laid lines.

A delay line is formed with a series of 13 CLBs connected to the shortest lines, called "direct lines", in between. The CLBs are arranged in an L-shape in the chip, as shown in Figure 2.

A DFF in the CLB is used to record the signal. The TDC-stop signal is fed to the clock input of each DFF through a global buffer and global nets, which is the signal-distribution mechanism with the smallest skew inside the chip.

The rising-edge counter and the priority encoder, which convert the 13 DFF outputs to a 4 bit digit, are built by utilizing 17 CLBs. A TDC is formed with 30 CLBs in total. Thus, we could put two TDCs with common STOP signals in an XC3020.

3 Performance

The performance of the TDC was tested with the setup shown in Figure 3. Both start and stop signals were generated from an NIM-level pulse generator at a rate of $(96 \text{ ns})^{-1}$. Both signals had a width of 48 ns, i.e. they had a 50% duty cycle.

These signals were converted to the TTL level and put into the TDC. The delay time was shifted by a 1 ns step and for each step, and the TDC output values were recorded by using LED's and a scope.

All of the measurements were carried out separately for the two TDCs installed in the chip.

Figure 4 shows an example of the TDC output as a function of the time delay. The zero point was adjusted to the time when the start and stop signals arrive at the TDC at the same time. In the figure, the circles show that the output was stable, and the triangle indicates that the output was fluctuating between two adjacent digits. Since this instability occurred very rarely, and only at the edge of the step function, the fluctuation in digitization could be deduced to be less than 1 ns.

A step function was fit to the measured points.

$$TDC \text{ output} = INT\left(\frac{t - t_0}{C}\right), \quad (1)$$

where $INT(A)$ is a function which truncates A to an integer; C and t_0 are free parameters of the fit, and correspond to the conversion coefficient of the TDC and the offset time when the step function rises from -1 to 0 , respectively.

A comparison was made for TDCs with three types of programmable gate arrays with different speeds: XC3020-70, XC3020-100 and XC3020-125. The numbers indicate the maximum toggle frequency in MHz for the DFFs in the CLBs. According to the specification, the maximum delay time between two CLBs of the delay line is 8 ns for XC3020-70 (7 ns inside the CLB and 1 ns from the connection line).

The fitting results are given in Table 1. Since the conversion coefficients obtained from the two TDCs in one chip were similar, the averages of the two are also listed. The time offset for the two TDCs are different by ~ 1 ns. This is due to the different path length from the input pads to the first CLBs of the delay line. A faster chip produces a faster delay line, as expected, resulting in a finer time resolution.

The TDC output was stable and reproducible for several measurements. For quantitative purposes, we checked the stability against variations of the temperature, supply voltage and signal pulse width.

The dependence on the temperature was measured by putting a test board with an XC3020-100 into a thermostatic unit. The fluctuation in the temperature at the board was measured to be within 0.1°C . The temperature was varied from room temperature (20°C) to 60°C . We repeated the measurements twice for each channel, and an average of the two measurements was obtained. The temperature dependence of the conversion coefficient and offset are shown in Figure 5.

The conversion coefficient and offset increased linearly as the temperature increased. Channel 1, which has a bigger time offset, seems to have a larger temperature dependence in its offset. This may show the different characteristics of the lines connecting the input pads to the inputs of the delay line. The temperature dependence of the conversion coefficient is similar for both channel. The averaged temperature coefficient was $13.7 \pm 0.8 \text{ ps}/^\circ\text{C}$, which corresponds to $0.3\%/^\circ\text{C}$.

The dependence on the supply voltage was measured by varying the voltage from 4.8 to 5.2 V at room temperature. The results are shown in Figure 6. The coefficient decreased linearly as the voltage was increased. The slope coefficient was $-0.34 \pm 0.11 \text{ ps/mV}$.

Finally, the dependence on the pulse width was checked. The signal width of the start signal was varied from 20 ns to 70 ns (or from 20% to 70% duty cycle). We found that the TDC output did not depend on the pulse width.

4 Application to the ZEUS Trigger system

The TDC was used in the first-level trigger (FLT) system in the ZEUS experiment[2] at HERA. HERA is the first electron-proton collider with a 96 ns bunch-crossing interval. Severe background was foreseen from the proton beam, such that nearly 1% of the beam crossing would encounter some hits inside the ZEUS detector. The majority of the background is generated by interactions between the proton beam

and residual gas inside the beam pipe or machine elements in the long straight section upstream of the detector.

A set of small scintillation counters (C5) partially surrounding the beam pipe are located in the proton-beam about 3 m upstream from the nominal interaction point. In case of the background interactions which occur further upstream of the proton beam, secondary particles hit the counters with a high probability. The timing of a hit is ~ 20 ns earlier than that of particles produced in ep collisions. The signal from the counter can therefore be used as a VETO in the trigger system, once this time difference is distinguished.

The C5 counters comprise two sets of 2 layers of plastic scintillators, whose dimensions are about $100 \times 150 \times 2.6 \text{ mm}^3$. A set of two scintillators, viewed from the beam direction, looks like the hoof of a horse, and surrounds about three-fourths of the beam pipe. Between the two layers, a 2 mm thick lead sheet is placed in order to eliminate any synchrotron radiation from the electron beam. Each layer is read out with a PMT. For each set of counters, the coincidence signal of the layers is first generated, then split and fed as TDC-start signals to the 2 TDCs in a single chip. For one input, an extra 2 ns delay was inserted in order to measure the time with a different bin boundary. The HERA machine clock, whose repetition cycle is 96 ns, was used for the TDC-stop. Thus, the C5 hit timing for each bunch is obtained with 4 TDCs in 2 chips.

An example of the time spectra of the counters recorded with one TDC is shown in Figure 7. Two peaks are clearly separated in the figure. Note that a larger TDC count means an earlier time in this setup. The right peak is from the proton-beam background, and the left one is from the electron-beam background, which comes to the C5 counters with the same timing as genuine ep events. The ZEUS main trigger is vetoed if a set of two TDCs, which measure the signals from the same counter, indicates the proton timing hit under the condition that none of the TDCs indicate the ep timing.

The TDC worked stably during the HERA running period in 1992 and 1993. The veto rate per bunch was 0.04% on the average for the 1992 runs and 0.05% for

the 1993 runs. The trigger rate at the first-trigger level was reduced from 400 Hz to 120 Hz in the 1993 runs by using this signal as a VETO.

The peak position of the proton background was monitored for an entire run period, and compared with the TDC data independently taken with LeCroy's TDCs (LRS2228). Both peak positions are consistent with each other within 1 ns.

5 Acknowledgements

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References

- [1] The programmable logic data book 1994, XILINX.
- [2] The ZEUS Detector, Status Report 1993, ed.by U.Holm.

Figure 1: Principle of the TDC. The shadowed bold line indicates the delay line. This figure shows a case in which a start signal reaches the delay line between the third and fourth taps.

Figure 2: (Upper) schematic view of a pipeline TDC. The remaining space of the XC3020 is used as an edge detector and priority encoder. (Lower) a inside view of a CLB surrounded by a bold circle line in the upper figure. An output X(Y) is connected to the edge detector(next to the CLB).

Figure 3: Setup of the performance tests. During the temperature-dependence measurements, the area surrounded by the dotted rectangle was put into a thermostatic unit.

Figure 4: Example of the TDC output (room temperature, XC3020-100). The circles and triangles indicate the measured points. The solid line indicates the fitted step function defined in the text.

Figure 5: Temperature dependence of the conversion coefficient C (left) and offset t_0 (right). The upper(lower) is channel 1(2). The circles indicates the measured points. These points were fitted with a straight line for determining the temperature coefficients.

Figure 6: Supply voltage dependence of the conversion coefficient and offset. The voltage coefficient was determined in the same way as those of the temperature.

Figure 7: TDC histogram obtained from typical runs of the ZEUS experiment in 1992. Data were taken with a self trigger. Since a 100 MHz chip was used, one bin width was about 5 ns, as described in section 3.

Chip	Conversion Coefficient (ns/digit)			Time Offset (ns)	
	Channel 1	Channel 2	Average	Channel 1	Channel 2
XC3020-70	6.87 ± 0.10	6.89 ± 0.08	6.88 ± 0.09	2.68 ± 0.55	1.72 ± 0.55
XC3020-100	5.12 ± 0.10	5.01 ± 0.10	5.07 ± 0.13	2.25 ± 0.72	1.45 ± 0.65
XC3020-125	4.12 ± 0.09	4.08 ± 0.06	4.10 ± 0.08	1.24 ± 0.66	0.86 ± 0.12

Table 1: Results of the TDC conversion coefficients and offsets for various chip speeds.