Final report on HV/HR CMOS devices

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The main goal of WP6 was to develop novel high voltage/high resistivity (HV/HR) CMOS active sensors for High Energy Physics applications. Initially, the target of the work package was to explore the performance and assembly process of hybrid (AC coupled) HV/HR CMOS devices. Various interconnection options between active pixel sensors and readout chips were realized. However, early into the hybrid active pixel activities, it was recognized that this approach would not offer clear advantages over current hybrid technologies. The focus then shifted towards monolithic devices, where the sensor and the readout blocks are integrated in the same silicon bulk. The breakthrough for the WP activities was to exploit the improvements in the manufacturing industry, that offered processing with high voltage or high resistivity wafers to obtain a large depleted region, that improved charge collection with respect to other CMOS technologies. Several depleted CMOS prototypes were developed within the WP, which can be classified in two groups: devices with small and devices with large charge collecting electrodes. Both approaches were extremely successful, and unprecedented advances were made in terms of speed and radiation hardness.
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Executive summary

The main goal of WP6 was to develop novel high voltage/high resistivity (HV/HR) CMOS active sensors for High Energy Physics applications. Initially, the main target of the work package was to explore the performance and assembly process of hybrid coupled HV/HR CMOS devices. In these hybrid devices, the active sensor and the readout electronics are placed in two separate substrates and interconnected with solder bumps (DC) or through capacitive coupling (AC). The hybridization process is technically demanding since the pixel size is extremely small (tens of μm). Various interconnection options between active pixel sensors and readout chips were realized. Within the WP the fabrication process of AC coupled devices was first investigated with test structures. Eventually, both AC and DC coupled hybrid CMOS devices were fabricated and characterized. However, while the DC coupling process is costly and offers no advantage with respect to current hybrid devices, the initial studies of AC couple devices also indicated difficulties in achieving uniform capacitive coupling across all the pixels, albeit the use of pillars to aid the hybridization process improved the uniformity of the capacitive coupling.

The experience with CMOS hybrid devices led to the conclusion that this approach would not offer clear advantages over current hybrid technologies. The focus then shifted towards monolithic devices, where the sensor and the readout blocks are integrated into the same silicon bulk. The breakthrough of the WP activities was to exploit the improvements in the manufacturing industry that offers processes that allow a relatively high bias voltage (HV) to be applied to the substrate, thus leading to a larger depletion region. At the same time, the use of high resistivity (HR) wafers to obtain a large depleted region that improved charge collection with respect to other CMOS technologies. Several depleted CMOS prototypes were developed within the WP, which can be classified into two groups: devices with small and devices with large charge collecting electrodes. The two approaches offer different advantages, in the case of the large electrode configuration, the results seem to indicate that a better radiation hardness can be achieved, while the small electrode design requires less power (due to the lower pixel capacitance), which can lead to faster devices. The details of the specific requirements of the particular use-case will determine which is the best design. Both approaches were extremely successful, and unprecedented advances were made: prototypes were designed, fabricated, irradiated and fully tested in laboratories and beam tests. These activities led to a large number of publications (23, up to March 2020), and constitute the scientific cornerstone on which the next generation of experiments that will surely rely on depleted CMOS devices, will build upon.

1. INTRODUCTION

The goal of the WP6 was to investigate High Voltage and Resistive (HV/HR) CMOS sensors for high energy physics (HEP). CMOS devices for radiation detection already existed but the charge collection mechanism relied on charge diffusion, given that the depleted region of these devices was extremely small. Charge diffusion leads to slow devices that are intrinsically radiation soft, so this technology was not used in high energy physics experiments. Recently a way to overcome this limitation was proposed in [1]. The main idea was to exploit the advancements in the microelectronic industry that offers processes that allow a relatively high bias voltage (HV) to be applied to the substrate, thus leading to a larger depletion region. At the same time, the use of high resistivity (HR) silicon wafers also results in larger depletion regions. In turn, larger biases and higher substrate resistivities enable charge collection by drift, a faster and more radiation hard mechanism. Initially, the main target of the work package was to explore the performance and assembly process of AC coupled HV/HR CMOS devices. In these devices, the CMOS sensor includes an analog amplification block that is then connected to a separate substrate (the readout chip) where further amplification or, directly, the digital processing of the signal is done. Various interconnection options between active pixel sensors
and readout chips were realized. However, early into the hybrid pixel activities, it was recognized that this approach would not offer clear advantages over current hybrid pixel technologies. The interconnection process, even in the simplified AC coupling approach, was still complicated and time-consuming, precisely the weaknesses of the traditional hybrid approach that the HV/HR CMOS technology promised to overcome.

The focus then shifted towards monolithic devices, where the sensor and the readout blocks are integrated into the same silicon bulk. Here the challenge was to develop, in a single substrate, the full suite of blocks that are separated in the standard devices: a sensing block, fast and relatively radiation hard, an analog step that amplifies the signal, and the digital process that also communicates with the data acquisition system. Several depleted CMOS prototypes were developed within the WP, which can be classified into two groups: devices with small and devices with large charge collecting electrodes. Both approaches were extremely successful, and unprecedented advances were made in terms of speed and radiation hardness.

The results and lessons learned in the hybrid activities are presented in section 2, while section 3 summarized the results of the development of monolithic CMOS devices for HEP applications.

2. INITIAL STUDIES WITH HYBRID DEVICES

As mentioned before, the initial approach to pixel CMOS sensors consisted of the development of devices with an active pixel sensor (meaning a sensor with an integrated amplification stage fabricated in the HV-CMOS technology) interconnected to a dedicated readout chip (ASIC). The most promising interconnection process was based on AC coupling. Test structures to study the performance of different methods of fabrication of AC coupled devices were designed and produced [2]. The main idea was to use a matrix of capacitors to test the uniformity of the gluing process. Two structures, shown in Figure 1, each containing one side of the capacitor were produced by companies participating in the project. The assembly procedure was to deposit the glue on top of one of the structures, and then align both structures (one with glue, one without) and apply light pressure to produce the hybrid device. By probing the pads in the edge of the device, the capacitance of the different “pixels” can be measured. Some structures were fabricated with pillars, which ultimately were shown to improve uniformity. Pillars of different height (3 and 5 µm) were deposited on 3 wafers through a photolithography process.

![Figure 1. Process of fabrication of test structures for AC coupling studies (left). Fabricated structures are shown in the center. The sample size is 1.5 × 1.5 mm². The pads to measure the capacitance of each pixel can be seen. The SEM picture on the right shows an AC coupled test structure.](image-url)

To produce the assemblies, different glues were used: Araldite 2011, 2020 and Masterbond (UV15DC80LV) and Tesa tape. A flip-chip machine, which allowed to align and bring together the
two pieces applying pressure, was used. Finally, the samples were allowed to cure. A detail of the assembly is shown in Figure 1. The best results, obtained with the use of pillars deposited with a photo-lithography process, resulted in a spread of the pixel capacitance of about 10%. These encouraging results on test structures were followed by the fabrication of full-sized assemblies based on depleted CMOS prototypes, in particular using the H35Demo.

The H35Demo [3] is a demonstrator chip produced in the 350 nm AMS technology. It is a large area chip, $18.49 \times 24.40 \text{ mm}^2$, which contains four-pixel matrices: a standalone (monolithic) nMOS matrix, two analog matrices, and a standalone CMOS matrix. In the context of the WP activities, H35Demo devices were AC and DC coupled to the FE-I4 readout chip. For AC devices, a dispensing machine was used to deposit a thin layer of epoxy glue with good uniformity over the CMOS chip. A high-precision flip-chip machine was used to align and perform the gluing cycle (heat, and apply pressure) in order to capacitively couple the CMOS sensors to the FE-I4 ASICs (see Figure 2, left).

Another approach that was investigated within the WP activities was the fabrication of devices that combined DC and AC coupling of depleted CMOS sensors to ASICs. This approach could be used to produce assemblies that rely on solder bumps, for power distribution and rigidity, while the pixels are AC coupled. Such a device is shown on the right, in Figure 2.

The resulting assemblies were measured before and after irradiation in beam test at the Fermilab Test Beam Facilities with 120 GeV protons and CERN SPS H8 beamline using 180 GeV pions. The in-time efficiency and tracking properties measured for the different sensor types are shown to be compatible with the ATLAS ITk requirements for its pixel sensors. See reference [4] for details.

Following these results, efforts were made to industrialize the AC coupling procedure by developing a wafer-level process. With this in mind, wafer-level packaging was investigated to obtain larger detectors reassembling good tiles for the AC coupling process on a full wafer.

However, it is important to note that the focus of the WP6 activities changed from AC coupled to monolithic devices (where no hybridization step is needed). At the time of the preparation of the AIDA-2020 proposal, the AC coupling hybridization technique for CMOS sensors was thought to be the best approach to produce CMOS devices. But even though progress was made, the experience showed that the hybridization process, either with the AC or the DC option, was too complex to really be a more cost-effective alternative to traditional hybrid devices. While, on the other hand, the CMOS devices did not show improved radiation hardness. Thus, the development of monolithic devices targeting moderate radiation hardness was undertaken as the main activities of the WP. This approach is clearly more convenient since the hybridization step is avoided altogether.
3. DEVELOPMENT OF MONOLITHIC DEVICES

After the lessons learned during the development of hybrid active pixel sensors coupled to readout chips, the focus of the WP shifted to monolithic devices. The early prototypes aimed to be fast enough and radiation hard enough to be operated in the High-Luminosity LHC (HL-LHC) upgrade of the experiments, were produced in the HV-CMOS technology using medium to high resistivity wafers (up to 1 kΩcm). These devices implemented a large collecting electrode (based on a deep n-well) to ensure sufficient charge collection. Different approaches were investigated with various foundries (first in AMS – Austria, and then in LFoundry – Italy). An alternative design was realized, that instead presented a small collecting electrode. In this case, the idea was to reduce the pixel capacitance of the devices (and thus power consumption) while retaining sufficient radiation hardness. These devices were developed mainly with TowerJazz – Israel. The following section presents the outstanding advancement that was made through the WP activities in these two approaches.

It is worth noticing that a large number of prototypes of different sizes for various applications were fabricated in the context of the WP activities. The following section only mentions a few of them. The full list of results is presented in [5].

3.1 MONOLITHIC DEVICES WITH LARGE ELECTRODES

The first prototype designed to investigate radiation-hard depleted monolithic active pixel sensors (DMAPS) in the context of the LHC experiments was the H35DEMO, a large electrode full reticle demonstrator chip produced in AMS 350 nm HVCMOS technology. It includes two large electrode designed monolithic pixel matrices which can be operated stand-alone. One of these two matrices was characterized at beam test before and after irradiation with protons and neutrons. Results demonstrated the feasibility of producing radiation-hard large area fully monolithic pixel sensors in HV-CMOS technology. H35DEMO chips with a substrate resistivity of 200 Ωcm irradiated with neutrons showed a radiation hardness up to a fluence of 1E15 n/cm² with a hit efficiency of about 99 % and a noise occupancy lower than 10−6 hits in an LHC bunch crossing of 25 ns at 150 V [6].

These early encouraging results led to the design of various follow-up prototypes.

The ATLASPIX1 and MUPIX8 are large monolithic pixel sensors implemented in AMS aH18 process on different high resistivity substrates [7]. The designs were based on isolated PMOS structures in deep p-wells (see Figure 1). The MUPIX8 has an area of 1 cm × 2 cm, 128×200 pixels of 80 μm × 81μm size. Zero suppressed signals (hits) are readout and transmitted via four digital links that operate at a rate of about 1.25-1.6 Gbit/s. The test system had been developed within the AIDA project. The ATLASPIX1 has been submitted in three versions, each with a matrix area of about 20 mm × 3 mm. Two chip versions have an un-triggered readout, while one version has triggered readout.

Figure 1. The ATLASPIX1 schematic pixel layout. The collection electrode is labeled DNTUB.

The ATLASPIX1 and the MUPIX8 prototypes have been characterized in detail. Detection efficiencies above 99% were measured. After irradiation, of more than 100 MRad and 1E15 n/cm², the detection efficiency was still excellent (about 99%), while the time resolution was in the range 7 to 10 ns (RMS).
The results obtained with the large electrode design highlight the strengths of the approach. Achieving excellent efficiency with monolithic devices after irradiation up to $1 \times 10^{15}$ n\textsubscript{eq}/cm\textsuperscript{2} was not expected and demonstrates the advancement and the potential of the technology.

### 3.2 MONOLITHIC DEVICES WITH SMALL ELECTRODES

Several prototype chips were also fabricated in the small electrode design. The ones detailed here were fabricated at ToweJazz and LFoundry [8, 9]. The specifications evolved as the technology matured. The first prototype had a primitive analog front-end circuit in each pixel. It was aimed at investigating the basic sensor performance. The Malta and TJ-Monopix are large scale chips with ALPIDE-type analog front-end and fast readout digital logics. The analog front-end of both chips were very similar but the fast readout was different from each other. In Malta, the pixel logic is asynchronous to the clock. The power consumption can be lowered by not distributing the clock signal to pixels. TJ-Monopix employed the column-drain architecture, which is also employed and tested well with LF-Monopix. In this architecture, the base clock of 40 MHz was distributed to the pixels. Although the power consumption will be higher than the asynchronous readout, its robust architecture has already proven to be useful in FE-I3 (the current ATLAS ID Pixel Detector readout chip). The fourth prototype (Mini-Malta) had a modified analog front and sensor structure.

Figure 2 shows the cross-section of the TowerJazz 180 nm CMOS process with a special low-dose n-type implant addition across the full pixel matrix. This sensor structure was employed in the MALTA and TJ-Monopix1 chips. This implant generates the junction to deplete the epitaxial silicon layer (25 μm thickness). The n−layer separates the deep p-well of the pixel circuit from the p-type substrate. The substrate is reverse biased (0 to −20 V) to fully deplete the epitaxial layer of the entire pixel. In Mini-MALTA, the sensor structure has been modified by adding a gap in the low dose n-layer through a mask change or by including an additional deep p-type implant. The purpose of these modifications is to improve the charge collection at the pixel edges and corners through the creation of a stronger lateral field, which focuses the ionization charge towards the collection electrode.

The threshold achieved in the early prototypes (TJ-Monopix1 and MALTA) were of the order of 350 e− (600 e−) before (after) irradiation (to $1 \times 10^{15}$ n\textsubscript{eq}/cm\textsuperscript{2}). The noise level before (after) irradiation was determined to be around 15 e− (25 e−). The hit detection efficiency before irradiation was about 97% but dropped to 70% after irradiation. This was due to a pattern of inefficient regions on the chip. A subsequent iteration of the small electrode DMAPS (Mini-MALTA) improved the performance after irradiation by implementing enlarged transistors. This modification lead to smaller operational thresholds (200 e− versus 350 e−) and thus to better hit detection efficiency. After $1 \times 10^{15}$ n\textsubscript{eq}/cm\textsuperscript{2} neutron irradiation efficiencies of up to 98% were obtained. Thus, the usage of enlarged transistors clearly increases efficiency after irradiation due to the higher gain, lower gain spread and reduced noise.

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**Figure 2. Cross section of the TowerJazz 180 nm process. The collection electrode is indicated in the upper center of the figure.**
4. CONCLUSIONS

The WP6 activities were initially aimed to develop hybrid HV/HR CMOS sensors. To this end, test structures were used to fine-tune the AC coupling process. AC coupled devices based on the different CMOS prototypes (H35Demo and LFCPIX) and the FE-I4 ASIC were successfully produced and tested. Considerable progress in addressing the complications of the fabrication process was done, in particular:

- The difficulty in obtaining uniform capacitive coupling between substrates was overcome with the use of pillars
- The problems with electroless UBM that resulted in shorts in the wire-bonds pads were solved with protective tape

However, the focus of the WP6 activities changed from AC coupled to monolithic devices (where no hybridization step is needed). At the time of the preparation of the AIDA-2020 proposal, the AC coupling hybridization technique for CMOS sensors was thought to be the best approach to produce CMOS devices. The progress made during the first period of the WP6 activities demonstrated that monolithic devices with moderate radiation hardness were possible and that they were the most attractive (and cost-effective) option for this technology.

Depleted monolithic CMOS sensors (DMAPS) have been designed and fabricated using two different approaches. The characterization of their performance is briefly described in this report, and further details can be found in reference [10]. In both types of devices, the electronic elements are integrated directly in the sensor substrate, embedded and shielded by multiple deep well implants. The two approaches are distinguished by the way the electronics is implemented. The first variant is called the large-electrode sensor in which the electronics is completely embedded in a large deep n-well that at the same time acts as a charge collection electrode. This “large electrode design” is realized in several technologies, like LFoundry 150 nm and in AMS 180nm. The second variant has a small charge-collecting electrode set spatially aside from the electronics. This “small electrode” design was realized, for example, at TowerJazz and LFoundry. The radiation tolerance assessment of both variants, in terms of noise, timing performance and hit reconstruction efficiency showed that, in both cases, good performance of the designs after $1 \times 10^{15}$ 1 MeV $n_{eq}$/cm$^2$ neutron irradiation can be achieved. The large electrode design has been explored further, up to $2 \times 10^{15}$ $n_{eq}$/cm$^2$, and the preliminary results indicate that a good hit reconstruction efficiency is maintained at this fluence. Thus, if the ultimate goal is radiation hardness, the large electrode approach is probably marginally better based on current results. On the other hand, the small electrode design is less demanding in terms of power. Also, the latest results indicate that radiation hardness up to the level of $1 \times 10^{15}$ $n_{eq}$/cm$^2$ can be obtained. Thus, the small electrode design, with the lower power dissipation, can be a favorable approach in moderate radiation hardness environments.

As a result of the HV/HR CMOS WP activities, critical progress was made in the understanding of the technology and its applications, which indubitably place the technology as the default for moderate radiation hardness requirements in future experiments. In fact, several future experiments (specially lepton colliders) are considering depleted monolithic sensors as their baseline, as for example, the CECP [11] and ILC [12]. This highlights the success of the activities carried out in this work package.
5. REFERENCES