Electronics Performance of the ATLAS New Small Wheel Micromegas Wedges at CERN

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ABSTRACT: A series of upgrades are planned for the LHC accelerator to increase its instantaneous luminosity to $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The luminosity increase drastically impacts the ATLAS trigger and readout data rates. The present ATLAS small wheel muon detector will be replaced with a New Small Wheel (NSW) detector which is expected to be installed in the ATLAS underground cavern by the end of the Long Shutdown 2 of the LHC. With the final micromegas (MM) quadruplets (modules) already produced the activities concerning the integration of the modules into the final, fully equipped MM wedges, that will then be installed on the wheel structure on surface, are currently in full swing at CERN. One crucial part of the integration procedure concerns the installation, testing and validation of the on-detector electronics and readout chain for a very large system with more than 2.1 M electronic channels in total. These include ~4K MM Front-End Boards (MMFE8), custom printed circuit boards each one housing eight 64-channel VMM Application Specific Integrated Circuits (ASICs) that interface with the ATLAS Trigger and Data Acquisition (TDAQ) system through ~1K data-driver cards (ADDC & L1DDC, respectively). The readout chain is based on optical link technology (GigaBit Transceiver links) connecting the back-end to the front-end electronics via the Front-End Link eXchange (FELIX), a newly developed system that will serve as the next generation readout driver for ATLAS. Experience and performance results from the first large-scale electronics integration tests performed at CERN on final MM wedges, including system validation with cosmic-rays, are presented.

KEYWORDS: Micropattern gaseous detectors, Data acquisition circuits, Analogue electronic circuits, Digital electronic circuits, Front-end electronics for detector readout, Trigger concepts and systems, Radiation-hard electronics, Detector control systems, Performance of High Energy Physics Detectors

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1 ATLAS New Small Wheel

In order to efficiently handle the increased luminosity that will be provided by the High-Luminosity LHC (HL-LHC), the first station of the ATLAS [1] muon end-cap system (Small Wheel, SW) will need to be replaced. The New Small Wheel (NSW) [2] will have to operate in a high background radiation region (up to 22 kHz/cm^2) while reconstructing muon tracks with high precision as well as providing information for the Level-1 trigger. The detector technologies to be used come from the family of gaseous detectors, the first is called small-strip Thin Gap Chambers (sTGCs), and the second comes from the category of micro-pattern gas detectors and is named Micromesh Gaseous Structure (Micromegas (MM)) [7]. The new experimental layout will consist of 16 detection layers in total and 8 layers per detection technology (8 layers sTGC and 8 layers Micromegas), as shown in Figure 1. The sTGC detectors are designed to provide fast trigger and high precision muon tracking under the HL-LHC conditions. On the other hand, Micromegas detectors have a small conversion region (5 mm) and fine strip pitch (0.5 mm) resulting in excellent spatial resolution and are primarily used for precise tracking.

The NSW electronics for the trigger and Data Acquisition (DAQ) path of both detectors can be divided into two major categories, on-detector and off-detector electronics, as shown in Figure 2. The NSW MM on-detector electronics (Front-End boards (MMFE8) [4], Level-1 Data Driver Card (L1DDC) [3], ART (Address in Real Time) Data Driver Card (ADDC)) [5] will be placed inside the cavern (detector area with radiation and magnetic fields) and consists of custom-made boards mainly using radiation-tolerant Application Specific Integrated Circuits (ASICs). The communication between these boards will be established with the use of mini Serial Attached Small Computer System Interface (SCSI) cables. The off-detector electronics (Front End LInk eXchange (FELIX), trigger processor, sector logic and services running on commercial server computers like Read Out Drivers (ROD), Detector Control System (DCS), event monitoring, configuration, trigger monitor and calibration) will be placed outside the cavern in an area that is called USA15.

Figure 1. A graphic representation of the NSW sector (left) which consists of 8 layers of Micromegas in the inner part and sandwiched by 4+4 layers of sTGC detectors in the outer parts and view of the NSW (right) with 16 sectors in total.

Figure 2. Overview of the NSW electronics scheme. The front-end detector boards are depicted on the left (for MM and sTGC), the data-driver cards (L1DDC, ADDC) in the middle while the back-end electronics can be seen on the right.

2 Micromegas

A single Micromegas is a position-sensitive gaseous detector with planar parallel electrodes and consists of three planes: the cathode, the anode and the micromesh, as shown in Figure 3. The mesh divides the gas volume between the anode (readout) and the cathode (drift) into two areas: the conversion/drift gap of 5 mm where the incident muon ionizes the gas molecules and creates primary electrons, and the amplification gap of 128 μm where electron avalanches occur. The anode plane is based on printed circuit boards (PCBs), with photo-lithographically etched copper strips and a layer of resistive strips on a kapton foil glued on the copper strips for the discharge protection. The resistive strips have a resistivity of 10 to 20 $\text{M}\Omega/\text{cm}$. The readout strips have a pitch of 450 μm .

The mesh is supported by 128 μm high pillars, which guarantee the uniformity of the amplification gap. The cathode is also a PCB having a copper surface. The resistive-strip Micromegas used in the upgrade of New Small Wheel features excellent spatial resolution ($\sigma < 100 \mu\text{m}$) irrespectively of the particle incidence angle, high detection efficiency even at the highest background rates, and good two-track separation. The very thin segmentation of the MM readouts (readout-strips), together with sufficiently good time resolution, can also be exploited to complement the TGC trigger system, adding to system stability and verification even as backups.

Figure 3. The schematic of the Micromegas detector divided into two regions, the conversion/drift gap and the amplification gap.

2.1 Electronics

A Micromegas double-wedge or sector combines 128 MMFE8, 16 ADDC, 16 L1DDC boards and 16 Low Voltage Distributor (LVDB) boards, as shown in Figure 4. The MMFE8 is the front-end board which collects all the analog and trigger signals for the readout strips and houses the VMM [6] and Read-Out Controller (ROC) [10] chips. These muon-related-pulse data (charge and time measurements) are calculated by the chip within 200 ns and stored in its Level-0 (L0) buffers, to be selected by another electronic device at a later stage, namely, the ROC ASIC. The ROC is responsible for receiving the Level-0 Accept (LOA) signal from the back-end electronics of the ATLAS trigger and then forwarding this signal to the VMM. The L1DDC is the interface between multiple FE boards and the FELIX network interface. This is achieved using the high-speed serializer/deserializer GigaBit TransceiverX (GBTX) ASIC developed at CERN. The GBTX is a radiation-tolerant ASIC fabricated using the IBM/GlobalFoundries 130 nm CMOS technology. The GBTX is capable of multiplexing a number of serial links (E-Links) to a single fiber. L1DDC provides also the clock and BC Reset (BCR) signals to the ADDC board. The ADDC receives the ART data (the address of the earliest strip) from 64 VMMs (eight MMFE8s). A priority-based hit selection is implemented in real time, and the selected data is sent to trigger processors. The LVDB provides low voltage power to MMFE8, L1DDC and ADDC boards.

Figure 4. Overview of the Micromegas electronics boards and their location on the Micromegas sector.

2.2 Wedge electronics integration

The electronics integration of the Micromegas wedges takes place at CERN prior to the installation of the Micromegas sector on the NSW. The electronics integration is divided into three steps. The first step is the board and detector preparation and the cable testing, which includes the FEB standoff, grounding interconnections, cooling pad and zebra holders installation, and the cable integrity testing. The second step is the FEB integration and cabling, which includes the installation of FEBs and cabling and small-scale readout tests to validate board connectivity and noise. The third and final step is the sector readout test, which includes the electronics validation by the configuration and readout of the full Micromegas sector via High Voltage (HV) pulsing, VMM internal pulsing and cosmic rays.

3 Electronics performance

3.1 Configuration path

For the configuration path, the various Micromegas boards are supplied with the GBT-SCA ASIC (Giga-Bit Transceiver - Slow Control Adapter) [8] which is part of the Gigabit Transceiver Link (GBT) chipset [9] and its purpose is to distribute control and monitoring signals to the front-end electronics embedded in the detectors. Also, the SCA provides a number of user-configurable electrical interface ports, able to perform concurrently at transfer operations. The user interface ports are: 1 SPI master, 16 independent I²C masters, 1 JTAG master and 32 general-purpose IO signals with individual programmable direction and interrupt generation functionality. It also includes 31 analog inputs multiplexed to a 12-bit Analog-to-Digital Converter (ADC) featuring offset calibration and gain correction as well as four analog output ports controlled by four independent 8-bit Digital-to-Analog Converter (DAC).

The Micromegas electronics system is using the SCA chipset for three different applications:

- **Monitoring:** Perform the front-end monitoring of the various power and temperature sensors directly connected to the ADC channel of the SCA. The monitoring application is shown in the right part of Figure 5.
- **Configuration:** Perform the configuration of the ASIC chipsets which are placed on front-end boards using the SCA SPI and I²C masters.
- **Calibration:** Perform the VMM calibration using an ADC channel of the SCA. The calibration procedure output plot of a MMFE8 can be seen in Figure 5.

Figure 5. A typical plot produced during the VMM calibration procedure (left) and the Graphical User Interface (GUI) which is used for the monitoring of various power/temperature sensors (right).

An overview of the configuration/calibration/monitoring path is shown in Figure 6.

Figure 6. Overview of the calibration/configuration/monitor path.

3.2 Readout path

The main components of the readout path are the VMM and the ROC chipset. The VMM consists of 64 discrete channels and each channel connects to one Micromegas readout strip and performs charge amplification, discrimination and precise amplitude and timing measurements through ADCs. The VMM can provide a precise amplitude measurement of the input pulse encoded in a 10-bit word (PDO) and a precise timing estimation of the pulse's peak encoded in an 8-bit word (TDO). Shared among channels are the bias circuits, a temperature sensor, a test pulse generator, two 10-bit DACs for adjusting the thresholds and test pulse amplitudes, a mixed signal multiplexer, the control logic and the ART which consists of dedicated digital outputs (flag and address) for the earliest above-threshold channel. The peak detector measures the peak amplitude and stores it in an analogue memory. The time detector measures the peak timing using time-to-amplitude converter (TAC). The data from up to eight VMMs are passed to the ROC ASIC that merges hits from the VMMs, re-formats the data, adds headers and interfaces with the L1DDC. The data from the ROC are received by a GBT in L1DDC and sent via fiber to a general purpose network with a high-availability interface, called FELIX, as shown in Figure 7. In the last step, the data which are available through FELIX and the general purpose network are collected through Software ReadOut Driver (SW ROD) applications and are packed up into architecture-defined ROOT [11] files.

Figure 7. Overview of the readout path.

Initially, the first step of the readout path validation is the determination of the noisy and dead readout channels per MMFE8 using VMM internal pulser mode, as shown in Figure 8. Boards with more than 5% noisy channels are replaced and noisy/dead lists per board are produced in order to proceed with the cosmic-ray data acquisition. The final step of the MM sector validation is performed with cosmic rays. The trigger is provided by scintillators at 100 Hz with full coverage along the precision coordinate covering partially the detector. For the Micromegas sector operation the nominal HV and gas settings are applied, +570 V for the strip channels, −300 V for the drift channels and the gas is Ar(93%) + CO₂(7%).

Next, the data analysis of the muons which are produced by cosmic rays takes place. The analysis is focused on basic detector parameters like charge, cluster size, time distributions. The muon track reconstruction is performed analyzing the data collected in the eight layers of the Micromegas

Figure 8. During the readout path validation, a mapping list of the alive (left) and noisy (right) channels per MMFE8 is produced using the VMM internal pulser.

sector. The measured tracking efficiency is mostly defined by the chamber parameters (HV, gas etc.) but can also be used for validating the electronics complementary to the other tests, as shown in Figure 9.

Figure 9. An example plot of muon tracking (left) and tracking efficiency per Micromegas sector layer (right) in a cosmic-ray run. The blue color on the efficiency plot indicates a low efficiency region due to the HV section instabilities during the cosmic-ray run.

3.3 Trigger path

The ART signals from the VMM are driven to the ADDC that connects with up to eight MMFE8s (thus, 64 VMMs). The ART ASIC on the ADDC deserializes the ART addresses from several VMMs, appends a 5-bit VMM geographical address and a BCID timestamp. It then forms and forwards a data packet to the MM Trigger Processor (TP) through optical fiber. A priority based hit selection is implemented in real time, and the selected data is sent to trigger processors. The basic idea for the ADDC is to use two customized ART ASICs to deserialize and align the 64 channels of ART data (32 channels for each ART) and complete the hit selection processing. After the hit selection processing is finished, the selected data from each ART ASIC are sent to one corresponding GBTX and then two fiber cables are used to transmit the data from the two GBTX chips to the MM trigger processor. An overview of the trigger path is shown in Figure 10.

The test objective of the trigger path validation is the confirmation of the electrical and optical

Figure 10. Overview of the trigger path.

connectivity by sending test pulses to all VMMs of a double wedge and reading out the ART data from the TP. An ART test run of a double-wedge where all VMM channels are pulsed sequentially and produce a map of the ARTs that are readout out on the TP (10 pulses sent to 3 different channels on each VMM) is shown in Figure 11. Ideally each bin content would be 30. No bins with 0 content lead to sign-off on electrical and optical connectivity of the chamber. A few low efficiency spots that can be seen in Figure 11 are attributed to dead VMM channels that had not been masked out.

Figure 11. Automated ART test plot produced during trigger path validation. All VMM channels are pulsed sequentially and produce a map of the ARTs that are read out in the TP.

4 Conclusions

The New Small Wheel is a fully redundant trigger and tracking detector system, adequately supported by an advanced electronics scheme and ready to handle the challenges of increased instantaneous luminosity at the HL-LHC. The NSW precision tracking and trigger detectors are able to work at high rates and will provide trigger and tracking primitives fully compliant with the HL-LHC rates. The electronics is designed to provide sufficient bandwidth even at a readout rate of 1 MHz for data acquisition and trigger paths, as well as low latency for the latter. The electronics performance of

the Micromegas sector has been studied during sector integration and commissioning at CERN and tests prove that the design goals are achievable.

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References

- [1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* 3 (2008) S08003.
- [2] ATLAS Collaboration, *New Small Wheel Technical Design Report*, CERN-LHCC-2013-006, ATLAS-TDR-020, <https://cds.cern.ch/record/1552862>
- [3] P. Gkoutoumis, *Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade Compatible with the Phase II 1 MHz Readout Scheme*, ATL-MUON-PROC-2016-010, <https://cds.cern.ch/record/2235344>
- [4] P. Gkoutoumis, *Electronics Design and System Integration of the ATLAS New Small Wheels*, ATL-MUON-PROC-2016-012, <https://cds.cern.ch/record/2235777>
- [5] L. Yao et al. , *The address in real time data driver card for the MicroMegas detector of the ATLAS muon upgrade*, *JINST* 12 (2017) C01047.
- [6] G. Iakovidis, V. Polychronakos, G. de Geronimo, *VMM - An ASIC for Micropattern Detectors*, ATL-MUON-PROC-2015-015, <https://cds.cern.ch/record/2104297>
- [7] T. Alexopoulos et al , *Performance studies of resistive-strip bulk micromegas detectors in view of the ATLAS New Small Wheel upgrade*, *Nucl. Instrum. Meth. A* 937 (2019) 125.
- [8] A. Caratell et al. , *The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments*, *JINST* 10 (2015) C03034.
- [9] P. Moreira, A. Marchioro, K. Kloukinas, *The GBT : a Proposed Architecture for Multi-Gb/s Data Transmission in High Energy Physics*, CERN-2007-007, <https://cds.cern.ch/record/1091474>
- [10] R. M. Coliban et al. , *The Read Out Controller for the ATLAS New Small Wheel*, ATL-MUON-PROC-2015-011, <https://cds.cern.ch/record/2102192>
- [11] I. Antcheva et al. , *ROOT – A C++ framework for petabyte data storage, statistical analysis and visualization*, *Comput. Phys. Commun.* 180 (2009) 2499.