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Development of the ATLAS Liquid Argon (LAr) Calorimeter Readout Electronics for the HL-LHC

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ABSTRACT: To meet new trigger and data acquisition (TDAQ) buffering requirements and withstand the high expected radiation doses at the High-Luminosity LHC, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded. The triangular calorimeter signals are amplified and shaped by analog electronics over a dynamic range of 16 bits, with low noise and excellent linearity. Developments of low-power preamplifiers and shapers in the 130 nm CMOS technology are ongoing to meet these requirements. In order to digitize the analog signals on two gains after shaping, a radiation-hard, low-power 40 MHz 14-bit Analog-to-Digital Converter (ADC) is developed using a pipeline + Successive Approximation Register (SAR) architecture in the 65 nm CMOS technology. Characterization of the prototypes of the front-end components show good promise to fulfill all the requirements. The signals will be sent at 40 MHz to the off detector electronics, where Field-Programmable Gate Arrays (FPGAs) connected through high-speed links will perform energy and time reconstruction through the application of corrections and digital filtering. Reduced data will be sent with low latency to the first level trigger, while the full data will be buffered until the reception of trigger accept signals. The data-processing, control and timing functions will be realized by dedicated boards connected through Advanced Telecommunications Computing Architecture (ATCA) crates.

KEYWORDS: Calorimeters, Front-end electronics for detector readout, Data acquisition concepts

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1 Introduction

The High-Luminosity Large Hadron Collider (HL-LHC) is planned to start operation in 2027. Its objective is to increase the luminosity by factor of up to 7.5 relative to the LHC design value, reaching $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The integrated luminosity is expected to be $3000 - 4000 \text{ fb}^{-1}$ at the end of the HL-LHC operation. The average number of interactions per bunch crossing (pile-up) is expected to be $140 - 200$.

These challenging conditions require substantial upgrade of the trigger and data acquisition (TDAQ) system of the ATLAS experiment [1]. The proposed TDAQ upgrade [2] imposes strong requirements on the detector electronics. In the baseline TDAQ configuration the detector electronics should be capable of processing a trigger rate of 1 MHz with a latency of $10 \mu\text{s}$. Electronics for further evolved dual-level TDAQ configuration should be capable of processing a Level-0 (Level-1) trigger rate of 4 MHz (800 kHz) with a latency of $10 \mu\text{s}$ ($35 \mu\text{s}$).

The current Liquid Argon (LAr) Calorimeter electronics does not match these TDAQ requirements and must be upgraded. Other reasons for upgrade are radiation tolerance (the current electronics is qualified only for 1000 fb^{-1} of integrated luminosity) and electronics aging (at the end of HL-LHC operation the current electronics will be 30 years old).

The following sections contain details about different electronics modules currently being developed for the LAr upgrade.

2 Road map of the upgrade

The LAr electronics upgrade is divided in two phases [3, 4] and has a free-running scheme in which all calorimeter data are digitized on detector at a rate of 40 MHz (the bunch-crossing frequency) and sent off detector with low latency for further processing, see figure 1.

Figure 1. Liquid argon calorimeter electronics for HL-LHC [4]. Copyright 2020 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

The Phase-I upgrade (to be finished early 2021) aims to provide higher granularity LAr data for the LAr trigger. This extended LAr information will be used in Run 3 of the LHC operation starting at that time. The LAr Trigger Digitizer Board (LTDB) located on detector and the LAr Digital Processing System (LDPS) located off detector need to be developed and installed during the Phase-I upgrade. The mass production and commissioning of this electronics is ongoing now.

During the Phase-II upgrade all other electronics modules (see blocks marked with blue squares in figure 1) needed for HL-LHC will be developed and installed.

3 Phase-II front-end electronics upgrade

The front-end electronics for Phase-II consists of the Front-End Board (FEB2) and the calibration board.

3.1 FEB2

Most functions of the LAr front-end electronics will be performed in 1524 FEB2 boards, each with 128 channels. The functions of the FEB2 board are:

- LAr counter signal amplification and shaping with 2 gains to get a high dynamic range for digital signal processing;
- digitization;
- serialization and transmission to back-end;
- feeding LTDBs with sum signals.

The FEB2 board is controlled with an optical lpGBT interface.

The channel density, power and radiation requirements impose the development of specialized Application Specific Integrated Circuits (ASICs) for these tasks.

3.1.1 Analog processing

Two ASICs (ALFE1 and LAUROC2) are being developed for analog processing on detector with the same set of features:

- tunable input impedance;
- preamplification;
- signal shaping with tunable shaping time and 2 output gains;
- control by serial interface.

Both chip designs are based on CMOS 130 nm technology. The first prototypes of both chips (ALFE0 and LAUROC1) were tested and showed excellent performance in terms of Integral Non-Linearity (INL) and Equivalent Input Noise (EIN). There was no visible degradation in operation after irradiation with a total ionizing dose (TID) up to several times the required dose.

The LAUROC2 chip has a modification called HPS in which the preamplifier is replaced with a pre-shaper and an inverter to process signals from the hadronic endcap (HEC) part of the calorimeter where the first stage of amplifying electronics is located in the calorimeter cryostat.

The decision on which design will be used is to be made after getting the prototypes test results.

3.1.2 Digitization

A special chip is being developed to meet the requirements for digitization in the FEB2 board:

- convert 2 gains $\times$ 4 channels with a 14 bit dynamic range;
- 40 MHz sample rate;
- effective number of bits (ENOB) > 11 ;
- radiation tolerance.

Its latest version (v.3) based on CMOS 65 nm technology was manufactured and is under tests now. Two options were implemented to get 14 bit ADC resolutions:

- 12 bit successive approximation register (SAR) ADC + dynamic range extender (DRE);
- 12 bit SAR ADC + multiplying DAC (MDAC).

The ENOB for the second option showed excellent performance — 11.7 bits.

Another option for digitization is the use of an ADC IP designed for CMS electronics upgrade. This IP has only 12 bit resolution but with a 160 MSPS (Mega-Samples Per Second) sample rate that is 4 times higher than required. Processing this data digitally later may allow to get satisfactory results for the calculated energy.

3.1.3 FEB2 board prototype

As working samples of the ASICs became available, the FEB2 board prototypes are being developed to confirm the overall design functionality. The version 2 of the FEB2 prototype called Slice test board will be ready in 2020. It contains 32 channels and will be used to demonstrate the multi-channel performance, operation of output data and control links. The radiation tolerant power components will be also checked with this prototype for compliance with requirements.

It is expected to get a full size FEB2 board prototype in 2021–2022.

3.2 Calibration board

The goal to calibrate the calorimeter is to be achieved with 130 calibration boards located on detector. The calibration board should generate a triangle-shaped pulse with a short rise time (< 1 ns) to emulate the response of the LAr cell (calorimeter channel). The other requirements are:

- integral non-linearity $< 1\%$;
- uniformity better than 0.25% ;
- radiation-tolerance up to 180 kRad;
- 16 bit dynamic range.

A special ASIC called CLAROC (Calibration of Liquid ARgon Output Chip) is being developed for this task. It is designed with HV-CMOS 180 nm technology and contains a 13 bit DAC with 3 bit current mirrors to control the amplitude of the output signal with an effective 16 bit resolution. The output current pulse is generated with a high frequency switch. This pulse terminated on R+L load forms a voltage pulse similar to the LAr cell response.

The latest version (v.2) of this chip was manufactured and tested. Good performance of the high frequency current switch was confirmed. No problems with radiation were observed. However the measured INL $\sim 0.3\%$ is higher than requirement of 0.1% . The origin was identified as DAC high bits and will be addressed in v.3 of the chip.

The concept design of the full-size calibration board with 32 CLAROC chips (128 calibration channels) has started. The prototype board is expected to be ready in the end of 2020 or beginning of 2021.

4 Phase-II back-end electronics upgrade

The main tasks of the Phase-II back-end electronics are:

- to control the front-end electronics and to provide it with timing information — to be performed by the LAr Timing System (LATS);
- to process digitally the LAr counter signals, to buffer results if needed and to provide ATLAS TDAQ and Trigger systems with needed LAr data – to be performed by the LAr Signal Processor system (LASP).

4.1 LATS

A special board called LATOURNETT (LAr Timing trigger cOntrol distribUtion and fRoNt End moniToring/configuraTion) is being developed for the task to distribute Trigger, Timing and Control (TTC) signals from the Central Trigger Processor to all LAr FEB2 and calibration boards. Essentially, it is a board with a matrix of FPGAs that form the required distribution tree. This project is in its early stage now, and the total number of boards to be manufactured and installed depends on how many FPGAs and optical transceivers can be placed on a single ATCA blade.

4.2 LASP

The tasks of digital processing of signals coming from the FEB2 boards are to be performed in the LASP system. The LASP system is a farm of electronic board pairs — main ATCA board (blade) and SRTM (Smart RTM) board working in tandem. These tasks are:

- gain selection;
- precise measurement of the energy and signal time of each calorimeter cell;
- identification of the correct bunch crossing;
- correction of baseline: active signal filter or time-dependent average correction;
- trigger input preparation: energy sums, energy ordering, filtering with noise threshold.

The LASP main board will include 1 or 2 high performance FPGAs where this processing will be performed. The exact number of FPGAs depends on whether the design with 2 FPGAs fulfills power/cooling requirements of the ATCA specification limits.

The diagram of the LASP main board firmware is shown in figure 2. It has a trigger path (ialign, remap, dacore, packer) for which the maximum latency constraint should be met. It has buffering logic (buffs blocks) to store processed data until they are sent to FELIX (the ATLAS DAQ farm) or read out by the data monitoring system. The firmware also has a pattern generator logic (patgen) that emulates data coming from FEB2 boards for debugging and commissioning purposes.

The LASP FPGA input data bandwidth from 4 FEB2 boards exceeds 880 Gbps (22 links running at 10.24 Gbps). The set of output data streams depends highly on the calorimeter region that is served by the specific LASP board, but the total output data bandwidth is of similar order.

Figure 2. LASP firmware design. Copyright 2020 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

The first LASP testboard is in the final stage of development. It has 2 Intel Stratix-10 FPGAs with all input and output interfaces implemented. Power distribution, power-up control, serial link connections, DDR4 connections were some of the challenges faced during design. The testboard is expected to be manufactured and fully mounted in the end of 2020.

The LASP main board firmware is also being developed now with the possibility to evaluate its feasibility on Stratix-10 development kits.

The LASP SRTM board extends connectivity of the LASP main board and monitors data processing there, using Xilinx Zynq Ultrascale+ SoC to perform these functions. The SRTM hardware design is almost ready and SRTM testboards are expected to be manufactured and delivered in July 2020. Currently the SRTM firmware and hardware tests are carried out with the Xilinx ZCU111 evaluation kit.

5 Summary

New TDAQ requirements and high radiation levels at the HL-LHC necessitate the upgrade of the LAr calorimeter electronics. The upgrade needs a number of boards with new ASICs and high

performance FPGA-based processing boards to be developed. This development is going smoothly and is expected to be finished and tested before the start of the HL-LHC operation.

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