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Tracking Detector**

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Invited paper presented by B. Foster,
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Second Level Trigger for the SDC Silicon Tracking Detector

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Abstract

The design of the second level trigger for the inner silicon tracking detector of the SDC experiment at the Superconducting Super Collider (SSC) is outlined. The main purpose of the trigger is to recognise with high efficiency high transverse momentum tracks in both the barrel and end-cap. By means of a two-stage analysis it is possible to measure track momentum with the full precision of the silicon tracker. An outline of a possible hardware implementation is presented.

1 Introduction

The SDC detector [1, 2] had 4π electromagnetic and hadronic calorimetry surrounding a solenoid producing a uniform 2 T field over the tracking volume. Outside the calorimetry was a toroidal magnet system for muon detection, also covering most of 4π . The tracking system was intended to reconstruct and measure the momentum of all tracks with a pseudorapidity, η , less than 2.5 units. The silicon detector layout [3] used in the work presented here consisted of a “barrel” region of eight layers of silicon strip detectors extending up to 1.5 units in η , as well as two “end caps”, extending out to an η of 2.5. The silicon detectors were double sided, with a small stereo angle between the strips on opposite sides. There were a total of approximately 6.5×10^6 electronic channels in the detector.

The SDC trigger architecture consisted of three levels of triggering [4]. The time between bunch crossings at the SSC was 16 ns so the first level trigger was pipelined. The number of channels of the silicon tracker was so large that it was impractical to read it out in time to be used as input to the first level trigger and therefore was used for the first time at the second level. This trigger was designed to cope with an input rate of between 10 and 100 kHz and to give a rejection factor of between 10 and 100 with a variable latency whose maximum would probably have been larger than $100 \mu\text{s}$ ¹. The third level trigger would have been microprocessor based and have reduced the output rate to be recorded to between 10 and 100 Hz.

2 Second Level Trigger - General Principles

The primary design goal of the silicon SLT (SiSLT) was to reconstruct with high efficiency high transverse momentum charged particles with a resolution of approximately $\sigma(p_T)/p_T = 5(\text{TeV}/c)^{-1} \times p_T$. To match to the calorimeter and the other detectors participating in the SLT, the SiSLT had granularity of 1024 in ϕ . The barrel region was divided into 5 regions of η and a similar division was under study for the end-caps. The SiSLT was also required to address a number of secondary goals. Most important among these was to recognise candidates for photon conversion to e^+e^- pairs occurring within the volume of the silicon tracker. Such conversions formed the main background to the inclusive electron trigger at the first level. It was also intended to use the trigger to tag heavy quark decay by detecting tracks not originating from the main vertex. Finally, some preliminary design work was carried out to combine the silicon tracker hits with other tracking detectors to form a preprocessor for the global second level trigger processor. Due to limitations of space these topics are not discussed further in this paper.

The input to the SiSLT was tables of hit positions in a two-dimensional space. In the case of the barrel silicon modules these were the radial distance of the silicon layer

¹The maximum size of the level 2 latency was under active discussion at the time of the cancellation of the SSC project.

from the origin and the azimuthal angle ϕ . In such a table high transverse momentum tracks have a very small variation in ϕ as a function of radius whereas low p_T tracks bend considerably. Typical resultant patterns from low and high p_T tracks are shown in figure 1. The pattern of hits produced in the table can be recognised and used to estimate the transverse momentum of the track.

In addition to recognising high transverse momentum tracks, the SiSLT must also measure their p_T . In many ways these two functions are distinct, and favour splitting the trigger into two parts. The first, known as the “coarse” trigger, concentrates on finding tracks whose p_T is greater than some variable threshold. The necessarily coarse measurement and crude pattern recognition implied in this first stage can then be improved by a second stage of processing, known as the “fine scan”. Here the areas selected by the coarse scan are examined with the full granularity to improve the pattern recognition and measure the transverse momentum with the required resolution.

Most of the simulations and results presented in this paper are concerned with the barrel region. Nevertheless, similar processors can be used for the end-cap modules, except that a table of ϕ against z , the distance along the beam line, is employed.

The simulations which form the basis of the design work reported here were carried out in the framework of the SDCSIM Monte Carlo [5], based on GEANT 3.15 [6] and therefore incorporating a realistic treatment of multiple scattering, interactions, conversions etc. Several event generators were used [7, 8, 9, 10]. The simulation of the trigger algorithm was carried out assuming an idealised geometry in which, in the barrel, strips were assumed to be laid out along the surface of a cylinder, rather than as elements of rectangular silicon wafers fixed to a cylindrical support structure. It was assumed that the efficiency to produce a hit in a silicon detector after the passage of a charged particle was 99 %.

3 The Coarse Scan Algorithm

On receipt of a first level trigger, data from the silicon tracker in the form of a list of hit strip numbers is multiplexed up to the trigger processors on optical fibres[11]. The essence of the pattern recognition problem is to detect straight lines in the $r - \phi$ two dimensional hit map, as shown in figure 1. The turn-on of the trigger algorithm will be a function of the width of the region in ϕ which is integrated over and the minimum number of hits required to define a candidate. The results shown in figure 2 show the variation in efficiency as a function of the minimum number of hits required to produce a track candidate, and for 2 different bins in ϕ . Hits are counted in a “window” of two vertical ϕ columns. On the assumption derived from studies of the first level trigger that high efficiency for charged tracks was required for a p_T greater than 10 GeV/c , the optimum choice for the coarse scan algorithm appears to be to use 2048 ϕ bins and a minimum requirement of 5 or 6 hits. This gives a track finding efficiency in excess of 95% for $p_T > 15 GeV/c$. Figure 3 shows results from a very

similar algorithm applied to the end-cap region of the silicon tracking detector.

4 The Fine Scan Algorithms

Once the coarse scan outlined above has identified regions likely to contain the high p_T tracks of interest, the hits in this region are transmitted to a further stage of processing, known as the “Fine Scan”. Here the pattern recognition problem is much more difficult because it is necessary to use the full resolution of the detector in order to produce the best possible transverse momentum measurement. This means that the number of possible patterns of hits produced by tracks with p_T ranging from 10 GeV/c to the maximum possible value is very large. In this situation the use of programmable microprocessors becomes competitive with more specialised pattern recognition hardware. The type of algorithm used in these two cases is very different.

4.1 Microprocessor Algorithm

There are many methods to estimate the transverse momentum of a charged track. We have investigated a particularly simple one, likely to be viable within the required latency for a microprocessor available today. It is based on the assumption that the hit pattern of a high p_T track does not differ greatly from a straight line. To first approximation the p_T will be inversely proportional to the residuals of the hits compared to the expectation for a straight track. Two quantities are calculated by the algorithm; the residual and slope:

$$R = \frac{1}{n} \left(\sum_{i=1}^8 s_i^2 - \frac{(\sum_{i=1}^8 s_i r_i)^2}{\sum_{i=1}^8 r_i^2} \right); \quad S = \frac{\sum_{i=1}^8 s_i r_i}{\sum_{i=1}^8 r_i^2} \quad (1)$$

The definitions of the quantities s_i and r_i are illustrated in figure 4 and n is the number of hits used in the calculation. The value of p_T can be calculated from either of the two relations:

$$p_T \sim \left(\frac{a}{R} \right)^b; \quad p_T \sim \left(\frac{S}{a'} \right)^{b'} \quad (2)$$

where a, b, a', b' are constants depending on the number of points on the track.

Figure 5 shows the efficiency as a function of three possible p_T thresholds for isolated electrons. Figure 6 shows results from multi-track events from gluon-gluon scattering producing two jets (known as “QCD jet background”). Monte Carlo studies² indicated that this type of event forms the major background after the first level trigger. Note that these efficiencies include the efficiency to be accepted by the coarse scan. The electron figure shows a sharp turn on and high efficiency for large p_T . For

²The Monte Carlo simulation includes an average of 1.6 minimum bias underlying events, as appropriate to an SSC luminosity of $10^{33} \text{ cm}^{-2} \text{ s}^{-1}$. Only those events which pass a simulation of the SDC first level trigger algorithm are considered in the SiSLT simulation.

the QCD generated background however the efficiency is much lower. In addition the rate of “fake” triggers generated by tracks whose real p_T is actually below the nominal trigger threshold runs at about 14% of all background events for a p_T threshold of 10 GeV/c , falling exponentially to less than 2% for $p_T > 20 GeV/c$. The major reason for this is the poor pattern recognition of this algorithm. Having started from a seed hit in the outermost silicon layers the algorithm looks for the nearest hit in ϕ in the next layer and then adds the hit nearest to the extrapolated position given the updated residual and slope. This algorithm is easily confused by close tracks and having once picked up a false hit tends to produce false triggers.

The p_T resolution of this trigger can be determined by fitting Gaussian line shapes to the measured p_T produced by the algorithm as a function of bins of the generated p_T . The resolution obtained for isolated muons is almost as good as the theoretical best attainable value given the granularity of the silicon strip readout. The resolution for isolated electrons is degraded by approximately a factor of three.

4.2 Road-based Algorithm

The pattern recognition problem in the fine scan is very similar to that at the coarse scan stage but requires many more roads. Each road is based on a single strip in the innermost layer of the barrel silicon detector and ends on a single strip in the outermost layer. In order to be sensitive to $p_T > 5 GeV/c$, roads ending within ± 125 strips of the strip which would be hit by an infinite momentum track are required. If every road were distinct, a total of 3×10^7 would be required. Fortunately, there is a high degree of symmetry in the problem. In the Monte Carlo simulations it is assumed that the same set of roads can be used independent of the position in the innermost layer. Moving away from this unrealistic degree of symmetry to one more likely to be useful in a real situation merely changes the amount of hardware required.

Since a given track satisfies several adjacent roads, it is necessary to take a weighted mean of the satisfied roads in order to give the best estimate of the p_T . This also implies that tracks very close in both ϕ and p_T will not be resolved. Tracks can be distinguished if the weighted means of their satisfied roads are more than about 6 roads apart, corresponding to $^{+1.3}_{-1.0} GeV/c$ for a 10 GeV/c track.

The p_T resolution of the trigger measured with isolated leptons is very similar to that of the microprocessor algorithm. However, both the rate of false triggers and the efficiency of the trigger for QCD jet events is much improved. For $p_T > 10 GeV/c$ around 5% of tracks produce a fake trigger, a rate which falls to below 2% for p_T threshold $> 15 GeV/c$. The overall efficiency for the trigger correctly to detect a high transverse momentum charged particle inside a QCD background event averages about 96%.

As well as satisfactory rejection power the algorithm also performs well with the physics processes of interest. The efficiency to detect one muon emanating from the decay of a 400 GeV/c^2 Higgs particle into 4 muons is high everywhere above threshold and averages about 99% for these very high p_T particles.

5 Outline hardware implementation

In a previous publication [11] we remarked that a solution for the coarse scan based on large memory look-up tables is both feasible and could be built with currently available technology. A better solution is provided by the Associative Memory Unit (AMU), developed by the Pisa group [12]. This device is a custom VLSI chip which is a form of *content addressable memory*. This has the advantage that only the patterns of interest, rather than all possible patterns, need to be stored.

We have assumed that AMUs holding 512 patterns are available. The minimum number of patterns was obtained by arranging them in a two stage configuration, each configured to deal with four layers of the detector, as shown in figure 7. The hit information is stored in a primary buffer and passed to the AMUs to begin the coarse scan. One array deals with layers 1,3,5 and 7 of the barrel detector, while the second deals with the remaining layers. A final bank of AMUs looks at the outputs of the even and odd AMU banks and selects the wanted patterns by combining their information. The addresses of patterns of interest are then output into a buffer memory where they are stored until completion of the coarse scan and used to gate the hits stored in the primary buffer which are of interest to the fine scan. Thirty-six processor boards, each containing eighteen AMUs, could implement the coarse scan function for the barrel silicon tracking detector. A slightly larger number of boards would be required to deal with this function for the two end-cap silicon detectors.

In the previous section we discussed two possible algorithms for the fine scan. Clearly the optimum device to implement the microprocessor algorithm is a special purpose processor with a reduced instruction set. A good choice is a Digital Signal Processor (DSP), which is both optimised for rapid execution of floating point arithmetic and widely available and competitively priced. We chose to use the Motorola DSP 56001, with which we have experience [13]. The microprocessor algorithm was coded in FORTRAN and the manufacturer's software simulator used to measure the performance of the device with the QCD jet Monte Carlo sample. The simulation assumed that four DSP wait states were required for all access to peripherals. We measured the distribution of execution time for the microprocessor algorithm based on inputting all hits from a wedge in ϕ of the silicon detector defined by 8 adjacent strips in the innermost superlayer³. Most of the events are processed within about 100 μ s. However, there is a tail extending to beyond 200 μ s. Given that DSPs are likely to improve execution speeds by a large factor in the near future it is likely that any reasonable maximum latency adopted by SDC could have been met by a DSP solution.

In order to implement the road-based algorithm, it seemed natural and advantageous to consider a solution based on AMUs. They have the advantage that their latency is smaller than the DSP. However, the number of roads required for the fine

³Note that this work was done before the details of the coarse trigger had been finalised and that therefore it does not correspond exactly to the ϕ regions provided by the coarse processing

processing is very much larger than that required for the coarse scan. This number is critically dependent on the amount of symmetry which can be assumed in the detector. Our simulation did not progress beyond this most symmetrical situation, so that we can only speculate as to the number of AMUs which might be required. The factors which influence this number include the geometrical layout of the detector, since the edges of each of the silicon wafers in the detector clearly introduce asymmetries. We are confident, that a solution would have been feasible within a system of reasonable size.

In conclusion, given the information available, it is neither possible to differentiate between the two hardware solutions presented nor to be convinced that either would necessarily have been adequate. Nevertheless, we believe it is plausible that both would in fact have been satisfactory. Although in figure 7 we show a block diagram indicating an AMU solution to the fine processing, their replacement by DSPs would be a minor change to the conceptual design.

6 Summary

We have presented ideas for a second level trigger processor for the SDC silicon tracking detector. Our Monte Carlo studies indicated that possible solutions to the problem exist. Had the US Congress permitted, we are confident that we could have built a trigger processor which would have coped with the great technical challenges and the enormous physics potential of the SSC.

Acknowledgements

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Figure 1: Schematic showing the appearance of two-dimensional tables for the second level trigger in the barrel region. The left pattern shows the expectation from a track with low transverse momentum, the right pattern one from a track with very high transverse momentum. The narrow rectangles represent the ϕ window over which the SiSLT integrates.

Figure 2: Results from the coarse trigger algorithm for isolated electrons as a function of the number of hit layers found within the window. The top figure shows the results from a window of 2 ϕ bins from a total of 1024 bins, the lower figure from 2 bins from a total of 2048.

Figure 3: Results from the coarse trigger algorithm for isolated electrons as a function of the number of hit layers found within the window for the endcap region. A total of 1024 ϕ bins was used.

Figure 4: Definition of the quantities used in the microprocessor algorithm for the fine scan.

Figure 5: Trigger efficiency for the microprocessor algorithm using isolated electrons. The solid line shows the results for a nominal threshold of $8\text{GeV}/c$, the dashed line for a threshold of $10\text{GeV}/c$, and the dotted line a threshold of $15\text{GeV}/c$.

Figure 6: Trigger efficiency for the microprocessor algorithm using "QCD 2-jet" events (see text). The solid line shows the results for a nominal threshold of $8\text{GeV}/c$, the dashed line for a threshold of $10\text{GeV}/c$, and the dotted line a threshold of $15\text{GeV}/c$.

Figure 7: Block diagram showing details of a possible implementation of the SiSLT algorithm on one of a number of 9U boards. The parts of the board dealing with the fine and coarse scans are outlined. Each board would deal with a given ϕ region of the silicon barrel detector. Interconnections would be required to deal with tracks crossing between ϕ regions.