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**BASIC CONCEPTS AND ARCHITECTURAL DETAILS OF THE DELPHI
TRIGGER SYSTEM**

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Abstract

DELPHI (Detector with Lepton, Photon and Hadron Identification) is one of the four experiments of the LEP (Large Electron Positron) collider at CERN. The detector is laid out to provide a nearly 4π coverage for charged-particle tracking, electromagnetic and hadronic calorimetry and extended particle identification.

The trigger system consists of four levels. The first two are synchronous with the BCO (Beam Cross Over) and rely on hardwired control units, while the last two are performed asynchronously with respect to the BCO and are driven by the DELPHI host computers.

The aim of this paper is to give a comprehensive global view of the trigger system architecture, presenting in detail the first two levels, their various hardware components and the latest modifications introduced to improve their performance and make the entire software user interface more user-friendly.

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1 INTRODUCTION

The DELPHI detector [1] consists of a complex set of 17 specialized subdetectors, which can be grouped into the following families: tracking (vertex detector, VTX, inner detector, ID, time projection chamber, TPC, outer detector, OD, barrel-muon chambers, BMU, forward chamber A, FCA, forward chamber B, FCB, forward-muon chambers, FMU), scintillation (time-of-flight counters, TOF, forward hodoscope, HOF), electromagnetic calorimetry (high-density projection chamber, HPC, forward electromagnetic calorimeter, FEMC, scintillator tile calorimeter, STIC, very small angle tagger, VSAT), hadron calorimetry (hadron barrel, HAB, hadron forward, HAF) and Cherenkov ring imaging (barrel-ring-imaging Cherenkov counter, BRICH, forward-ring-imaging Cherenkov counter, FRICH).

All these subdetectors, with the exclusion of the VTX, the BRICH and the FRICH, contribute to forming classes of trigger decisions [2], [3] corresponding to the two regions of the angular coverage (barrel and forward/backward) or corresponding to the physics requirements (e^+e^- , $\mu^+\mu^-$, $\pi^+\pi^-$, $\gamma\gamma$, etc.). The principal physics components forming the triggers are: track, muon, electromagnetic energy, hadronic calorimeter, luminosity.

A good trigger condition is fulfilled when a predefined minimum number of subdetectors or more have fired among those logically grouped together.

The trigger decisions are constructed as majorities of multiplicities. Each way of grouping together subdetectors defines a majority. There is a majority 1 and a majority 2, which are respectively fulfilled if at least one or two grouped subdetectors have fired. The final trigger decision is the OR condition of all the previously constructed majorities.

Multiplicity itself is a similar concept restricted to individual subdetectors. When there have been at least one or two basic trigger signals (number of tracks, shower, etc.) within a subdetector, the related multiplicity is fulfilled.

2 THE DELPHI TRIGGER SYSTEM

2.1 Overview

Since 1991 the LEP collider has been upgraded to work with eight bunches at the nominal energy of 45.625 GeV (four bunches during 1989/1991). A further upgrade could be either a higher number of bunches (12, 18) or the so-called bunch train, i.e. a train of four bunches each containing four packets of particles separated by 250 nsec.

These LEP operational modes are compatible with the architecture of the trigger system [4] which consists of four levels, usually labelled as T1, T2, T3, T4 (Fig. 1) Timing of DELPHI trigger system.

T1 and T2 are based on hardwired decisions that are fully synchronous with the BCO of the LEP machine. They represent, therefore, the real time trigger part of DELPHI.

For a typical luminosity of $15 \times 10^{30} \text{ cm}^{-2} \text{ sec}^{-1}$ and eight bunches, T1 reduces the event rate from 90kHz to about 800Hz and is built with those subdetectors that can resolve the decision before the next BCO (11.11 μsec later). Therefore, no successive events are lost and there is no degradation of the trigger efficiency. T2 accepts slower subdetector responses that complete the trigger sequence and additionally reduce the rate from 800Hz to about 4 Hz.

During the T1 and T2 trigger phases the data coming from the detectors ($DET_i \dots DET_j$) are digitized and stored in optional DIGitization Buffers (DIGB) or directly into one free buffer of the Front End Buffer (FEB) bank.

Fig. 1 Timing of Delphi trigger system

When the event is accepted, i.e. $T1 = YES$ and $T2 = YES$, the data is compacted, copied from the DIGB into one free buffer of the FEB — Front End Freeing (FEF) action — and the event pointers are updated to accept the next event — Next Event Identification Done (NEI_D) action.

The trigger sequence will then split in two parallel flows: 1) wait for the next BCO, and 2) continue with the next trigger decision phase, T3.

In the opposite case of a rejected event, i.e. $T1 = NO$ or $T2 = NO$, the event is simply ignored, the loading of the DIGB or FEB is stopped and with the following BCO these buffers are overwritten with the new data.

T3 and T4 [5] are software-driven, asynchronous with respect to the BCO and take place in two steps: during the phase in which the frontend buffers are readout (FEB readout) and in the last phase of data recording. The typical processing time for computing T3 is from 20 to 30 msec, while for T4 it is 200–500 msec. T3 reduces the event rate to about 2 Hz while T4 discards those events found to be empty and adds extra flagging information.

During the FEB readout the data of each subdetector is merged into one free buffer of the Multi Event Buffer (MEB) bank and properly labelled. T3 is performed on the data stored in the MEB. If the event is accepted, i.e. $T3 = \text{YES}$, the detector's entire data is copied into one free buffer of the Global Event Buffer (GEB) bank and the data recording phase occurs. In the opposite case, the data in the MEB is discarded.

The presence of the two previously mentioned buffers, DIGB and FEB, makes it possible to perform the FEB readout phase in parallel with the acquisition of a new event (digitization phase).

During data recording, the selected GEB is read out and its information finally processed by a farm of emulators and stored.

2.2 Trigger control signals

The real-time trigger sequence is based on handshaken signals synchronized with the BCO. The present BCO rate (eight bunches) is 90 kHz.

CLK_BCO (CLOCK_BCO) is the signal used to synchronize the whole trigger sequence. It is a 100 nsec pulse with the same frequency as the BCO and occurs about 5 μsec before the BCO. Another signal called WNG_BCO (WarNinG_BCO) starts the trigger sequence. WNG_BCO is a copy of CLK_BCO gated with a signal called FE_RDY (FrontEnd_Ready). FE_RDY is true when the whole DELPHI detector is ready to accept a new event and becomes false as soon as a new trigger sequence is initiated by WNG_BCO.

Fig. 2 a) T1_NO sequence, b) T1_YES/T2_NO sequence, c) T1_YES/T2_YES sequence, d) DIGB to FEB data transfer sequence.

Four timing signals called T1_NO, T1_YES, T2_NO and T2_YES generate three possible trigger sequences depending on the level 1 and 2 trigger results: T1_NO sequence (Fig. 2a), T1_YES/T2_NO sequence (Fig. 2b) and T1_YES/T2_YES sequence (Fig. 2c). T1_NO/YES are two mutually exclusive signals respectively carrying the bad and good first-level trigger results and occurring 3 μ sec after the BCO. T2_NO/YES are two similar signals for the second-level trigger result and occurring 39 μ sec after the BCO.

When an interaction produces a T1_YES/T2_YES sequence, the event is good for the first two trigger levels. A signal called FEF (FrontEnd Freeing) initiates the data transfer from DIGB to FEB (Fig. 2e). This phase ends with the updating of the DELPHI crate processors controllers (FIP [6], i.e. FASTBUS Intersegment Processor) to accept the next interaction. The handshake is closed by a signal called NEI_DONE (Next Event Identification_DONE) which causes the end of FEF and the enabling of FE_RDY real-time trigger hardware

2.3 Overall view on the system.

The DELPHI detector is organized in partitions. Each partition corresponds to a subdetector, to a part of it, or to a group of subdetectors. The central control logic of the trigger system is also defined as one partition (trigger partition or central partition). This configuration allows a large flexibility in the operation of the whole experiment because a particular partition can isolate itself from the central control logic and operate locally.

Figure 3 shows the general architecture of the whole DELPHI trigger system. Its hardware is based on FASTBUS [7] units.

Fig. 3 Delphi trigger system block diagram.

In the central partition two devices control the trigger decisions and the timing signals: the Trigger Supervisor Decision Box (TS_DB), also called 'Pythia', and the Trigger Supervisor Control Box (TS_CB) or 'Zeus', respectively. Similarly, in every local partition two other modules control the local trigger decisions and the local timing signals: the Local Trigger Supervisor Decision Box (LTS_DB) and the Local Trigger Supervisor Control Box (LTS_CB), the latter also called 'Pandora'.

Pythia receives the trigger information from every subdetector through the decoder box of the LTS_DBs, the only unit not built in FASTBUS standard. A set of Trigger Data lines (TDLs) connect Pythia, the decoder box, the LTS_DBs and, in addition, a set of scalers (Pythia Scalers) for monitoring purposes. Pythia, by means of a number of LUTs (LookUp Tables) that specify the logic combination of detectors forming the physics trigger, produces four input signals for Zeus. These four signals represent the two global decisions (accept or reject) corresponding to the first two trigger levels, T1 and T2.

Zeus adds timing information to the decision signals by giving them the appropriate time relation with respect to other signals, and distributes timing signals to the Pandoras of every partition through the Trigger Control Lines (TCLs). These timing signals are the previously mentioned T1_NO, T1_YES, T2_NO, and T2_YES. A number of fanout units take care of the distribution of the TCLs.

An additional task of Zeus is to disable the central trigger logic until the full DELPHI detector has been read out after a T2_YES event, i.e. the data are copied to one free buffer of the FEB bank and the event pointers have been properly updated.

The Pandoras generate local gating and clock signals (bursts or free-running, phase locked with the LEP radiofrequency) called WNGs (WarNinGs) and CLKs (CLoCKs), to be sent to the frontend digitizer modules through other fanout units (not shown in Fig. 3). Each Pandora is set up accordingly to the particular needs of its own subdetector application, i.e. their WNGs, CLKs and its mode of operation. The protocol between Pandora and Zeus is based on handshaken signals (see 2.2 and Fig. 2a, 2b and 2c) that assure the correct synchronism of the subdetectors with the machine cycle and the event type.

In case a subdetector is wanted to run independently from the central decisions, it is possible to disconnect it from Zeus and run it directly from the local Pandora. In this configuration the corresponding LTS_DB assumes the tasks of a 'local Pythia'. A status signal is sent from the local Pandora to Zeus to inform it that this partition is running in local mode.

Pythia is the closest module to the physics needs, i.e. it is through it that the type of physics is chosen. A detailed description of the use of Pythia and its related software can be found in the references [2], [3], [8] and [9]. Here, only its hardware description will be presented.

There are two Pythias: one for the generation of the T1 decision and another for the T2 one. They are identical in their hardware, but different in their software setups.

Figure 4 shows the block diagram of Pythia. It consists of four FASTBUS units: a receiver unit, two level A/B units and a level C unit. The receiver unit receives up to a maximum of 120 TDLs and fans them out four times (Fout0, Fout1, Fout2, Fout3). These TDLs can be of two types: coded or uncoded. The coded ones carry the information on multiplicities (i.e. multiplicity = 0, 1, 2, >2), while the uncoded ones represent a selfmeaningful trigger response already preprocessed by units specific to a detector — for instance Bhabha. At present, 86 TDLs are used for the T1 decision and 95 for the T2 decision.

The Level A/B unit is a cascade of two sets of LUTs.

The first set (A LUTs) consists of two identical groups of 10 LUTs, with each group taking 10 sets of 12 input signals from the 120 TDLs and generating a total of 160 output signals, CFs (Component Functions), organized in 10 sets of 16 signals. Within a group of

10 LUTs, all the output bits of the same weight 'i' ('i' = 1 to 16) are ANDed together (bit to bit AND function). Two sets of 16 signals are formed. These TFs (Term Functions) first enter into the next group of two LUTs (B LUTs) and then are independently driven at the output of the level A/B unit.

Fig. 4 Pythia block diagram.

The CFs are programmed to represent detector multiplicities (0, ≥ 1 , ≥ 2). The TFs and the B LUTs form the desired majorities. The B LUT outputs are programmed to represent the fulfilled majorities.

The level C unit receives both outputs of two level A/B units and performs again a bit to bit AND function on these four groups of 16 signals. The result Cinp (i.e. level C LUT input function) is used as input for a LUT (C LUT). The DFs (Decision Functions) are the 16 C LUT output signals. They are independently masked, prescaled and finally ORed together to form the trigger decision. At present, the level C LUT is programmed to identity, i.e. the LUT is transparent.

From the application point of view, this way of implementing the T1 and T2 trigger decisions by means of a series of LUTs gives users the best flexibility for covering any needs.

Both Pythias for the T1 and T2 decisions are housed in the same FASTBUS crate. This crate has a personalized auxiliary backplane to provide the electrical connectivity between the level A/B units and the receiver unit on one side, and the level C unit on the other.

2.4 Zeus

Zeus is the module that supervises the timing of the whole trigger system and selects the modes of operation of the full experiment. A detailed internal description of Zeus can be found in the reference [10].

Zeus consists of two FASTBUS boards connected by front panel cables: the Zeus mother and the Zeus daughter. Zeus mother responds to FASTBUS commands and controls the trigger

activity, while Zeus daughter is a dummy FASTBUS unit, only taking power from the crate, and containing all the fast electronics running at the LEP radiofrequency ($Rf \approx 352$ MHz), at $1/2$ ($Rf_2 \approx 176$ MHz) and $1/3$ ($Rf_3 \approx 117$ MHz) of it.

Figure 5 shows the main tasks of Zeus and its connectivity within the trigger system.

Fig. 5 Zeus block diagram.

The master timing signals used by Zeus are the LEP Rf and two electrostatic beam pick-up signals (LEP PICKUPS) that detect the passage of the bunches some 400 nsec before the actual interaction point. Two down-scaled frequencies (Rf_2 and Rf_3) as well as the main synchronization signals (CLK_BCO and WNG_BCO) are built from the LEP Rf.

All the FE_RDY signals of each partition come to Zeus. They are masked with a register containing the pattern of the active partitions and ANDed together to produce the internal FE_RDY signal used to start the next trigger cycle.

Every partition that wants to be active in the central acquisition must set its GBL (GloBaL) line. Zeus latches these GBL lines into the GBL register. Another register, the P (Present) register, is set by FASTBUS at the beginning of the run with the list of those partitions wanted to be active. The GBL and P register patterns are compared to check the partitions that are really active. An error is set if the two are different.

Zeus can run in four different modes: Normal, External, Late and Random. For each of these modes a different set of trigger decision lines is taken.

Normal mode: This is the default mode to run DELPHI in central acquisition. It is also the case considered up to this point in the present paper. The decision lines are the four GT1 Y/N and GT2 Y/N lines from Pythia which are valid 3 μ sec and 39 μ sec respectively after the BCO.

External mode: Zeus uses the EXT_T1 decision line. After a WNG_BCO, a gate signal is open whose duration can be adjusted by a front panel trimmer. At the end of this gate Zeus generates T1_YES or T1_NO if a signal is or is not present on the EXT_T1 line. In the case of a T1_YES, Zeus opens another gate, again adjustable by a front panel trimmer, at the end of which a T2_YES is produced.

Late mode: A special input signal, the LATE trigger line, is used to generate the T2 trigger decision, while the T1 trigger decision is fixed to YES. This is the case in which a slow detector (response delay > T1 delay time) is wanted for participating in the trigger sequence.

Random mode: The T1 and T2 trigger decisions come from two one bit/8k deep internal memories loaded by FASTBUS. The address counter of the first memory is incremented at every WNG_BCO, while the second one is at every T1_YES. After reaching the end of the memories, the two sequences restart from the beginning of them. The time delays of T1 and T2 are 3.5 μ sec and 35 μ sec respectively after the BCO or thereabouts.

In order to avoid a hang-up in the trigger sequence, five individually set timeout timers can be triggered in case of: (a) no answer from Pythia after WNG_BCO, (b) no FE_RDY after T1_NO, (c) no FE_RDY after T2_NO, (d) no FE_RDY after T2_YES, or (e) FE_RDY after WNG_BCO (i.e. FE_RDY not lowered as consequence of WNG_BCO). The correspondent error bit is set in case of timeout. The trigger sequence needs to be reset and restarted by FASTBUS action to run again.

Zeus also provides some monitoring facilities for checking the system functionality and the correct synchronism of every partition. There are nine scalars for the most important signals (CLK_BCO gated with run bit, CLK_BCO ungated with run bit, WNG_BCO, T1_NO, T1_YES, T2_NO, T2_YES, Zeus FE_RDY, COSMIC) and one account number register that is incremented by FASTBUS at every T2_YES. The values read from these registers are compared with the values of similar registers also available in the Pandoras.

The debugging of the trigger system is made easier by running Zeus step by step. By means of this feature Zeus allows only one trigger sequence to be started at a time; to start the next one — i.e. to accept the next WNG_BCO — a bit in a register (step bit) must be cleared by FASTBUS.

Fig. 6 Pandora block diagram.

2.5 Pandora

The main role of this FASTBUS device is to generate WNG and CLK signals. The WNG is a single-pulse signal whose leading and trailing edges can be set independently. The CLK is a burst or free-running clock signal with variable frequency; in the case of the burst, the delay of the first clock pulse and the number of pulses can both be set. There are five channels of warnings and three channels of clocks per Pandora completely independent of one another. These signals are sent to the front-end digitizer modules of each partition in synchronism with the central trigger control unit (Zeus) or in stand-alone mode.

The most important feature of Pandora is flexibility, because it must interface the different needs of every partition with Zeus and its protocol, common to the whole experiment.

Every partition, including the trigger partition, must have its own Pandora.

Figure 6 shows the connectivity of Pandora within the trigger system and its internal logical structure. It consists of three parts: FBUS, CNTRL MACHINE and RF.

The FBUS part deals with the FASTBUS protocol and provides all the CSR space registers needed for the unit (i.e. CSR0, CSR1, CSR C000_0000 to C000_0019). The important role of this block is to provide a standard and well-defined way to interface the other two parts.

The CNTRL MACHINE part is interfaced with the protocol of the whole trigger system, and generates the WNGs and the delays for the start of the CLKs.

Table 1
Pandora operative modes

<i>Modes</i>	<i>Start_seq</i>	<i>T1_Y</i>	<i>T1_N</i>	<i>T2_Y</i>	<i>T2_N</i>	<i>Nei_done</i>
Gbl	wng_bco	gbl	gbl	gbl	gbl	any ¹
Loc_norm	clk_bco	loc	loc	loc	loc	any
Loc_prog	any ²	ram	ram	ram	ram	any
Loc_start	ext_start	ram ³	ram ³	ram ³	ram ³	any
Loc_conf	any ²	ext_conf	ram	ram	ram	any

¹ except: csr nei_done

² except: wng_bco

³ program: ram = always yes

For the protocol, a ‘one hot’ synchronous state machine with a simple linear block diagram is built, as shown in Fig. 7. Eight bits in CSR1 allow a complete choice of Pandora operative modes. These modes are not vetoed by hardware; it is the task of the Pandora software driver to inhibit possibly meaningless selections. Table 1 lists the principal modes and their uses. For the generation of the five WNGs and three delays for the CLKs, 13 loadable counters are implemented in FPGA (Field Programmable Gate Array) devices. The Xilinx 3090 FPGAs have been chosen. The maximum clock speed of these devices makes it impossible to have them running at full Rf_3 speed. In order to keep the increment step down to one Rf_3 period (i.e. 8.51 ns), a bank of five clock signals of $Rf_3/5$ (≈ 23.5 MHz) frequency and shifted in phase by

five steps of 72 degrees has been used to drive the counters. In this way every counter always runs at $Rf_3/5$, i.e. with a coarse step of 42.6 nsec, while the fine step of one Rf_3 period can be obtained by choosing the appropriate clock phase.

Tests done on the WNG signals show a min/max jitter of less than 100 ps.

Fig. 7 State Machine block diagram.

The heart of the RF part consists of three custom-designed PLL (Phase Locked Loop) devices for the generation of the 3 CLK signals along with their 3 BURST logical units. In addition a multiplexer unit allows to take the Rf_3 and the CLK_BCO signals either from Zeus (i.e. external) or to generate them internally by means of a high stability crystal tuned at the Rf_3 frequency. The multiplexer unit also provides the bank of 5 clock signals at $Rf_3/5$ frequency, to be used as explained before in the WNG generation.

The PLLs work as frequency synthesizer (Fig. 8). Its input frequency, $Rf_3/145$ (≈ 810 kHz), is small enough to guarantee a fine stepping in the PLL frequency range and its value has been chosen in order to maintain the phase synchronism with all the foreseen bunch upgrading of the LEP machine.

Fig. 8 PLL block diagram.

All the various pieces of the loop are standard market ICs. The VCM can be tuned to a range of 40 to 150 MHz, the phase comparator is a digital $\pm 2\pi$ radians phase detector, the loop filter is built with a wideband operation amplifier (GB = 8 MHz) configured as a type 2, second-order loop filter to guarantee the 0 phase locking of the PLL and its stability and noise performance.

Since some partitions in DELPHI need frequencies lower than those directly obtainable from the PLL, three scalars have been added at its output, dividing its frequency by two or four or eight. In this way a coarse range is set by choosing the two bits that select the appropriate scaling factor $2^P = 1, 2, 4, 8$ and the fine range is set by loading the eight-bit N register (PLL multiplication factor). Therefore, the full range of the PLL functional unit is about 5–150 MHz.

Concerning the a.c. performance, tests have shown a jitter on the output clock signal of 400 ps min/max and 80 ps RMS.

The Burst unit follows the PLL unit and deals with the correct starting, counting and stopping of the burst. The synchronism for a clean start in any conditions of CLK delay (i.e. the delay between CLK_BCO and the first burst pulse) and PLL output frequency is particularly important. For this purpose it has been necessary to delay the trailing edge of the PLL input clock (i.e. the Rf₃/145 clock signal) compared to the CLK_BCO of the same amount as the CLK delay. This is to guarantee that the gate enabling the burst is always opened in phase with the positive edge of the PLL output clock corresponding to the phase comparison in the phase detector, i.e. the only edge for which the 0 phase locking is stable in time under any conditions.

The Pandora unit has recently been redesigned to meet the above specifications. FPGA technology has largely been used for all the FBUS and CNTRL MACHINE parts, while for the RF part the fast ECLiPS (Emitter Coupled Logic in PicoSeconds) technology was more appropriate.

The functional blocks are all implemented on various daughter boards that nearly cover all the mother board area. The mother board only provides connectivity and conversions for electrical signal compatibility (TTL/ECL/NIM). This remarkably improves the manufacturing, debugging and maintenance of the unit by subcontracting companies.

3 CONCLUSIONS

The basic concepts of the DELPHI trigger system have been presented, starting with a brief list of the detectors participating in the trigger decision process, and moving through an overview of the system requirements.

A detailed description of the trigger control signals has been given for only the first two trigger levels (real-time trigger) and their associated hardware.

Pandora was the unit required to be re-engineered. Five prototypes have been successfully tested in the laboratory and are now being installed in the experiment for data taking. A total of 35 units is needed.

The DELPHI trigger system has been fully operational and running since 1990, with global efficiency very close to 100%, proving that its design is also well-suited for operation in the near future at higher energies for the production of W^+W^- pairs.

4 Acknowledgements

We are grateful to the technical assistance of Mr. Angelos Agoritsas and the Layout and Assembly Workshop teams of the Product Engineering & Support Group for the valuable work done in designing and assembling the prototype of the new Pandora unit.

References

- [1] P. Aarnio et al. 'The DELPHI detector at LEP' Nucl. Instrum. Methods Phys. Res., **A303** (1991) pp. 233–276.
- [2] J.A. Fuster et al. 'The online software for the first and second level trigger of DELPHI' DELPHI 91–112 DAS 115 91/12/16.
- [3] V. Bocci et al. 'Architecture and performance of the DELPHI trigger system' CERN PPE/94–141 94/09/02 Submitted to Nucl. Instrum. Methods in Phys.
- [4] L. Bentau et al. 'Architecture and performance of the DELPHI trigger system' IEEE 1992 NSS Orlando Florida 92/10/25.
- [5] B. Bouquet, Ph. Gavillet, J.Ph. Laugier 'The fourth level trigger of DELPHI' DELPHI 93–29 DAS 141.
- [6] P. Charpentier et al. 'The FASTBUS intersegment processor (FIP)' IEEE Conference Washington October 86.
- [7] 'IEEE Standard FASTBUS modular high speed data acquisition and control system and IEEE FASTBUS standard routines' IEEE Std 960–1989 IEEE Std 1177–1989.
- [8] J.A. Fuster et al. 'The 1st and 2nd level trigger user manual; summary of the 1992 trigger performance' Delphi 93–42 DAS 144 PROG 197 93/5/10.
- [9] V. Canale, G. Valenti 'Pythia programming' DELPHI 92–15 DAS 122.
- [10] L. Cerrito 'Zeus the DELPHI trigger supervisor control box writeup and user manual' DELPHI 90–12 DAS 102 90/12/21.

NOTE: Any DELPHI note referenced here can be obtained on request from: DELPHI Secretariat, CERN, CH–1211 Geneve 23, Switzerland.