Upgrade of the ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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Abstract. The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment. It is a scintillating plastic tiles and steel absorbers sampling calorimeter. The scintillators are read-out by wavelength shifting fibers coupled to photomultiplier tubes (PMTs). The TileCal response and its readout electronics are monitored to better than 1% using radioactive source, laser and charge injection systems. The TileCal electronics will undergo major upgrades for the high luminosity phase of the LHC (HL-LHC), so that the system can cope with increased radiation and can meet the requirements of a 1 MHz trigger. Digitized signals from all PMTs are sent to the back-end electronics and to the first level of trigger at 40 MHz. This will provide better precision in the trigger system and will allow the development of more complex trigger algorithms. The TileCal upgrade program has included extensive R&D and test beam studies. A Demonstrator module was inserted in ATLAS in 2019 for testing in actual detector conditions. The main features of the TileCal upgrade program and results obtained from the Demonstrator tests are discussed.

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1. Introduction

The High Luminosity upgrade of the LHC (HL-LHC) [1] will provide an instantaneous luminosity 7.5 times larger than LHC, to reach a dataset size of 4000 fb^{-1} by the end of the HL-LHC. This opens up a new precision physics era in the Higgs sector and allows to probe for Beyond the Standard Model physics with unprecedented sensitivity. The HL-LHC will start to provide collisions in 2027. In preparation, the ATLAS experiment [2] is deep into the design and construction of the upgraded detector. The ATLAS Tile Calorimeter (TileCal) is a scintillating plastic tiles and steel absorbers hadron calorimeter located at $|\eta| < 1.7$. The light is read out by wavelength shifting fibers and photomultipliers. The TileCal role is to measure the energy of hadronic jets and is crucial to the measurement of the missing transverse momentum upon which many physics analyses rely. The TileCal information is also used in the ATLAS trigger to identify events of interest with jets, missing transverse momentum or more complex topologies.

The upgraded ATLAS Trigger and Data Acquisition (TDAQ) system [3] requires the full granularity of TileCal data in order to perform complex algorithms for trigger decisions at 40 MHz. Due to the very high luminosity, up to 200 simultaneous pile-up collisions are expected per bunch crossing. The HL-LHC radiation environment poses new challenges to the TileCal electronics. Electronics components for the upgraded TileCal will have to withstand a total

ionising dose of up to 1000 Gy, a 1-MeV-neutron-equivalent fluence of $\sim 2 \cdot 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$ and a fluence of 20-MeV hadrons of $\sim 10^{12} \text{ hadrons}/\text{cm}^2$, including safety factors.

The new TDAQ architecture along with significantly higher radiation levels require to completely replace and redesign the read out electronics of TileCal. The 10% most exposed PMTs will be replaced by new PMTs, while the remaining optics is to be kept. The higher radiation levels also require the redesign of the low and high voltage distribution and regulation.

2. Mechanics

TileCal is organised into three cylindrical sections along the beam axis. Two Extended Barrels (EB) are located at $0.8 < |\eta| < 1.7$ and one Long Barrel (LB) is located at $|\eta| < 0.8$. Each section is constructed of 64 wedges or modules in the azimuthal direction around the beam line. An EB module is read out by 32 PMTs housed in a super-drawer together with the associated electronics. Super-drawers are located at the outer radius of the calorimeter. An LB module is read out by two super-drawers each housing 45 PMTs and associated electronics. The total number of PMTs is 9852, nearly all calorimeter cells are read out by two PMTs for redundancy.

Figure 1. Mini-Drawer design along with the positioning of the Daughter Board for electronic readout. Figure from Ref. [4].

Figure 2. Arrangement of the MDs in long barrel (top) and extended barrel modules (bottom). Figure adapted from Ref. [4].

The super-drawers are constructed of mechanically linked Mini-Drawers (MD), shown in Figure 1. They hold the PMTs and on-detector electronics. Each MD can hold up to 12 PMTs and is electrically independent from its neighbours. Four MDs are linked to make up one LB super-drawer while only three are required for an EB super-drawer as shown in Figure 2. In EB super-drawers two additional micro-drawers hold PMTs in the right position. The micro-drawers do not hold digital electronics. This modular design was chosen to facilitate handling during installation and maintenance. The MDs are produced from aluminium and high density fire resistant polyethylene. Cooling of the electronics is ensured via a cooling bridge and a water cooling channel inside the aluminium frame. Following extensive prototyping and tests in beam at CERN, the design has been finalised and has entered the final production phase.

3. Read-out electronics

The TileCal read-out electronics (Figure 3) is divided into on-detector electronics that must be radiation hard, and off-detector electronics located in underground counting rooms about 100 m away from the detector. Radiation hardness is not required for off-detector electronics.

Figure 3. Upgraded TileCal electronics. On the left, the on-detector electronics with the PMTs, FENICS, Main Board and Daughter Board, connected by long fibers to the off-detector electronics on the right part of the figure, with the Tile PreProcessor and the TDAQ interface.

3.1. PMT blocks

The PMTs are located inside metal cylinders that include HV-dividers and analog read out boards named FENICS. HV-dividers are described in section 5. The FENICS boards provide shaping and amplification of the PMTs signals. Two types of read out are used. The “fast readout” for physics operates in two different gains in order to cover a dynamic range from ~ 200 fC (MiPs), and up to 1000 pC for the highest energy multi-TeV hadronic jets. The “integrator read out” integrates the PMT current for calibration of the calorimeter with a ^{137}Cs source. It also provides a relative measurement of the accelerator luminosity at the ATLAS collision point [5]. The integrator read out uses six different gains to precisely cover eight orders of magnitude in luminosity measurements, from van der Meer scans to physics collisions. The FENICS board is also able to inject a precise charge and to measure the conversion from pC to ADC counts. The radiation qualification of FENICS along with validation of the design in test beam has been completed and pre-production has been launched.

3.2. Main Boards

One Main Board per MD digitises the data from up to 12 PMTs. The fast read out uses 24 12-bit ADCs @40MSPs, while for the integrator read out it uses 12 16-bit SAR ADCs. The Main Board routes the data to the Daughter Board and provides digital control of the FENICS to configure it for example for calibration or for physics. The Main Board has been fully qualified for the expected radiation environment at HL-LHC and has entered pre-production. For robustness, both the Main Board and the Daughter Board have been designed to have two electrically independent halves. Since each calorimeter cell is read out by two PMTs, the two PMTs are connected to the two separate halves.

3.3. Daughter Boards

One Daughter Board per MD is responsible for the high speed communication (4.8/9.6 Gbps) with the off-detector electronics. It sends both precision data but also slow control data and monitoring data of the on-detector electronics. The Daughter Board receives the LHC clock and distributes it to the on-detector electronics, and exchanges configuration and control commands. Each Daughter Board uses 2 Kintex Ultrascale FPGAs. An earlier design iteration with Kintex Ultrascale Plus exhibited single event latch-ups at the HL-LHC hadron fluence, however the latest iteration uses Kintex Ultrascale and did not exhibit latch-ups on a sample of two FPGAs. The final prototype is to be fully validated in radiation field.

3.4. PreProcessor

The TileCal PreProcessor receives the data from the Daughter Board, computes the energy and time of the PMT pulses using digital filters, and buffers the data while waiting for a trigger decision from the ATLAS trigger. Upon a trigger acceptance signal, the data is transmitted

to the Front End Link eXchange [6] (FELIX) system. The PreProcessor system is based on an ATCA standard carrier board, with four Compact Processing Modules (CPM), each being able to process the data from two TileCal modules. The CPM is designed as a double mid-size Advanced Mezzanine Card (AMC) with Kintex Ultrascale FPGAs. A dedicated system-on-chip extracts monitoring data from the data stream and communicates with the ATLAS Detector Control System via Ethernet. A rear module, the TDAQ interface (TDAQi), uses cell energies to compute trigger objects such as fully customisable sums of calorimeter cell energies, to pass on to the first level of the ATLAS trigger. The carrier board and CPM have been prototyped in their full size configuration and are used successfully with a full size demonstrator (see Section 6). Validation of high speed communication working with a prototype of the rear module has been performed successfully in the lab.

4. Low voltage distribution

Figure 4. The architecture of the low voltage system for the TileCal HL-LHC upgrade. The 10 V bricks represent the 200 VDC to 10 VDC converters. Stage 3 is located directly on the front-end electronics.

A three stage low voltage system, as shown in Figure 4, is used. Low voltage power supplies (LVPS) are placed on-detector and convert 200 VDC to 10 VDC as required for the on-detector electronics. Due to their placement, the LVPS are the TileCal component most exposed to radiation. The LVPS rely on switching “Buck Converter” technology, assembled with COTS components. Following an extensive irradiation test campaign, radiation hard components have been identified. The monitoring and control functions have been separated for enhanced robustness. The monitoring functions are ensured by the CERN-developed ELMB2 which is functionally equivalent to, but more radiation hard than the legacy Embedded Local Monitor Board (ELMB) [7]. The on-detector part of the ON/OFF/ENABLE control of each LVPS is ensured with a purely passive system relying on a so-called ELMB-motherboard and uses a tri-state voltage level to minimise the necessary cabling. The control system allows individual

control of single MDs and each Main Board and Daughter Board half is powered by a separate converter for additional robustness. The ELMB-motherboard also routes power to the ELMB2. Point-of-load regulators located directly on the Main Board and the Daughter Board make up the third stage of the LV system. A full vertical slice of the LV system was tested at CERN at the end of 2019 and early 2020. It demonstrated required functionalities and robustness of the full system, from its on-detector elements all the way to its remote control elements.

5. High voltage distribution and regulation

Figure 5. Architecture of the High Voltage system for the TileCal HL-LHC upgrade. Figure from Ref. [4].

In order to ensure a 1% precision on the energy scale in TileCal, the high voltage fed to the 8-dynode PMTs must be stable within better than 0.5 V in the range 600–900 V. Active dividers are necessary in order to maintain a linearity better than 1%, given the high PMT current at high luminosity. This current can reach 40 μ A in the most exposed cells. To maintain the linearity, a design with transistorised dividers in the last dynodes was selected. The linearity of the system active-divider-PMT was successfully tested in a set up designed to emulate pulses from physics on top of a continuous activity from pile-up. The active dividers have been fully validated in radiation tests and have recently completed pre-production.

The high voltage regulation is done remotely from underground counting rooms, see Figure 5, with custom HV supply boards and custom remote regulation boards. Each regulation board serves one TileCal module. Full size prototypes of the regulation boards have been validated and were shown to meet the HV stability requirements. Full size prototypes of the supply boards are currently being tested with the regulation boards. The remaining elements are passive: long cables from counting room to every module and passive distribution boards. The passive distribution boards have been successfully prototyped and used in test beam. The cables are challenging due to limited space for routing inside ATLAS and strict material safety regulations from CERN. One manufacturer has so far been able to provide cables that met all requirements, but work with several additional manufacturers is ongoing.

6. Testbeam and demonstrator results

Five test beam campaigns were carried out at CERN with the TileCal upgrade demonstrator with electronics for HL-LHC. Most hardware evolution since the test beam is related to specific

components replacements to ensure radiation hardness. Figure 6 (left) shows the TileCal response to electron beams, allowing to measure the pC to GeV scale and verify the linearity. Figure 6 (right) shows the response to hadrons in data and Geant 4 simulations [9] as function of the beam energy. In July 2019 the demonstrator was installed inside ATLAS and its read out has been integrated and tested successfully with the overall ATLAS data flow.

Figure 6. Left: Total energy deposited in the TileCal demonstrator with electron beams and comparison with simulation. Right: Energy response $R^{<E^{raw}>} = \langle E^{raw} \rangle / E_{beam}$. The energy E^{raw} is the total energy in the shower obtained by summing TileCal cells with signals larger than two times the electronic noise after calibration with charge injection and a ^{137}Cs source. Figures from Ref. [8].

7. Conclusion

The detailed design of ATLAS TileCal for HL-LHC is nearly complete, where essentially all parts of the system have been prototyped and tested with other parts of the system. Several system level tests have been performed, in particular with the read out electronics with the demonstrator in test beam and more recently with the insertion of the demonstrator into ATLAS. System level tests for the low voltage distribution systems have been successfully completed. Most of the on-detector electronics is entering the pre-production phase. The project is on schedule for installation in the ATLAS pit by the end of 2024.

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