Design of Bus Tapes for the ATLAS Strip End-Cap at the HL-LHC

F.Carrió, J.Bernabeu, V.Cindro and A.Gorišek

Abstract—The ATLAS Phase-II Upgrade will replace the Inner detector with a new all-silicon Inner Tracker (ITk) to accommodate the radiation damage and track density expected at the High-Luminosity LHC (HL-LHC).

The all-silicon ITk for the HL-LHC consists of a pixel detector with 5 barrel layers and multiple forward disks at a small radius, and a strip tracking detector at the outermost part with 4 barrel layers and 6-end-cap disks on each side.

This contribution presents the design of the flexible circuit (bus tape) for the local support structures of the end-cap region of the strip detector, called petals.

The bus tapes provide the electrical interface to common services for all the on-board subsystems including power, control and data interfaces. Connections to external services outside of the petals are carried out through the End-of-Structure (EoS) card using optical fibres and copper wires.

The bus tapes are manufactured as a 2-layer printed circuit board using polyimide and adhesive Kapton films, with a total thickness of $185\ \mu\text{m}$ and a total length of 60 cm. The layout design has been focused on achieving good signal and power integrity while keeping low mass and low thermal resistance.

A total of 768 end-cap bus tapes are needed between 2021 and 2022 for the production of 384 petals with 6,912 modules, where each end-cap disk will consist of 32 petals.

Index Terms—ATLAS Inner Tracker (ITk), Data Acquisition (DAQ) systems, High Energy Physics, High-speed electronics, Radiation Hard Electronics.

I. INTRODUCTION

THE ATLAS experiment [1] at the Large Hadron Collider (LHC) has been operating for the last decade, collecting an integrated luminosity of $175\ \text{fb}^{-1}$ between Run 1 (2011–2014) and Run 2 (2015–2018).

In 2025, ATLAS will undergo a major detector upgrade, called Phase-II Upgrade [2], to cope with the requirements of the High Luminosity LHC (HL-LHC), and to accommodate the detector to a new trigger and acquisition architecture. The HL-LHC will provide an instantaneous luminosity of $7.5 \times 10^{-34}\ \text{cm}^{-2}\text{s}^{-1}$ increasing the total pile-up collisions in ATLAS up to 200 simultaneous events. The HL-LHC is expected to deliver a total integrated luminosity of $4000\ \text{fb}^{-1}$ in 10 years of operation.

The current ATLAS Inner Detector will be replaced with a new all-silicon Inner Tracker (ITk) detector [3], which will extend the tracking coverage of ATLAS from a pseudo-rapidity

of $\eta < |2.5|$ to $\eta < |4.0|$. ITk has been designed to meet the increased density track and radiation levels expected at the HL-LHC. The ITk detector will consist of a pixel detector at the region closest to the beam pipe and a strip detector surrounding it. Figure 1 presents the layout of the ITk detector.

Figure 1: Layout of the ITk detector [3].

The pixel detector is subdivided in five barrel layers with inclined sensors in the forward region and an end-cap with individual rings. The strip detector consists of four barrel layers in the center and forward regions with six disks at each end, so-called end-caps.

II. ITK STRIP DETECTOR

The strip detector comprises of 18,000 modules with 60 million of channels integrated in modular local support structures with two different designs: staves for barrel region and petals for the forward regions.

The barrel consists of a total of 392 rectangular staves, each one hosting 14 sensor modules per side. Each of the end-caps are composed of six disks, where each disk contains 32 wedge-shaped petals with 6 modules per side. In total, the forward regions of the strip detector will contain 384 petals.

A. End-cap Local Supports

The end-cap local support structures, or petals, provide high-precision positioning, mechanical stability, cooling and an electrical connections to the sensor modules.

Petals are formed by a carbon-fibre core with integrated titanium cooling tubes for a dual-phase CO_2 cooling system operated at a design temperature of -35°C . Both surface sides of the carbon-fibre core are enclosed with carbon-fibre face-sheets and co-cured with polyimide flexible printed circuit boards (PCBs), called bus tapes, which provides data transmission and power distribution for the sensor modules. The

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strip modules are glued to the surface of the bus tapes, and electrical connections between the modules and the bus tapes are done via ultra-sonic wire-bonding. The local support design provides a short thermal path for the sensor modules and a low increase of the detector mass.

Figure 2 presents a cross-section of the end-cap local support structures and modules for the strip detector.

Figure 2: Schematic cross-section of the end-cap local support structure and modules [3].

Each petal is readout and operated via a End-of-Substructure (EoS) card which interfaces with the ATLAS trigger and data acquisition system through optical fibres and lpGBT chips [4].

Petals are organized in 6 sub-regions or rings (R0-R5), where R0 corresponds to the innermost ring and R5 to the outermost ring. Figure 3 presents a picture of a fully-assembled petal with the sensor modules and readout electronics.

Figure 3: Semi-electrical petal fully-assembled with the readout and power electronics, one real R0 sensor and 5 dummy sensor modules.

B. Sensors modules

The basic detector units of the strip detector are the modules. A module consists of a silicon strip sensor, one or two hybrid

circuits boards hosting the readout ASICs, and a power board to provide high and low voltage (LV) to the detector electronics. Figure 4 depicts an assembly schema of a sensor module with all the components forming a module.

Figure 4: Assembly schema of a end-cap sensor module with its components [3].

The strip sensors are single-sided n^+ -in-p Float Zone sensors [5], capable of operating under fluences of $1.6 \times 10^{15} n_{eq}/cm^2$ (including a safety factor of 1.5). Contrary to the n-bulk sensors, n^+ -in-p sensors do not suffer from radiation-induced type inversion. The isolation between neighboring strip sensors is achieved with the p-stop implants. The strip sensors are $320 \mu m$ thick and they are produced on 6-inch wafers. In the end-caps, there are six different sensor designs with wedge shape and curved edges providing full $R-\phi$ coverage.

The hybrid circuit boards [6] are 4-layer Kapton flexible printed circuit boards hosting the readout sensor ASICs for the ITK strip detector: the ATLAS Binary Chip (ABCStar) [7] and the Hybrid Controller Chip (HCCStar). Due to the petal geometry there are 13 different hybrid designs.

The ABCstar is the analog front-end readout ASIC. This ASIC has been built from 130 nm CMOS technology and it provides amplification, shaping and binary discrimination to read out 256 strip sensors. The HCCStar, also built from 130 nm CMOS technology, provides control and readout capabilities to the ABCStar chips. It transmits processed configuration and calibration commands to the ABCStar chips and aggregates the readout sensor data from the ABCStar chips in a single event before its transmission towards the EoS.

Finally, the power board hosts DC-DC converters with low-mass [8] to lower the voltage from the distributed 11 V to the required 1.5 V by the hybrids, and High Voltage (HV) bias filtering for the sensors. Each power board hosts an Autonomous Monitor and Control Chip (AMAC) ASIC to monitor voltages, currents and environmental conditions, and to individually control LV and power states.

III. ELECTRICAL BUS TAPE

The bus tapes are flexible solutions which provide the necessary electrical connections to common services for all the on-detector subsystems including high and low voltage distribution, control and data interfaces. Connections to external

services outside of the petals are performed through the EoS card via optical fibres and copper wires.

The bus tape is designed as a 2-layer flexible printed circuit board using polyimide and adhesive Kapton films, with a total thickness of $185\ \mu\text{m}$ and a total length of 60 cm. Figure 5 presents a detailed schema of the composition of the petals.

Figure 5: Full assembly schema of a petal structure.

These flexible printed circuit boards are co-cured onto both sides of low-mass carbon fiber structures providing high thermal performance and proper cooling for the sensor modules. Figure 6 shows a picture of the first prototypes of the flexible bus tape with zoomed-in portion details of the EoS, hybrid and power board interconnections.

Figure 6: Picture of the first prototypes of the bus tape.

A. Bus Tape Layout

The bus tape layout design has been focused on achieving proper signal and power integrity, while keeping the material detector budget low and a short thermal path to the sensor modules. Via connections are avoided in order to enhance the reliability of the bus tapes and increase the manufacturing yields, and all interconnections to the hybrids, power boards and EoS are done through ultra-sonic wire-bonding. Since no via interconnections are present in this flexible circuit, connections to the bottom layers are achieved via opening cuts in the polyimide and top layers.

The bus tapes provide a high-speed point-to-point communication path between the hybrids and the EoS card for the

readout and operation of the petals. Binary sensor data is transmitted from the hybrids to the EoS card at 640 Mbps, and Timing, Trigger and Control (TTC) data is distributed from the EoS to the hybrids at 160 Mbps.

The differential lines for the communication between the modules and the EoS have been designed to match $100\ \Omega$. Multiple differential micro-strip geometries with different track and gap configurations were simulated and tested to adjust the manufacturing process of the flexible circuits. The optimal geometry resulted in differential lines with a $116\ \mu\text{m}$ gap and a $84\ \mu\text{m}$ track width.

Signal integrity of the bus tape differential lines was verified during the PCB design. Simulations with ANSYS Workbench software were performed to ensure low insertion loss levels and to predict the maximum voltage drop in the low voltage rails powering the readout electronics. Figure 7 presents the results of the insertion loss simulations for all the sensor data lines between the hybrids and the EoS card.

Figure 7: Simulated differential insertion loss for the transmission data lanes between the hybrids and the EoS card.

The maximum insertion loss at the Nyquist frequency (320 MHz) for the longest path (R0) is $-3.5\ \text{dB}$. These low attenuation levels indicate proper signal integrity at the designed operation data rates using Kapton material as dielectric.

Figure 8 presents the simulations of the voltage drop across the LV power plane at worst case conditions. The maximum round trip voltage drop observed in the simulations between the power and return rails is lower than 200 mV for module R0. These results exceed the requirements of a maximum voltage drop of 1 V [9].

B. Automated Quality Control Tests

The detection of defects in the bus tapes prior to the assembly of the petals is important to prevent low production yields and high infant mortality rates. The difference between the thermal expansion coefficients of the bus tapes and carbon-fibre core could introduce important defects in the flexible boards during the co-curing process.

All bus tapes undergo to a Quality Control (QC) process to validate the properties of the electrical interfaces and physical dimensions according to specifications. The tests include

Figure 8: Simulation of the voltage drop across the LV power plane at worst case conditions. The maximum voltage drop is 100 mV for module R0.

the measurement conductivity and resistance of tracks, HV insulation between adjacent traces and measurements of the dimensional tape distortion. The testing procedure is carried out at different production stages of the petals: after the production of the bare bus tapes; after co-curing the bus tapes to the carbon-fibre face-sheets; and finally after the completion of the petal assembly.

An automated vision robot [10] has been developed to perform electrical and dimensional tests for every bus tape. The test station consists of motorized XY table and two independent probe heads with cameras for alignment with XYZ control. The linear stages provide a resolution of $5 \mu\text{m}$ in XY position with a range of $0.6 \text{ m} \times 1.6 \text{ m}$, and the stepper motor achieves a $1 \mu\text{m}$ resolution in Z direction. A vacuum chuck holds the bus tapes to the test station during the measurements. Figure 9 presents a picture of one of the head probes testing a HV pad.

Figure 9: Detail of a head probe testing a HV pad.

Global fiducial markers are used by the automated system to measure the dimensional distortion of the bus tapes, while local fiducial markers permit the correct positioning of the probes. These fiducial markers are also used by other automated systems to assemble and wire-bond the sensor modules with high precision.

During the tests, the automated robot determines the position of the bus tape by using the cameras and the global fiducial markers. Variations on the bus tape dimensions could be caused during the lamination process due to the flexibility of the Kapton material or during the co-curing process because the expansion of the material. A maximum variation of $300 \mu\text{m}$ of the bond-pad nominal locations respect to the bus tape center is accepted in the dimensional test.

The resistance per length for all the interconnections is measured by positioning the two probe heads between two pads in the same net. Defects producing open and short circuits are also detected during these tests. Figure 10 presents a histogram of the resistance per length measurements for all the interconnections. The measurements are grouped in three different sets of lines according to the track width ($84 \mu\text{m}$, $100 \mu\text{m}$ and $200 \mu\text{m}$).

Figure 10: Histogram of the resistance per length measurements for all the interconnections in the bus tape.

For the HV insulation resistance test, the leakage current in the HV lines is measured with nA precision. The maximum leakage current when applying 1000 V (twice the maximum sensor bias voltage in operation) should not exceed 20 nA, indicating an insulation resistance greater than $50 \text{ G}\Omega$. An example for the HV insulation resistance measurements is presented in Figure 11.

Figure 11: Histogram of the leakage currents during the HV insulation test measurements.

Furthermore, the sacrificial area of the bus tape includes an additional set of test coupons with bonding pads, differential lines and high voltage test structures. These test coupons are used as support for the automated QC tests and for traceability.

IV. CONCLUSIONS AND FUTURE PLANS

The new conditions imposed by the HL-LHC require the replacement of the inner detector with an all-silicon Inner Tracker detector by 2025.

As part of the local support structures for the strip detector, the end-cap bus tapes will provide to sensor modules a electrical path for data communication and power distribution. The designed bus tapes exceed the requirements in terms of low insertion losses in the data communication lines and minimal voltage drops across the power planes.

The qualification of the bus tapes is a key point during the production stage which requires specific QC test procedures. The QC tests will be performed with an automated vision system capable of identifying different types of defects on the bus tapes as cracks or high leakage currents.

The bus tape design passed the Final Design Review in 2019. The production of about 800 bus tapes will start during 2021 and it is expected to end in 2022. The installation and commissioning of the ITk strip detector is foreseen for 2025.

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