AN INTEGRATED CIRCUIT LOGIC MODULES SERIES

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# TABLE OF CONTENTS

**PART I**

INTEGRATED CIRCUITS AND DATA HANDLING SYSTEMS

1. INTRODUCTION ........................................ 1

2. A SHORT REVIEW OF THE INTEGRATED CIRCUIT TECHNOLOGY ........ 1

   2.1 Transistors .................................... 1
   2.2 Resistors ....................................... 2
   2.3 Capacitors .................................... 2

3. INTEGRATED CIRCUIT RELIABILITY ......................... 4

   3.1 Component reliability .......................... 4
   3.2 Component misapplication ...................... 4
   3.3 Connections .................................. 4
   3.4 Ways to increase integrated circuit reliability . 5

4. INTEGRATED CIRCUIT LOGIC FAMILIES ..................... 5

   4.1 Direct coupled transistor logic ............... 5
   4.2 Resistance transistor logic ................... 6
   4.3 Diode transistor logic ........................ 6
   4.4 Transistor-transistor logic .................. 10
   4.5 Conclusions .................................. 10

5. SEMICONDUCTOR CIRCUITS AND MODULAR PACKAGING .......... 11

   5.1 The use of plug-in modules .................... 11
   5.2 Packaging dominates cost ..................... 11
   5.3 Basic packaging decisions .................... 12
   5.4 Integrated circuit package styles ............. 12
   5.5 Component interconnection techniques .......... 13
   5.6 Best module size ................................ 13
   5.7 Throw away module cost ......................... 14
   5.8 Input/Output connector ........................ 15
   5.9 Module interconnection techniques ............. 16

6. THE DEVELOPMENT OF AN INTEGRATED CIRCUIT LOGIC MODULES SERIES .... 16
PART II

THE CHARACTERISTICS OF THE NFA INTEGRATED CIRCUIT MODULES SERIES

1. GENERAL DESCRIPTION 19
2. MECHANICAL FEATURES 19
   2.1 Base material 19
   2.2 Physical size 19
   2.3 Connector characteristics 19
   2.4 Integrated circuit packaging 19
   2.5 Soldering system 21
3. PRINTED CIRCUIT CHARACTERISTICS 21
   3.1 Artwork characteristics 21
   3.2 Conductors characteristics 21
   3.3 Plated-through holes 24
4. CONNECTOR CHOICES 24
   4.1 Winchester Connector 24
   4.2 Burndy connector 24
   4.3 AMP connector 24
5. RELIABILITY, TESTS AND COSTS 25
6. ELECTRICAL CHARACTERISTICS 25
   6.1 The integrated circuit family used 25
   6.2 System speed 25
   6.3 Nominal logic levels 27
   6.4 Loading factor and driving ability definitions 27
   6.5 Noise immunity 29
   6.6 Timing 29
   6.7 Power supply requirements 35
   6.8 Temperature range 35
   6.9 Grounding and power distribution rules 36
   6.10 Glossary 38
   6.11 Symbology 39

BIBLIOGRAPHY 40
PART III
TECHNICAL SPECIFICATIONS OF THE MODULES

<table>
<thead>
<tr>
<th>Module</th>
<th>Stock Number</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2/3 IN GATE</td>
<td>(NPA 231 G01)</td>
<td>1.1</td>
</tr>
<tr>
<td>4 IN GATE</td>
<td>(NPA 231 G02)</td>
<td>2.1</td>
</tr>
<tr>
<td>8 IN GATE</td>
<td>(NPA 231 G03)</td>
<td>3.1</td>
</tr>
<tr>
<td>4 IN BUFFER</td>
<td>(NPA 231 G04)</td>
<td>4.1</td>
</tr>
<tr>
<td>N FAN-IN OR</td>
<td>(NPA 231 M01)</td>
<td>5.1</td>
</tr>
<tr>
<td>QUAD EXCL. OR WITH EXP.</td>
<td>(NPA 231 M02)</td>
<td>6.1</td>
</tr>
<tr>
<td>4 BIT BINARY COMP AND EXCL. OR</td>
<td>(NPA 231 M03)</td>
<td>7.1</td>
</tr>
<tr>
<td>PARITY GENERATOR</td>
<td>(NPA 231 M04)</td>
<td>8.1</td>
</tr>
<tr>
<td>READ/WRITE MULTIPLEXER</td>
<td>(NPA 231 M05)</td>
<td>9.1</td>
</tr>
<tr>
<td>MEMORY FLIP-FLOP</td>
<td>(NPA 231 F01)</td>
<td>10.1</td>
</tr>
<tr>
<td>SEQUENTIAL FF AND GATES</td>
<td>(NPA 231 F02)</td>
<td>11.1</td>
</tr>
<tr>
<td>SHIFT REGISTER</td>
<td>(NPA 231 F03)</td>
<td>12.1</td>
</tr>
<tr>
<td>SYNC UP/DOWN BCD DECADE AND DECODER</td>
<td>(NPA 231 F04)</td>
<td>13.1</td>
</tr>
<tr>
<td>INTEGRATING MULTIVIBRATOR</td>
<td>(NPA 231 S01)</td>
<td>14.1</td>
</tr>
<tr>
<td>MONOSTABLE MULTIVIBRATOR</td>
<td>(NPA 231 S02)</td>
<td>15.1</td>
</tr>
<tr>
<td>TRANSMITTER</td>
<td>(NPA 231 S03)</td>
<td>16.1</td>
</tr>
<tr>
<td>RECEIVER</td>
<td>(NPA 231 S04)</td>
<td>17.1</td>
</tr>
<tr>
<td>INPUT LOGIC LEVEL CONVERTER</td>
<td>(NPA 231 S05)</td>
<td>18.1</td>
</tr>
<tr>
<td>OUTPUT LOGIC LEVEL CONVERTER</td>
<td>(NPA 231 S06)</td>
<td>19.1</td>
</tr>
</tbody>
</table>

*) The stock numbers are in brackets
PART I

INTEGRATED CIRCUITS AND DATA HANDLING SYSTEMS
PART I
INTEGRATED CIRCUITS AND DATA-HANDLING SYSTEMS

1. INTRODUCTION

Monolithic integrated circuits are now available at prices, and with specifications, which make them attractive for use in scientific and industrial as well as in military and aerospace applications. Until very recently, integrated circuits were considered useful only for special environments which demanded maximum reliability, and minimum size and weight. The prices of integrated circuits have decreased to such an extent that it can cost less to build, and certainly cost less to operate a system built with these devices than one using discrete components. The drop in price is due to many factors: in fact, the past two years have seen profound developments in the state-of-the-art of semiconductor integrated circuits. These developments have culminated in the announcement of general availability of "multi-function" semiconductor networks with two, three, four, or more complete circuits diffused into a single bar and contained in a single package. A step-function decrease in the effective cost of integrated circuits has resulted.

In fact, an examination of the integrated circuit manufacturing cost-structure verifies that the network cost increases only slightly with increased complexity. The manufacturing cost of integrated circuits can be divided into two distinct areas: slice processing and network assembly (in fact 80 to 90% of the total cost is due to the sub-assembly steps). The first area includes the cost of individual handling of the slices (each of which contains many network bars), and although the cost accumulates per slice, it is constant regardless of the network complexity. Of course the number of networks per slice decreases directly with increasing complexity; therefore slice preparation costs per network vary according to the complexity of the networks. Assembly costs involving handling, mounting, inspecting, and capping each individual network are almost constant in spite of the variations in complexity and size. Even the probe and final electrical test costs are insensitive to complexity since automatic test equipment is used.

2. A SHORT REVIEW OF THE INTEGRATED CIRCUIT TECHNOLOGY

At this point it is perhaps worth while to present a short review of the integrated circuit technology.

2.1 Transistors

Transistors in integrated circuits are diffused silicon structures which differ from their discrete device counterparts in that generally they must be electrically isolated from one another and their collector contacts must be brought out from the top surface for interconnection purposes. Figure 1 illustrates typical cross-sections for an all-diffused NPN device and for a diffused-epitaxial structure. Isolation is achieved by surrounding the N-type collector regions with a P region. In digital circuits this region is usually connected to ground so that it is held at a negative potential with respect to any of the collectors in operation. Top-side collector contacts are made with aluminium deposited in
pre-diffused n-contact areas. Since the collector current must flow laterally in these devices, they will have a higher saturation collector resistance than that of discrete transistors, and in direct-coupled low-level circuits this prescribes a limit for the maximum operating current level.

The isolation junction has electrical significance in that it adds capacitance to ground, and in fact this capacitance can become a limiting factor in performance. For devices designed to operate at a given current level and hence a given collector saturation resistance, the epitaxial design will have typically one-half the isolation capacitance of the all-diffused device. At the present time, the smallest geometry transistors that have been made show a typical saturation collector resistance of 70 Ω and an isolation capacitance of 10 pF.

A peculiar property of the structures in Fig. 1 is that if the collector junction is close enough to the isolation junction, then the PNP transistor action can occur between the base, collector, and isolation areas.

This can be beneficial in the sense that it helps to control collector charge storage in saturation by collecting carriers injected into the collector region. However, it can also be detrimental in some forms of logic, such as transistor-coupled logic. This is illustrated in Fig. 2, where the PNP transistor is shown by a dashed line. If all inputs to this gate are high, a fraction of the node current I_n equal to the alpha of the PNP transistor will be shunted to ground by the PNP action.

2.2 Resistors

Resistors for integrated circuits have, until recently, been made entirely by diffusion. They are usually fabricated at the time of the transistor base diffusion in separate isolation regions. A typical cross-section is shown in Fig. 3.

Because of the surrounding junctions, stray elements are an integral part of these resistors and have a net effect of adding capacitance to ground, thus limiting circuit performance. Other disadvantages of these devices are poor tolerance control on absolute resistor values, large amounts of substrate area required, and large temperature coefficients. More recently, resistors have been made by thin film deposition techniques on top of silicon oxide, which is used for electrical isolation. A typical structure is shown in Fig. 4.

2.3 Capacitors

Capacitors for integrated circuits can be fabricated either by utilizing the capacitance of a PN junction or by metal-over-oxide techniques. Figure 5 shows a metal-over-oxide capacitor in which the bottom contact is formed during the emitter n⁺ diffusion. The capacitance of a PN junction will vary between one-half and one-third of the applied voltage power, and becomes completely unusable when the junction is forward biased. Metal-over-oxide capacitors, on the other hand, show very little variation over ranges of ±10 volts applied. The latter would therefore have wide application in timing circuits where linearity is important. It is also worth noting that the maximum capacitance per unit area is 0.5 pF/mil², which sets a practical upper limit on the value of capacitance that can be obtained at about 0.001 μF. This is more than adequate for most digital applications.
3. **INTEGRATED CIRCUIT RELIABILITY**

The reliability performance of integrated circuits is constantly being compared to that of transistors in similar applications. The ARINC report *) surveys five operational computer systems, and illustrates that the rate of replacement of integrated circuits is no higher than that of transistors in similar digital applications. Equipment reliability has therefore been improved by a factor comparable to the quotient of the original number of transistors divided by the replacing number of integrated circuits.

To appreciate the reasons for increased equipment reliability by the use of integrated circuits, we must recall the main reliability problems, namely:

- component reliability
- component misapplication
- unreliable connections.

These problems have been reduced by the use of integrated circuits.

3.1 **Component reliability**

Electronic equipment can be no more reliable than the cumulative reliability of its components.

Since some reliability factors are directly dependent simply upon the number of basic elements in a piece of equipment (whether they be functional electronic blocks or discrete components), the reliability will be improved by the use of integrated circuits merely by reducing the total number of elements.

3.2 **Component misapplication**

A second cause of equipment reliability problems is due to the misapplication of components; integrated circuits are designed around specific parameters and will not function unless used under these conditions. The application must duplicate closely the design criteria and optimum conditions for which the circuit was manufactured and tested; thus reliability problems due to misapplication are reduced.

3.3 **Connections**

A large number of connections, including evaporated, thermal-compression welded, crimped and soldered types, both internal and external to the components, are required for discrete component printed-board circuitry. These connections involve a number of materials and, in the case of internal component connections, are made by different manufacturers. In integrated circuit equipment, fewer connections are required, and a higher percentage of these are formed simultaneously by evaporation. There is also a smaller number of different materials involved in the connections. The majority of the connections are internal to the integrated circuit package; thus their integrity can be assured by the integrated circuit manufacturer. The reduction in the number and variety of connections made possible by the use of integrated circuits is another major contribution to improved reliability of electronic equipment.

3.4 Ways in which to increase integrated circuit reliability

The major factors affecting reliability within the control of the user are as follows:

i) Derating

ii) Redundancy

iii) Cooling

i) When considering the rating of a network it must be appreciated that one major difference between networks and conventional circuits is that power dissipation in the network is a characteristic and not a rating: when a given voltage is applied, a defined current will flow through the network, and this current level is set by the network manufacturer. The user is therefore unable to derate the component on power dissipation; he can, however, derate on logical power and effectively increase the system reliability. For example, a unit with a driving ability of 20, when used with a fan-out of only 5, will accept much wider deviations within the package from the test limit before the actual system-failure level is reached. Thus derating at the function level may be used effectively to improve reliability.

ii) Redundancy may be applied either at the component level or at the function level within a network, both controlled by the manufacturer and affecting his nominal failure rate, or at the network level within a system, controlled by the user. By applying suitable redundant techniques at network level in a system, an increase in MTBF of 5:1 is possible for an increase in the number of networks of 4:1.

iii) In considering the cooling of a system, it is interesting to consider failure-rate variation with temperature. Nominal failure rates obtained to date, when plotted on a logarithmic scale against \(10^y/\text{°K}\) on a linear scale, give a reasonably straight line. The decrease in failure rate for semiconductor networks when operating ambient temperature is reduced from 125°C to 65°C is from 4.5 to 1, thus indicating that one possible method of increasing the percentage confidence of completing an operating period is to cool the system using thermoelectric cooling elements.

A further method of improving digital system reliability is to use much faster digital circuits. This is not immediately obvious, but can be appreciated from the following argument. The argument is based upon the assumption, which is reasonable when using semiconductor networks, that a medium-speed range of networks, say 1 MHz, and a high-speed range of networks, say 100 MHz, have equal failure rates. A particular piece of logic in a system involving \(x\) medium-speed elements may perform a number of operations \(y\) in a time period \(t\). If this piece of logic is replaced by \(x/10\) high-speed elements which may perform the same number of operations \(y\) in the same time period \(t\), then the number of operations per failure has been increased by one order, or the MTBF for this part of the system has been increased by one order. This applies to any digital system in which the logic can be redesigned to utilize higher-speed networks in this way.

4. INTEGRATED CIRCUIT LOGIC FAMILIES

4.1 Direct-coupled transistor logic

The early lines from Fairchild and Texas Instrument followed quite closely those of their discrete-component predecessors. Component count was kept low, as the concept that
active elements in a monolithic chip are very inexpensive had not yet been exploited. The early logic scheme was DCTL (Direct-Coupled Transistor Logic). Figure 6 shows the NAND/NOR gate of this family. The threshold function is achieved through the base-to-emitter V-I characteristics of the load transistor. This characteristic is of the diode type. Whenever a gate input is at a high state, the output (point A) is low, and the output of each of the load transistors, Q₁ through Q₄, is high. To achieve a logic fan-out, several threshold devices must be connected in parallel; these devices constitute the total load seen by the gate element. The gate element should, ideally, supply the same amount of current to each of the loads. However, relatively small variations in threshold characteristics result in a wide variation in the current supplied to the loads. It may happen that one load is therefore supplied with three times its required current. This current represents waste, and the condition is called current-hogging. Current-hogging limits the loading capability of DCTL gates, and thus limits their application except when the base-to-emitter characteristic of the load transistors can be closely matched. Figure 6 also shows that when the gate is not conducting, a small negative noise voltage introduced between A and any of the loads will turn off that particular transistor, since the base-to-emitter voltages are small.

4.2 Resistance transistor logic

A small resistance (100 Ω) introduced into the base of each transistor (see Fig. 7) in the DCTL system reduces the spread of the diode-type load characteristic, reduces the waste current, and increases fan-out capability. Noise rejection, however, will still be relatively low.

The operational levels are:

\[ 0 \rightarrow V_{CE} \text{ sat} \]

\[ 1 \rightarrow \frac{V_{CC} R_2}{R_1 + R_2} \]

the second being a function of the fan-out N.

The circuit is unfortunately slower than the basic circuit because the turn-off current is limited by R₂.

4.3 Diode transistor logic

Signetics first introduced diode transistor logic. The basic circuit of the DTL family is shown in Fig. 8. The salient feature of this circuit is the replacement of one of the offset diodes usually found in conventional circuits (Fig. 9) by a transistor whose collector is returned to the midpoint of the pull-down resistor. By this means the relative gating efficiency is doubled that obtained with the conventional DTL design; hence the hFE requirement of the output transistor is reduced by one-half for a given fan-out or, conversely, the fan-out is doubled for a given hFE requirement. The compromises necessary in power dissipation, component tolerance, and fan-out capability are thus greatly relaxed, permitting a performance unattainable with the conventional approach.

A disadvantage of DTL is the need for close-tolerance (10%) resistors.
Fig. 6  DCTL NAND GATE

Fig. 7  RTL MODIFIED DCTL NAND GATE
Fig. 8 Integrated DTL gate

Fig. 9 Conventional DTL gate
Fig. 10  "PHOENIX GATE"

Fig. 11  SERIES 54/74 GATE

Fig. 12  SYLVANIA SUHL GATE
4.4 Transistor-transistor logic

Transistor-transistor logic (TTL) was developed to solve the problem of capacitive loading resulting from some packaging schemes, e.g. flat packs on multilayer printed circuit boards.

The circuit was first realized in the configuration used in Litton's Phoenix Missile project, shown in Fig. 10. Seeking to better the performance of the "Phoenix gate", several firms have developed modified TTL circuits, notable amongst which are TI's "Series 54/74" and Sylvania's "SUHL".

The Series 54/74 circuit configuration (Fig. 11) was selected primarily for power/speed considerations. The "Phoenix gate" circuit has the advantage of ability to drive higher capacitive loads from a lower output impedance at slightly higher speeds, but this needs to be balanced against the disadvantage of higher power dissipation. Notice that Series 54/74 employs the "Phoenix gate" circuit at the one place in the line where it is really needed (for the power gate SN 5440).

The Sylvania "SUHL" gate is shown in Fig. 12. As one can see, in this configuration the diode that guarantees that the output transistors would be in opposite states, even during d.c. conditions, has been placed in the base of the top transistor; in this way, proper operation of the totem-pole output is insured, but the diode does not perform its current-limiting action during the switching transition. Also, with the diode placed in this position it will take longer to turn off $Q_1$, since the base charge removed from $Q_1$ will need to flow through the diode. The result will be that $Q_2$ will turn on quickly; but since $Q_1$ will turn off slowly, both transistors will be on for a longer time, thus allowing the surge current to flow for a longer time; at the speeds in the megahertz range this surge current would flow for a considerable percentage of the time and power dissipation would be higher.

4.5 Conclusions

At present, the logic family that seems to be the most adequate for the majority of projects is the TTL family; this is due to the fact that the multiple-emitter transistor is an economically feasible component, and that with this device more circuitry per area, hence per chip, can be attained. Thus the consequences are that with this family, complex logic arrays are feasible on a single chip and that faster speed can be obtained resulting from the lower capacitance associated with the smaller area. Further on, the TTL configuration employs a circuit which has a very low output impedance for high-capacity drive capability and high speed.

However, when using such a family we are aware of the problems that this type of family involves:

i) Oscillations. Due to the very fast edges typical of the TTL family, oscillations occur even with quite short lines.

ii) Power dissipation. When a TTL gate switches, the two output transistors are switched on simultaneously presenting a very low resistance between $V_{CC}$ and ground. At this time there is a very large current flow. For this reason the power dissipation of a
TTL gate is much higher when switching at 1 MHz than it is in the d.c. condition; consequently, the power supply, \( V_{CC} \) conductors, and ground conductors must be designed according to the highest frequency figure.

iii) Noise. The high current pulses which flow as the gates switch cause noise voltage spikes on the \( V_{CC} \) and ground lines, and this can be sufficient to cause the gates to switch. The high current pulses are inductively coupled to signal lines which also may cause undesired switching.

iv) Logic efficiency. The push-pull output gate makes it impossible to use a wired-OR configuration which typically reduces the element count by 15-20%.

v) Input extension. The fan-in of TTL elements is achieved by adding multi-emitter transistor arrays at the fan-in extension point; as two connections between the extender transistor and the gate are required, printed circuit layout is rather complex. Also the TTL extender adds capacitance at a high impedance point in the circuit where capacitance increases the switching times very significantly.

5. SEMICONDUCTOR CIRCUITS AND MODULAR PACKAGING

5.1 The use of plug-in modules

For the past decade or so, the majority of complex ground and shipborne electronic equipment has been constructed from discrete components, mounted on plug-in modules, and assembled in racks or cabinets. Plug-in modules became popular due to cost saving and ease of maintenance: the cost saving begins with a reduction in engineering time. Because of versatility of plug-in modules, they can be used for many functions in several systems that may be in the process of design or production. Cost saving continues into the production area, as the plugable capability of the modules enables the equipment to be built as a parallel instead of a series programme, normal with unitized construction. A parallel programme of assembly reduces the assembly space and inventory cost by reducing the assembly time.

When semiconductor integrated circuits first became available in production quantities, they were used in systems for aerospace computers such as A.C. Spark Plugs "Magic", North American's "Monica", and Librascopes "L 90" where their minute size could be taken advantage of, regardless of cost. In these aerospace systems, microminiaturization was of prime importance, and the equipment was therefore of unitized construction. In the next design phase we saw attempts at modularization beginning with the Univac "1284" and the Martin-Marietta "Martac 420". These two systems both used modules connected permanently in the equipment. The third phase, that brings us up to the state-of-the-art, is the packaging of integrated circuits based upon the use of plug-in modules, thus incorporating the advantages of a new technique with that of an established concept of proven worth.

5.2 Packaging dominates cost

The major barrier to full utilization of the advantages of integrated circuits is packaging: the technology of protecting, connecting, cooling and housing the circuits.

Monolithic IC's are now cheaper than the discrete component circuits they replace, but the packaging usually costs as much, if not more, than the IC's themselves. If the
individual circuit packages are considered as part of the system hardware, which they rightly are, then the packaging is the only significant cost. In the past, circuit costs predominated, and designers aimed at reducing the number of discrete components; today, the cost of individual components in an IC is negligible. In other respects, packaging offers the best chance to benefit from improved design: smaller size and weight, shorter signal paths, better reliability through improved cooling, and fewer mechanical contacts, and welded or soldered joints.

5.3 Basic packaging decisions

With IC, the minimum assembly level shifts upward from the circuit component to the circuit function. But the use of IC's has not changed the basic packaging design approach in which the system is broken down into smaller, manageable sections. A definition of these sections which has proved useful in IC system packaging is:

Level I: a logical function module of interconnected circuits;
Level II: a sub-system of interconnected level I modules that usually are easily replaced;
Level III: a system of level II modules; interesting figures for the packaging efficiency on these levels can be obtained by calculating the number of packages per square cm of mounting area, or per cubic cm or m of volume. The old formula, components per cubic cm, is difficult to use because the integrated equivalents of discrete components may not be clearly defined.

The three-level approach requires decisions on the type of circuit package and the method of joining the leads to the interconnections at level I, the optimum size of the modules, and the number of their input-output connectors and module interconnection. These decisions are affected by the factors previously discussed, and involve numerous trade-offs.

5.4 Integrated circuit package styles

The first major step is selecting the circuit package style. This, of course, is influenced by all the design requirements: size, weight, power, speed, maintenance philosophy, factory handling, cooling medium, etc.

The packaging designer now has three general form factors from which to choose:

5.4.1 Flat packages

These are small cases with radial leads. Flatpacks are usually rectangular, but round ones are sometimes used when a large number of leads are needed.

Their strong points are: the reduced height reduces system volume; the form factor is efficient for three-dimension packaging, the heat-transfer surface is accessible for conductive cooling.

This packaging is very popular whenever minimum use of space is needed.

5.4.2 TO packages

These resemble transistor cans but have more leads. Their advantages are: lower cost than flatpacks and better hermetic seal (the industry's long experience in making circular metal-to-metal seals customarily results in a seal that is roughly ten times as good as in the other package forms). For this reason, this package has occasionally been selected for satellite equipment.
5.4.3 Dual in-line packages

These were introduced more recently to suit non-military applications where minimum design and assembly costs are more important than minimum size, weight, and ability to withstand severe environments. The in-line packages have vertical leads spaced 0.1 inch apart, twice the spacing of flatpack leads. This relaxes the requirements for printed circuit precision and has a number of other cost-cutting advantages on the production line.

5.5 Component interconnection techniques

The methods which may be used to interconnect ICP's to printed circuit boards can be summarised as follows:

|-------------------------------|------------------------|----------------|-------------|--------------------------------|-----------------|--------------|----------|----------------|-------------|---------------|-----------------|------------|--------------|-------------|---------|------------------|-------------|

The electron beam and laser welding are relatively new and are not generally used at this time. Dip soldering was an obvious first choice for flatpack-lead bonding, but the attempts were usually unsuccessful. There were difficulties with lead forming; joints in printed circuit boards became solder-starved because a ribbon in a round hole leaves a large void which the capillary action of the molten solder often could not fill; temperature shock often damaged the integrated circuit or the package seal.

Lap soldering with a hand iron requires a skilled operator. Since the iron-tip temperature must be about 300°C to melt 60-40 solder, great care must be taken to prevent board delamination or heat damage to the integrated circuits.

Reflow soldering alleviates the problem; just the right amount of solder is pre-placed at the joint by use of pre-forms or solder cream, or by tinning the conductors. The heat that is applied to reflow the solder, thus forming the joint, can be controlled. As the project progresses into even small productions, it is almost mandatory to use automatic soldering methods.

5.6 Best module size

Establishing the size for the basic logic module is the most critical decision, as conflicting requirements of reliability and maintenance must be balanced.

5.6.1 Compactness

Apart from the mainly military requirements for small computers for use in aircraft and vehicles, the compact construction possible with solid-state elements results in shorter
connections and therefore faster operation of the equipment.*).

5.6.2 Reliability

The tighter one tries to pack the circuits, the higher the power and connection density, which means lower reliability and increased costs. An integrated circuit is inherently more reliable than a discrete component circuit; however, careful thermal management is needed because studies indicate that circuit life drops 20% to 50% for each 10°C rise in temperature over 25°C. Microscopic joints and conductors are difficult to make perfectly, and new interconnection techniques are not fully proved.

As reliability or mean-time between failures in the system increases, a surprising problem arises: maintenance calls become so rare that it is impractical to train troubleshooters. It may be cheaper to build the system with modules and throw them away when they fail.

5.6.3 Spare logistic

A large module improves reliability and maintenance, but the larger the module the more likely it is to be unique. If all modules are unique, 100% stocking of spares is necessary, and the designer cannot be sure that the same circuits, with known reliability and characteristics, will remain available in years to come. There is therefore a trade-off between making modules large for reliability, and keeping them small for interchange.

5.6.4 Speed

Circuits are getting faster due to new processing techniques. A 10 nssec circuit delay was once considered fast; now 5, 1, and even fractions of nanoseconds are being announced or discussed. The main reason is that chip size and propagation path-lengths are minute. Computers with clock rates of 25 to 100 Mc become feasible. Now the speed limitation becomes the length and characteristics of the wiring outside of the chip. The interconnection inductance and capacitance becomes part of the circuit. Simple wire must be replaced with transmission lines, aggravating the packaging problem and increasing interconnection volume. With higher speed, it becomes necessary for the location of circuits in the system, the delays in the wiring, and the cross-talk to be considered in the system, interconnection, and packaging design.

5.7 Throw-away module cost

Another factor significant to the module size is whether the modules which fail in use are to be thrown away or repaired. In the past, $50 has been a widely accepted throw-away cost. As the circuits' reliability and their mean-time between failures (MTBF) rise, the

*) This is particularly true when high-speed circuits are used, for then the capacitance and the inductance of the wiring have a more pronounced effect in determining the overall speed of the equipment. In order to charge up quickly the capacitance of the wiring, large currents are required. Large currents result in high power dissipation, give trouble due to the inductance of the wiring, and cause increased cross-talk and noise. Thus it becomes necessary to treat long interconnections as transmission lines and terminate them correctly. How long the interconnections have to be before this becomes necessary, depends upon the speed of the circuits. With edge speeds of a few nanoseconds, the inductance of even a few inches of wire can give trouble. Transmission lines need not be terminated, however, unless the propagation time of electromagnetic waves down these lines is comparable to the delay through an element; this is about 20 cm or so for an element with a propagation delay of a few nanoseconds.
cost can be higher; 1/100 is now being discussed. One approach that is gaining favour is to establish a figure of merit based upon operating hours per dollar for an assembly. One figure quoted is \( \frac{1}{100} \) per 10,000 hours. Monolithic IC failure rates are about 0.002% per thousand hours at present; 0.003% is anticipated in the near future, and 0.001% is reasonable for long-range planning. To this must be added joint and interconnection failure rates. This is 0.00001% per joint or 0.0002% for the average IC interconnection of 20 joints. Thus the designer can plan on a failure rate of 0.0032% for each assembled IC.

Therefore, with

\[
\lambda = \text{failure rate in \% per 1000 hours per connected integrated circuit} = 0.0032\%/1000 \text{ hours}
\]

for a module containing one integrated circuit, the mean-time between failures (MTBF) will be

\[
MTBF = \frac{1000}{0.000032} = 31,250,000 \text{ hours}.
\]

Furthermore, if we admit that the probability of failures in a module equals the sum of the failure probabilities of integrated circuits mounted on it, it is obvious that for a module with \( N \) circuits the probability will be \( N\lambda \), so that in general

\[
MTBF = \frac{1000}{N\lambda}.
\]

The value of MTBF that can be obtained varies with \( N \), decreases very rapidly as \( N \) increases.

Now, if a throw-away cost of \( \frac{1}{100} \) per each 10,000 hours of operation becomes a maintenance-cost rule, permissible module prices can be calculated with the following expression:

\[
C_{TM} = \frac{MTBF}{10,000} = \frac{10}{N\lambda}.
\]

The allowable price per integrated circuit in the module is inversely proportional to the number of circuits; hence

\[
C_{TC} = \frac{C_{TM}}{N} = \frac{10}{N^{\lambda}}.
\]

From this last expression we can easily find that for \( N > 20 \) the allowable price per IC is much lower than the actual price, which means that for modules with more than 20 IC it becomes convenient to repair eventual faults.

On the other hand, reliability considerations (MTBF = 1000/N\( \lambda \)) advise against increasing the number of IC per module.

5.8 Input/output connector

Circuit-type modules, in which circuit leads are brought out to edge connectors for interconnections, are widely used in discrete component equipments. This is efficient
because a plug-in card has only enough room for a few circuits, and use of such cards standardizes sub-assembly fabrication. It also permits easier maintenance, since only a few types of cards must be stocked as spares; technicians can readily repair such circuits with hand tools.

Circuit-type modules are little used in the new IC data-handling equipment. Large numbers of circuits can be placed on small cards, but even if each circuit lead could be brought out to the card edge, the edge could not carry enough connector pins. Cards would have to be tiny or the number of circuits on them low and interconnection hardware multiplied.

Instead, the functional approach is preferred. Circuits are interconnected in the module to form all or part of a sub-system. Fewer pins and less wiring and hardware are required. Also, it is easier to isolate a fault to a function than to an individual circuit. The rub is, that as the functional assemblies become larger and hence more efficient, the maintenance problems become more severe. The spare parts required for a small computer might be another computer, unassembled. Otherwise, field technicians would have to try to repair the modules on the spot. However, the spare parts problem becomes less severe as the system becomes larger. The possibility of repeated use of one circuit of the same type increases, and this can be helped along by dividing the larger functions among several modules. However, this is still difficult to achieve in practice.

5.9 Module interconnection techniques

The type of wiring usually depends upon the wire terminating methods which are as follows.

5.9.1 Poke-home connectors

These are miniature connectors whose pins look into place when they are inserted into the connector body. One or two wires can be fastened to a pin so that long, daisy-chain wiring assemblies can be tied together in advance.

5.9.2 Wire wrap

Wrapped wire connections were pioneered by the Bell Telephone Laboratories, Inc. The wiring routes can be programmed during design, and the wiring done automatically with wire-wrap machines made by the Gardner-Denver Co.

5.9.3 Termination

This product of AMP, Inc., is a small spring-clip that forces the wire into intimate contact with a post. The properties of the joint are similar to wire wraps. Its advantages are: the wire can be stranded; a clip at the bottom of a post can be snapped off and a new one added to the top of the post, forcing the higher pins down the post; the terminations can be made more quickly.

6. THE DEVELOPMENT OF AN IC LOGIC MODULES SERIES

Whenever an IC Logic Modules Series is going to be developed, the main objectives are:

i) to isolate, design, package, and interconnect complete major system elements;

ii) to maintain regularity and simplicity at all levels for logic, circuits, packaging, and records;
iii) to use systematic procedures in order to remove the need for unnecessary human decisions whenever possible.

Figure 13 shows the diagram of the fundamental steps necessary to meet the above-mentioned objectives.

1) The project definition and scope are set.
2) From all the available background knowledge, specific techniques are selected.
3) A detailed system specification is developed, spelling out major functional elements, performance circuit, and package specifications, etc.
4) From the detailed system specifications, design tasks are outlined and assigned. Logic flow-charts are developed and co-ordinated.

In any data-handling system, the circuit requirements generally fall into one or more of the following categories:

a) **Bulk memory circuits.** This group includes all circuits required to store and access information in the memory cells of the basic memory.

b) **Volatile memory circuits.** These are primarily flip-flops or equivalent circuits employed to accept, store, or transfer information within the system.

c) **Logic circuits.** Logic circuits provide all decision-making functions, and generally include circuits to increase fan-in and fan-out or restore logic levels.

d) **Pulse circuits.** In this category are found the clock pulse generators or similar-type circuits whose fundamental purpose is to provide time control signals to the flip-flop and logic circuits.

e) **Input/Output circuits.** This group includes circuit functions which enable the system to communicate with associated equipment and/or an operator.

5) The circuit family is chosen, and the logic design and wiring rules developed.
6) The package standards are detailed specifically to match the functional breakdown and implementation rules.
7) After logic specifications are set, a logic diagram is made.
8) From the logic design, a layout of a matrix of the interconnections is made. As the layout is made on a standard printed vellum, no dimensions or critical tolerances need be considered by the draughtsman. The layout vellum provides for one plane of essentially horizontal, and one plane of essentially vertical interconnections.
9) The draughtsman makes the horizontal and vertical interconnections artwork by directly taping each on to stable plastic placed over the layout. The artwork is then checked back to the original logic to ensure that final interconnections match the design exactly, before any parts are made.

10) The artwork is photographed and a printed circuit board is made.
11) The printed circuit board and the components are assembled for test and debugging. Design changes are incorporated by scratching out printed circuit lines and/or adding wire jumpers. After testing, the working unit is returned, and both the logical design and the artwork are changed. The artwork is then re-photographed and a new board is substituted for the old one. At each completed design phase the logical design, together with the properly labelled negatives of the artwork, become a master record for both the change level status and the production wiring master.
**PROJECT DEFINITION**
Performance Environment

**TECHNOLOGY AVAILABLE**
Logic manufacturing Packaging components

**DETAILED SYSTEM SPECIFICATIONS**
Diagrams Performance Interconnections Type of logic
Packaging Power Environment

**DESIGN TASKS**
- MEMORY CIRCUITS
- LOGIC CIRCUITS
- PULSE CIRCUITS
- IN/OUT CIRCUITS
- POWER SUPPLY

**IC. AND COM.**
IC PACKAGE STYLE WIRING RULES

**PACKAGE SP.**
- BOARD SIZE
- LEAD JOINT SYSTEM
- PRINTED CIRCUIT
- SOLDERING SYSTEM
- ARTWORK RULES
- CONNECTORS

**LOGIC SPECIFICATIONS**
LOGIC DIAGRAM
LOGIC LAYOUT

Check Production master

**ARTWORK**

**P.C. BOARD**

**TESTS**

Fig. 13 FUNDAMENTAL STEPS FOR MODULES DEVELOPMENT
PART II

THE CHARACTERISTICS OF THE INTEGRATED CIRCUIT LOGIC

MODULES SERIES
PART II
THE CHARACTERISTICS OF THE NPA INTEGRATED CIRCUIT LOGIC
MODULES SERIES

1. GENERAL DESCRIPTION

NPA integrated circuit logic modules are monolithic integrated circuit assemblies supple-
mented by some discrete hybrid combinations mounted on 110 x 90 x 1.6 mm glass-impregnated
epoxy cards.

NPA circuit logic modules have already been used as the building blocks for NPA-MOLE
(Measuring On-Line Equipment). Their design thus ensures reliable operation, even in the
adverse large-system environment of electrical noise resulting from electromechanical de-
vices, long signal and power supply leads, ground loops, and power supply surges.

The cards are designed to provide grouping of gates and logic functions that are most
commonly used in the implementation of general purpose logic configurations.

The series now includes 19 modules. The logic functions range from basic NAND gates
to D and J-K flip-flops. Functional modules include: four-bit binary comparator; parity
generator; six-bit shift register; sync. Up/Down BCD counter. Special circuits include:
integrating multivibrator; monostable multivibrator; transmitter; receiver; input logic
level converter; output logic level converter.

While the basic logic functions are performed by integrated flip-flops and gates, many
of the peripheral circuit functions cannot be conveniently performed in this way. For
such requirements, hybrid or discrete component circuits are used. They are fully silicon,
operated from the same single voltage as integrated circuits, and are packaged on similar
modules.

2. MECHANICAL FEATURES

2.1 Base material

The base material for all the modules is the Stratibol glass-epoxy G 10, 1.6 mm thick,
double-sided copper-coated; the copper coat is 35 μ thick, which corresponds to 1 oz.

2.2 Physical size

The dimensions of the glass-impregnated epoxy cards are 90 x 110 x 1.6 mm.

Up to ten 16-lead dual in-line IC can be mounted on a single board. The complete board
outline is shown in Fig. 14.

2.3 Connector characteristics

All boards feature a 44-pin finger-strip connector with gold plate over nickel base.
All modules have standard pins for the ground and power supply connections. Namely, pin 44
is used for ground, pin 41 for +5 V and, when necessary, pin 1 for -5 V.

2.4 IC packaging

The integrated circuit family used throughout features dual in-line packages.
2.5 The soldering system

The method that has been used to connect the components to the printed circuit boards is the ZEWA drag soldering system. The main advantages of using this automatic soldering system are:
- quick adaptability to any soldering task;
- bridge-free soldering even of very close circuitry;
- little or no uneven solder build-up on conductors or large copper areas;
- consistently good soldering quality, independent of the influence of operating personnel;
- high number of soldering operations per hour (roughly one hundred NPA standard boards/hour).

3. PRINTED CIRCUIT CHARACTERISTICS

3.1 Artwork characteristics

The layout of the printed circuit, commonly referred to as "artwork", has been done (with the exception of the discrete component boards) keeping in mind a certain number of rules:
- Holes have been located with a regular spacing: the draughtsman is allowed to choose the most convenient component locations.
- All integrated circuits have been oriented on the same axis.
- To take full advantage of the dual in-line package, conductors can run under the integrated circuit cases.

Figures 15 and 16 show the typical configurations for the artwork both for the component side and the wiring side.

3.2 Conductor characteristics

The following cross-section shows the characteristics of the conductor adopted for all the printed circuits:

```
1 μ gold plating
5 μ nickel
15 μ copper
1,5 μ chemical copper
35 μ base copper
```

As shown in the cross-section, the conductors are gold-plated; in fact, gold solders well and in addition provides a low resistance surface which is very suitable for the finger-strip connector. The use of gold-plated conductors thus makes it possible to have one type of plating over the entire circuit board conductor surface.

The minimum width of a conductor is 0.5 mm, and the minimum spacing between two conductor centres is 1.27 mm. For the reasons mentioned above, the characteristics of the 44-pin finger-strip connector are the same as those of the conductors.
Fig.16  ARTWORK  (wiring side)

All dimensions in mm - in brackets in inches.
3.3 Plated-through holes

Plated-through holes are the most advanced method of electrically connecting double-sided printed circuits. Holes are drilled through the laminated assembly and the interior of the holes plated to join the conductors on the two layers.

The plating of the holes has the following characteristics:

- 15 μ copper
- 5 μ nickel
- 1 μ gold

The minimum hole size is 0.8 mm.

4. CONNECTOR CHOICES

The board 44-pin finger-strip connector has been dimensioned so that three different connectors can be used.

4.1 Winchester connector

All boards fit in a Winchester solder-pin connector; namely the HBD 22, which is a light entry type with double termination for 1/6" thick printed circuit board on 0.156 contact centres.

4.2 UECL connector

All boards are compatible with the UECL Series 10WA printed wiring connector 305660A2222. This solder-pin connector is in the CERN stock.

4.3 AMP connector

The board finger-strip connector matches also with the AMP Termi-Twist connector 67031-1. This connector features a phenolic housing and high performance bifurcated contacts. This is a one-piece printed board-edge connector designed primarily for wiring with Termi-Point wiring devices.

Physically, the technique is a compression termination method that employs a phosphor-bronze spring clip, the wire to be applied, and a rigid metal post. The clip acts as a holding device and is not to be confused with crimped terminals. Instead, the clip is precision engineered so as to position and then grip the wire as it is affixed to the post by hand or automated tooling.

Terminations are gas-tight, and can be disconnected easily using hand tools without electrically disturbing adjacent terminations on the same or on other posts. Because the complete procedure—stripping and terminating—is accomplished in application, significant savings both in time and labour are realized.

The terminal posts are rectangular-shaped and specially plated for a low coefficient of friction; the post, although specifically designed for Termi-Point clip applications, can be wrapped, welded, or soldered.

The phosphor-bronze pressure clip is such that it acts as a memory spring device, holding the termination at a pressure close to the yield point of the wire.
5. TESTS AND COSTS

All boards are semi-automatically tested with the help of a Test Station that has been developed in the NPA Electronics Laboratory.

The cost of the boards is relatively low as it ranges from 50 SP to 100 SP per assembled module. This result has been achieved using cost-saving procedures at all the stages of development: the dimensions of the board are such that the artwork development is relatively simple; the specifications for the printed circuit have been set, keeping in mind good quality but also costs; the automatic soldering system saves a great deal of manpower.

6. ELECTRICAL CHARACTERISTICS

6.1 The integrated circuit family used

NPA integrated circuit logic module series employs Transistor-Transistor-Logic Texas Instruments Semiconductor Networks in a molded plug-in package; in fact the Series 74 N consists of the Series 74 general purpose TTL circuits mounted within a 14-pin plastic package and characterized for operation over the temperature range of 0°C to 70°C.

The main features are:

- typical propagation delay-time/gate: 13 nsec;
- typical propagation delay-time/flip-flop: 30 nsec;
- typical d.c. noise margin: 1 V;
- power dissipation/gate (50% d.c.): 10 mW;
- output impedance at logical 1 output state: 100 Ω.

6.2 System speed

The NPA integrated circuit logic modules are guaranteed for operation at frequencies up to 6 MHz, unless otherwise noted. This is a typical value, as specific modules can operate at higher frequencies depending on the number and the type of cascaded logic elements.

Glossary

- \( t_{r} \) RISE-TIME: is the time delay between the 10% and 90% points of a voltage swing from 0 V to +3.6 V nominal levels.
- \( t_{f} \) FALL-TIME: is the time delay between the 10% and 90% points of a voltage swing from +3.6 V to 0 V nominal levels.
- \( t_{pd} \) PROPAGATION DELAY: is the propagation delay time measured from the switching point of the command signal (+1.5 V) to the switching point of the output signal (+1.5 V) in the output transition from logic "1" to logic "0".
- \( t_{pu} \) PROPAGATION DELAY: is the propagation delay time measured from the switching point of the command signal (+1.5 V) to the switching point of the output signal (+1.5 V) in the output transition from logic "0" to logic "1".
- \( t_{p} \) CLOCK PULSE DURATION: is the duration of the clock pulse measured at the switching points (+1.5 V).
\( t_{su} \) SET UP TIME: is the minimum time prior to clock switching point (+1.5 V) when the input signal is required to become stable.

\( t_{h} \) HOLD TIME: is the minimum time after the clock switching point (+1.5 V) during which input signal is required to remain stable.

**Effects of Input/Output Connections on Gate Speed**

a) **Input**

The unused inputs of a TTL gate may be connected in three ways:

i) **Inputs parallel**

![Diagram](image)

Typical values

\[
\begin{align*}
  t_{pd_0} & = 8 \text{ nsec} \\
  t_{pd_1} & = 18 \text{ nsec}
\end{align*}
\]

Unused gate inputs are connected to used inputs.

**Advantage**: It is the fastest method of connection.

**Disadvantage**: The input current requirements will be multiplied by a factor of \( N \) if \( N \) is the number of parallel inputs.

ii) **Inputs open**

![Diagram](image)

Unused gate inputs are left open.

**Advantage**: It is the cheapest method of connection, because fewer connections are required. The input loading is the same as with one input.

**Disadvantage**: Referring to method (i), \( t_{pd_0} \) will increase by approximately 1 nsec/spare input, while \( t_{pd_1} \) will remain unchanged. Moreover, the high impedance of these input terminals might introduce noise more easily than other low impedance inputs.

iii) **Inputs on \( V_{cc} \)**

![Diagram](image)

Unused gate inputs are connected to power supply.

**Advantage**: It is a compromise solution between the methods described in cases (i) and (ii). The propagation delay is lower than in case (ii), but higher than in case (i).

**Disadvantage**: It restricts \( V_{cc} \) rating to 5.5 V max. Referring to method (i), \( t_{pd_0} \) will increase by approximately 0.5 nsec/spare input, while \( t_{pd_1} \) will remain unchanged.
b) **Output**

The effect of capacitive loading at the output is to increase both propagation delays. Namely, the increase of $t_{pd}$ is of 0.05 nsec/pF and the increase of $t_{pd}$ is of 0.1 nsec/pF.

---

**6.3 Nominal logic levels**

Positive logic will always be used. The logic levels are:

- $(2.4 - +3.6 \text{ V})$ HIGH LEVEL (H) $\rightarrow$ "1"
- $(0.0 - +0.4 \text{ V})$ LOW LEVEL (L) $\rightarrow$ "0"

The guaranteed voltage levels and the typical switching level (the level at which the input signal changes the output state) are shown in the figure.

---

**6.4 Loading factor and driving ability definitions**

In order to simplify the system design, input current requirement and output driving ability are defined in terms of unit loads (UL).

The **unit load** is the load represented by a circuit that causes the driver to supply a leakage current of about 40 μA in state "1" and to sink a current of about 1.6 mA in state "0". As a result:

i) **The input current requirement (loading factor)** of an input of a standard module is said to constitute $N$ unit loads for the driving circuit ($N = 1$ typically).

ii) **The output driving ability** of the output of a standard module is said to have the ability of driving $M$ unit loads ($M = 10$ typically)

---

**Unit load definition**

- **STATE "1"**
  - "DRIVING ELEMENT" with 40 μA
  - "LOAD" with 1 UL

- **STATE "0"**
  - "DRIVING ELEMENT" with 1.6 mA
  - "LOAD" with 1 UL
Fig. 17 Typical output characteristics of the standard TTL gate
The typical output characteristics of the standard TTL gate are shown in Fig. 17 and may be used when the load consists of circuits other than TTL logic circuits.

6.5 Noise immunity

6.5.1 Direct noise immunity

For all the modules of the series, unless otherwise noted, the output of a gate switches from a logical "one" to a logical "zero", or conversely when the input voltage reaches about +1.5 V.

Since the input voltage is given at standard TTL levels, i.e. it will be no lower than +2.4 V in "1" status and no higher than +0.4 V in "0" status, this means that the gate input may experience a voltage of one volt higher than the logical zero limit and still not false-trigger; hence the series features a one-volt d.c. noise margin typically.

6.5.2 Absolute worst-case noise margin

While the d.c. noise margin guarantees that the gate will not switch logic levels when noise is applied, the absolute worst-case noise margin guarantees that the voltage at the output of a gate is higher than +2.4 V in state "1" and lower than +0.4 V in state "0" while the noise voltage is applied.

The characteristics of Series 74 N (Fig. 18) are such that the gate output is at a voltage higher than +2.4 V (in worst-case conditions) when the input is at a voltage lower than or equal to +0.8 V, and that the gate output is at a voltage lower than +0.4 V when the input is at a voltage higher than or equal to +2 V.

This means that when a Series 74 N gate is driving another, the output of the first (driving gate) can experience either a 400 mV negative perturbation from a logical "1" or a 400 mV positive perturbation from a logical "0", and still the resulting voltage at the input of the gate being driven will not be less than the guaranteed test condition of 2.0 V (status "1"), or more than 0.8 V (status "0").

It can be said that the Series 74 N has an absolute worst-case noise margin of 400 mV.

6.6 Timing

6.6.1 Type of flip-flop

According to their characteristic equation, the flip-flops may be classified in various types. We consider clocked flip-flops, whose content may change only at fixed intervals of time determined by a clock generator.
SR type (Set/Reset):

Truth table

<table>
<thead>
<tr>
<th>( t_n )</th>
<th>( t_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>( Q_n )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>?</td>
</tr>
</tbody>
</table>

Characteristic equation \( Q_{n+1} = (S \bar{R} Q)_n \)

N.B. \( t_n \) is time before bit time, 
\( t_{n+1} \) is time after bit time.

D type (Delay):

Truth table

<table>
<thead>
<tr>
<th>( t_n )</th>
<th>( t_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Characteristic equation \( Q_{n+1} = D_n \)

JF type:

Truth table

<table>
<thead>
<tr>
<th>( t_n )</th>
<th>( t_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>J</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>( Q_n )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>( \bar{Q}_n )</td>
</tr>
</tbody>
</table>

Characteristic equation \( Q_{n+1} = (K Q + J \bar{Q})_n \)

"
Fig. 18 Typical d.c. margin and voltage transfer characteristics
6.6.2 Entry of information

The information carried out at the flip-flop input terminals may enter at the leading edge or at the trailing edge of the clock pulse. Also the clock triggering may be d.c. coupled or a.c. coupled, depending on the input circuitry.

A special way for entering information is based on the master-slave principle.

Actually as shown below, the master-slave flip-flop is formed of two flip-flops, the first one called the Master, the second one the Slave.

This device has AND gate inputs for entry into the master section which are controlled by the clock pulse.

The clock pulse also regulates the state of the coupling gates which connect the master and the slave sections.

The sequence of operations is as follows (refer to the figure below).

1) Isolate slave
2) Enter information to master
3) Isolate master
4) Enter information to slave

![Fig. 19]
Entry of information in a master-slave flip-flop

The main advantage using master-slave techniques is that it is independent of clock rise-time, fall-time, and speed. A sine wave, or any other wave shape having distinct low and high levels, is a reliable trigger.

The master-slave is obviously trailing-edge triggered.
6.6.3 TTL triggering characteristics

a) SN 7470 JK flip-flop

This is a type JK flip-flop.

**Triggering**

Direct-coupled clock triggering; information is transferred to the outputs on the positive edges of the clock pulses; information must be stable at least 20 nsec prior to clock transition (1.5 V, standard TTL switching point), i.e., $t_{su}$ must be $\geq$ 20 nsec; minimum clock-pulse width must be $\geq$ 20 nsec; clock rise-time must be between 5 and 150 nsec; minimum input hold-time (i.e., minimum time from clock transition before input can change) is 5 nsec.

![Fig. 20 SN 7470 JK switching waveforms](image)

**Recommended conditions**

$$
\begin{align*}
\text{t}_{su} & \geq 20 \text{ nsec} \\
\text{t}_p & \geq 20 \text{ nsec} \\
\text{t}_{pd0} & = 50 \text{ nsec} \\
\text{t}_h & = 5 \text{ nsec} \\
\text{t}_r & = 5 \text{ to } 150 \text{ nsec}
\end{align*}
$$

b) SN 7472, SN 7473 (Dual)

This is a type JK flip-flop.

**Triggering**

Master-slave. Information is transferred to the outputs on the negative edges of the clock pulse (trailing edges). Information must be stable during the time the clock pulse
is higher than the switching level of 1.5 V. The hold time \((t_h)\) must then be equal or higher than applied clock-pulse width.

The minimum clock-pulse width is 20 nsec.
The propagation delay is 35 nsec typically.

\[
\begin{align*}
\text{INPUT J or K} & \quad \{ \begin{align*}
2.4 \, V \\
1.5 \, V \\
0.4 \, V \\
2.4 \, V \\
1.5 \, V \\
0.4 \, V
\end{align*} \}
\end{align*}
\]

\[
\begin{align*}
\text{CLOCK} & \quad \{ \begin{align*}
2.4 \, V \\
1.5 \, V \\
0.4 \, V
\end{align*} \}
\end{align*}
\]

\[
\begin{align*}
\text{OUTPUT} & \quad \{ \begin{align*}
2.4 \, V \\
0.4 \, V
\end{align*} \}
\end{align*}
\]

\[
\begin{align*}
\rightarrow t_h \\
\rightarrow t_p \\
\rightarrow t_{pdo}
\end{align*}
\]

\textbf{Fig. 21 Master-slave switching characteristics}

\textbf{Recommended conditions}

\[
\begin{align*}
t_p & \geq 20 \, \text{nsec} \\
t_h & \geq t_p \\
t_{pdo} & = 35 \, \text{nsec typical}
\end{align*}
\]

\textit{Note:} If clock rise-time is not derived from standard TTL series, flip-flops SN 7472-73 will behave as Set/Reset master-slave flip-flops.

c) \textbf{SN 7474 (Dual)}

This is a type D flip-flop.

\textbf{Triggering}

Edge triggering. Information is transferred to output on the positive edge of the clock pulse.

Information must be stable at least 20 nsec prior to clock transition (1.5 V standard TTL switching point), i.e. the set-up time \((t_{su})\) must be higher than 20 nsec.

Clock-pulse width must be higher than 30 nsec.

Minimum input hold-time (i.e., minimum time from clock transition before input can change) is 5 nsec.
Fig. 22 SN 7474 D flip-flop switching characteristics

Recommended conditions

- $t_{su} \geq 20$ nsec
- $t_p \geq 30$ nsec
- $t_{pdo} = 50$ nsec
- $t_h \geq 5$ nsec

6.7 Power supply requirements

The logic module series is intended for operation with a power supply of +5 V. In order to eliminate the need of protective resistances when connecting unused inputs to high signal, the voltage range must be limited to +5 V. Certain auxiliary and input/output types use, in addition, a -5 V bias.

All modules have standard power and ground input connections; these pins on opposite edges of the card permit busbar distribution of power and ground to all cards in a panel. Power and ground pins of all the elements on a board are prewired with laminated copper and glass-epoxy distribution lines. The copper and glass planar arrangement should permit maximum decoupling of spurious signals from power and ground lines.

All modules include RC low-pass filters for the power supply.

6.8 Temperature range

The operating temperature range for the series is 0°C to +70°C; storage conditions cover the temperature range of -55°C to +70°C.

The cards are designed for self-convection cooling up to +50°C; however, forced air-cooling is recommended in case of obstructed air access and local heat sources.
6.9 Grounding and power distribution rules

A significant percentage of logic system problems have been caused by some form of digital "noise". They require a good deal of time for correction due to their intermittent nature, and the following discussion describes the techniques which will greatly reduce the probability of similar problems in logic system.

6.9.1 Digital ground system

Most noise problems are a result of differences in potential between the various digital "grounds" within the system. These potential differences are generally in the form of "spikes" or "grass", and are the results of pulse current flowing in the ground structure. The logic system designer should observe the following rules in order to minimize noise problems:

i) All logic trays should have a 1-inch braid as the digital ground connection from the tray ground-bus to the system digital ground bus.

ii) The system digital ground-bus should have a minimum cross-section equivalent to 1-inch braid. In most cases, a larger copper bar is mechanically most convenient. The ground terminals of the digital power supplies are considered as the origin of the bus.

iii) Every effort should be made to minimize the number of intertray logic connections required. These connections are the source of most of the high-frequency current that flows in the ground structure.

iv) System layout should be planned to make the digital ground system as compact as possible. Those trays which represent the largest loads should be placed closest to the power supply, if this is feasible. The ground braids from the trays should be connected together at the closest point. It is not advisable to run separate ground lines all the way to the power supplies from every tray.

v) Care should be taken to see that current returns from large pulse signals (such as that required to drive a long string of shift registers) do not flow in the main ground system. This is especially important when signals are being routed through cable retractors.

vi) Equipment, such as tape transports that have chassis and signal ground (or shield ground) in common, requires some special attention. The head cable shields and the start-stop command are returned to chassis. It may be most convenient to lift these chassis connections, but it is also possible to eliminate most problems and retain the chassis grounds.

6.9.2 D.c. power distribution

If the preceding rules on grounding are followed, power distribution problems are minimized. The following rules should also be observed for power distribution.

At the currents normally encountered with NPA circuits, the inductance of interconnecting wiring is of more significance to signal lines than to wire resistance. However, for +5 V wiring it is important that the d.c. resistance be low enough to prevent excessive voltage drops and resulting reduction signal levels because of the reduced supply voltage.
The current-carrying capacity of a wire is limited by the permissible temperature rise; the following diagram is a table of recommended maximum current for various sizes of stranded wire in free air based on 105°C vinyl insulation with a temperature rise of 10°C at the wire surface.

<table>
<thead>
<tr>
<th>Stranding</th>
<th>Size</th>
<th>Current (A)</th>
<th>ΔV (mV/foot) at 20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-36</td>
<td>28</td>
<td>1.5</td>
<td>89</td>
</tr>
<tr>
<td>7-34</td>
<td>26</td>
<td>2.5</td>
<td>93</td>
</tr>
<tr>
<td>7-32</td>
<td>24</td>
<td>3.5</td>
<td>83</td>
</tr>
<tr>
<td>7-30</td>
<td>22</td>
<td>5</td>
<td>74</td>
</tr>
<tr>
<td>7-28</td>
<td>20</td>
<td>7</td>
<td>65</td>
</tr>
<tr>
<td>19-31</td>
<td>18</td>
<td>9</td>
<td>61</td>
</tr>
<tr>
<td>19-29</td>
<td>16</td>
<td>12</td>
<td>51</td>
</tr>
<tr>
<td>19-27</td>
<td>14</td>
<td>15</td>
<td>40</td>
</tr>
<tr>
<td>19-25</td>
<td>12</td>
<td>20</td>
<td>34</td>
</tr>
<tr>
<td>19-23</td>
<td>10</td>
<td>21</td>
<td>29</td>
</tr>
</tbody>
</table>

The figure also lists the voltage drop per foot for each wire size at the recommended maximum current at 20°C; the drop will increase by approximately 20% at 75°C.

6.9.3 a.c. power distribution

Many systems are operated from power lines that are extremely noisy. The following rules will reduce the associated problems.

i) Line filters should be installed on all systems. The cases of the filters should be insulated from ground and a separate return to "dirty earth" provided.

ii) The a.c. power lines throughout the system should be routed so as to avoid coupling to either the ground system or the logic wiring.

iii) a.c. neutral should not be connected to ground anywhere in the system.
6.10 Glossary

The terms defined and explained in this glossary are used in describing the logic modules that are identified in the following section.

Fan-In : Maximum number of AND GATE outputs that can be used to drive an input.

Loading Factor : Amount of load imposed upon the sources supplying signals to the input.

Driving Ability : The number of unit loads that can be driven by the output of a circuit.

Module Dissipation : The values of the module dissipations are based on the typical power dissipation figures, at 50% duty cycle, given by TI for the 74 N Series and on laboratory tests.

Maximum Operating Frequency: Maximum repetition or clock rate at which the modules will perform reliably when in operation continuously, under worst case conditions, without special trigger pulse (clock) requirements.
### 6.11 SYMBOLOGY

<table>
<thead>
<tr>
<th>DENOMINATION</th>
<th>SYMBOL</th>
<th>BOOLEAN EXPRESSION (for positive logic)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND</td>
<td><img src="image" alt="NAND Symbol" /></td>
<td>$X = \overline{AB}$</td>
</tr>
<tr>
<td>EXPANDABLE</td>
<td><img src="image" alt="Expandable Symbol" /></td>
<td>$X = (AB) + (CD) + \overline{Ex}$</td>
</tr>
<tr>
<td>OR GATE</td>
<td><img src="image" alt="OR Gate Symbol" /></td>
<td>$Ex = ABCD$</td>
</tr>
<tr>
<td>D FLIP-FLOP</td>
<td><img src="image" alt="D Flip-Flop Symbol" /></td>
<td>$Q_{n+1} = D_n$</td>
</tr>
<tr>
<td>JK FLIP-FLOP</td>
<td><img src="image" alt="JK Flip-Flop Symbol" /></td>
<td>$Q_{n+1} = (KQ + J Q)_n$</td>
</tr>
<tr>
<td>MULTIVIBRATOR</td>
<td><img src="image" alt="Multivibrator Symbol" /></td>
<td></td>
</tr>
</tbody>
</table>
Acknowledgements

The authors wish to thank Mr. G. Castelli for the exhaustive tests carried out by him on the circuits, Mr. P. Genini for the development of various diagrams, and Mrs. D. Metral for the artwork layout of the circuits and the drawing of the diagrams.

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The authors also wish to point out that this work would not have been possible without the constant interest and support of Prof. G.A. Ramm.

***

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PART III

TECHNICAL SPECIFICATIONS OF THE MODULES
LOGIC DIAGRAM: 1.2
Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 1.3
Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 11
INTEGRATED CIRCUITS/MODULES: 3
INTEGRATED CIRCUITS USED: 2 × SN 7400 N
1 × SN 7410 N

LOADING FACTORS: PIN: 5,6,7,9,13,14,15,16,17,19,23,21
25,24,27,29,28,35,39,30,33,31,37,40,36
1 unit

DRIVING ABILITY: PIN: 8,10,14,12,18,20,26,22,34,32,38
10 units

POWER DISSIPATION/MODULE: 110 mW (typ.)

FUNCTIONAL DESCRIPTION:

FOR POSITIVE LOGIC:

\[ X = \overline{A \cdot B} \]

\[ X = \overline{A \cdot B \cdot C} \]

Eleven NAND gate circuits are contained in this module: three have three-term inputs; eight have two-term inputs. NAND circuits are used where maximum speed and/or the logical inversion of an AND function are required.

This card is specially suited for transfer gating.
2/3 IN GATE
Electric Diagram
NPA 231 G01 C
LOGIC DIAGRAM: 2.2

Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 2.3

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 6
INTEGRATED CIRCUITS/MODULE: 3
INTEGRATED CIRCUITS USED: SN 7420 N

LOADING FACTORS: PIN: 7,9,13,11,16,15,12,10,18,17,19,21, 26,28,25,22,30,29,31,33,38,37,35,34 1 unit

DRIVING ABILITY: PIN: 8,14,20,24,32,36 10 units

POWER DISSIPATION/MODULE: 60 mW (typ.)

FUNCTIONAL DESCRIPTION:

For positive logic:

\[ X = \overline{ABCD} \]

Each module contains six four-input NAND gates, which are useful for decoding and control. This card connects all gate inputs and outputs to connector pins providing the logic designer with maximum flexibility.
4 IN GATE
Logic Diagram
NPA 231 G02 B
4 IN GATE
Electric Diagram
NPA 231 G02 C
LOGIC DIAGRAM: 3.2
Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 3.3
Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 4
INTEGRATED CIRCUITS/MODULE: 4

INTEGRATED CIRCUITS USED: $4 \times SN\ 7430\ N$

LOADING FACTORS: PIN: $6, 8, 10, 3, 5, 7, 9, 12, 16, 18, 11, 3, 15, 17, 19, 20, 24, 21, 23, 25, 29, 27, 31, 26, 30, 32, 33, 39, 37, 35, 34, 38$ 1 unit

DRIVING ABILITY: PIN: $14, 22, 28, 36$ 10 units

POWER DISSIPATION/MODULE: 40 mW (typ.)

FUNCTIONAL DESCRIPTION:

FOR POSITIVE LOGIC:

![Logic Diagram]

$x = ABCDEFGH$

Each module contains four eight-input NAND gates, mostly useful for buffering and decoding.
8 IN GATE
Logic Diagram
NPA 231 G 03 B
8 IN GATE

Electric Diagram

NPA 231 G03 C
**LOGIC DIAGRAM** 4.2

Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

**ELECTRIC DIAGRAM** 4.3

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

**LOGIC FUNCTIONS/MODULE**: 8

**INTEGRATED CIRCUITS/MODULE**: 4

**INTEGRATED CIRCUITS USED**: 4 x SN 7440 N

**LOADING FACTORS**: PIN: 2, 4, 1, 3, 5, 10, 8, 14, 16, 9, 11, 11, 15, 13, 20, 25, 19, 21, 23, 27, 29, 28, 26, 35, 33, 31, 32, 37, 39, 38, 40

1 unit

**DRIVING ABILITY**: PIN: 6, 12, 18, 22, 24, 30, 34, 36

30 units

**POWER DISSIPATION/MODULE**: 212 mW (typ.)

**FUNCTIONAL DESCRIPTION**:

FOR POSITIVE LOGIC:

```
X = A B C D
```

Each module contains eight four-input power NAND gates, each of which may drive up to 30 standard loads. With this drive capability, these circuits are useful for common clock or reset distribution. They can also be used to minimize rise-time deterioration due to capacitive loading in applications where the signal distribution is extensive.
4 IN BUFFER
Logic Diagram

NPA 231 G04 B
4 IN BUFFER
Electric Diagram
NPA 231 G04 C
LOGIC DIAGRAM: 5.2

Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 5.3

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 1
INTEGRATED CIRCUITS/MODULE: 3
INTEGRATED CIRCUITS USED: 1 x SN 7453 N
2 x SN 7460 N
LOADING FACTORS/PIN: 11, 7, 9, 6, 8, 10, 14, 12, 23, 13, 15, 17, 21, 19, 22, 26, 39, 35, 33, 31, 25, 27, 29, 37
1 unit
10 units

DRIVING ABILITY/PIN: 16

POWER DISSIPATION/MODULE: 31 mW (typ.)

FUNCTIONAL DESCRIPTION:

FOR POSITIVE LOGIC:

\[ X = AB + CD + EF + GH + E1 + \ldots \]

Maximum Fan-in: 24

The module includes one Expandable Quad AND-OR-INVERT gate with both expander inputs brought to the connector and four four-input expanders to increase the fan-in up to 24.
H FAN-IN OR
Logic Diagram
NPA 231 M01 B
H FAN-IN OR

Electric Diagram

NPA 231 M01 C
LOGIC DIAGRAM: 6.2
Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 6.3
Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 4
INTEGRATED CIRCUITS/MODULE: 3
INTEGRATED CIRCUITS USED: 2 × SN 7450 N
1 × SN 7460 N
LOADING FACTORS: PIN: 5, 7, 10, 11, 15, 17, 19, 24,
23, 25, 29, 31, 35, 37
1 unit
DRIVING ABILITY: PIN: 20, 26, 32, 36
10 units
POWER DISSIPATION/MODULE: 66 mW (typ.)

FUNCTIONAL DESCRIPTION:
This card contains four independent exclusive OR gates that can be used for sensing the exclusive OR and the equality of two inputs. The basic exclusive OR configuration finds application in comparators, adders, and parity generators. Two exclusive-OR are expandable (the board contains two expanders) to permit the formulation of wider input configurations.
QUAD EXCL OR WITH EXP.

Logic Diagram

A

B

C

NPA 231 M02 B
Electric Diagram
NPA 231 M02 C
LOGIC DIAGRAM: 7.3
Numbers out of the logic symbols are finger-stripe connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 7.4
Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-stripe connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 2
INTEGRATED CIRCUITS/MODULE: 4
INTEGRATED CIRCUITS USED: 2 × SN 7451 N 1 × SN 7450 N
1 × SN 7460 N

LOADING FACTORS: PIN: 8,5,7,9,6,11,15,13,17,23,21,19, 35,40,36,38,33,31,27,29
25
1 unit
8 units

DRIVING ABILITY: PIN: 10,22
10 units

POWER DISSIPATION/MODULE: 95 mW (typ.)

FUNCTIONAL DESCRIPTION:

FOR POSITIVE LOGIC:

\[ x = \overline{a_1} \oplus b_1 + a_2 \oplus b_2 + a_3 \oplus b_3 + a_4 \oplus b_4 \]

DESCRIPTION

A binary comparator is a combinational circuit whose inputs are two binary words \( (a_1...a_n, b_1...b_n) \) and whose output \( (bc) \) is a function that is "one" when the two words are different.

The function is obtained by summing modulo 2 the corresponding bits of the two words, and by summing up logically the resulting functions:

\[ bc = a_1 \oplus b_1 + ... + a_n \oplus b_n \]

The modulo-2 adder is an exclusive-OR circuit as shown in the figure:

\[ F = X \oplus Y \]
The binary comparator function in this module is also gated by an external signal g and, because of the circuit configuration, it is also inverted. So the function obtained is:

\[ x = \text{bo} \cdot g \]

In order to have the gated function, it is necessary to invert the output.

**HOW TO USE THE CIRCUIT**

a) **Words of less than, or of four bits.**

Connect the unused inputs \((a_1, \ldots, b_2, \ldots)\) to ground and their complements \((\overline{a_1}, \ldots, \overline{b_2}, \ldots)\) to +5 V; the inverted output \(x\) will be available at pin 22.

The function obtained is:

\[ x = \text{bo} \cdot g = \overline{g(a_1 \oplus b_1 + a_2 \oplus b_2 + \ldots)} \]

\(\overline{x}\) is "one" when the gate \(g\) is "one" and the two words are different.

b) **Words of more than four bits.**

Use two or more boards.

Connect output signals \(x_1\) (pin 22) \(\ldots\) \(x_n\) (pin 22) of each board to an \(N\)-input NAND gate.

The function obtained is:

\[ x_n = \overline{g(a_1 \oplus b_1 + \ldots a_4 \oplus b_4 + \ldots / a_1 \oplus b_1 + a_4 \oplus b_4)} \]

\(x_n\) is "one" when the gate \(g\) is "one" and the two words are different.

c) **The spare "exclusive OR" may be used for comparing words of one bit each.**
FOUR-BIT BINARY COMP AND EXCL. OR
Logic Diagram

FOUR-BIT BINARY COMP AND EXCL. OR
Logic Diagram

A

B

C

D

25_y

27_\overline{a_4}

29_\overline{b_4}

31_b_4

33_a_4

36_\overline{a_3}

38_b_3

40_b_3

19_b_2

23_\overline{b_2}

17_a_2

15_\overline{a_1}

13_b_1

6_a_1

11_b_1

7_a_1

9_b_1

5_b_0

8_a_0

10_10

21_a_2

22_x

24_{\overline{a_4}}

26_{\overline{b_4}}

12_12

11_11

13_13

10_10

9_9

8_8

4_4

3_3

3_3

5_5

4_4

2_2
FOUR-BIT BINARY COMP AND EXCL OR

Electric Diagram
NPA 231 M03 C
LOGIC DIAGRAM: 8.3

Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 8.4

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.
No connection between elements on a board has been indicated, with the exception of the power and ground connections.

LOGIC FUNCTIONS/MODULE: 4

INTEGRATED CIRCUITS/MODULE: 6

INTEGRATED CIRCUITS USED: 2 x SN 7400 N
4 x SN 7450 N

LOADING FACTORS: PIN: 8, 10, 12, 14, 6, 5, 18, 16, 9, 11, 13, 20,
7, 15, 19, 17, 27, 23, 31, 33, 32, 30, 28, 37
1 unit

DRIVING ABILITY: PIN: 25, 29, 34, 35 10 units
21, 40 8 units
36, 38 9 units

POWER DISSIPATION/MODULE: 196 mW (typ.)

FUNCTIONAL DESCRIPTION (for positive logic):

This logic circuit is intended to provide means to generate a parity bit (even or odd) from a binary word.

- \( e_p_n \) (even parity bit for \( n \) bits word)
  - The last added bit, i.e. \( e_p_n \), lets the sum of "ones" in the resulting \( n+1 \) bits word (\( n \) bits word + 1 parity bit) be an even number.

- \( o_p_n \) (odd parity bit for \( n \) bits word)
  - The last added bit, i.e. \( o_p_n \), lets the sum of "ones" in the resulting \( n+1 \) bits word (\( n \) bits word + 1 parity bit) be an odd number.

By these definitions \( e_p_n \) and \( o_p_n \) may be obtained by summing modulo 2 all the bits of the given word,

\[
e_p_n = b_1 \oplus b_2 \oplus \ldots \oplus b_n
\]

\[
o_p_n = b_1 \oplus b_2 \oplus \ldots \oplus b_n \oplus 1
\]

Also the following relation holds:

\[
o_p_n = \overline{e_p_n}
\]
The modulo-2 sum is obtained by the mean of an "exclusive-OR" circuit which is fed by the two signals and their complements.

```
  x
  w
  x
  w
```

```
ep_2 = x \oplus y
```

**HOW TO USE THE CIRCUITS**

Two "two-input" gates are available and may be used for obtaining, instead of the even parity bit, an odd parity bit:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(35)</td>
<td>ep_2</td>
<td>Use the spare &quot;exclusive-OR&quot;.</td>
</tr>
<tr>
<td>(21)</td>
<td>ep_3 = a \oplus b \oplus c</td>
<td>Use inputs a, \overline{a}, \overline{b}, \overline{c}. Connect d to ground, \overline{d} to +5 V. In this case ep_4 = ep_2.</td>
</tr>
<tr>
<td>(40)</td>
<td>ep_3 = e \oplus f \oplus g</td>
<td>Use inputs e, \overline{e}, f, \overline{f}, g, \overline{g}. Connect h to ground, \overline{h} to +5 V. In this case ep_4 = ep_2.</td>
</tr>
<tr>
<td>(21)</td>
<td>ep_4 = a \oplus b \oplus c \oplus d</td>
<td>Use inputs a\overline{a}, b\overline{b}, c\overline{c}, d\overline{d}.</td>
</tr>
<tr>
<td>(40)</td>
<td>ep_4 = e \oplus f \oplus g \oplus h</td>
<td>Use inputs e\overline{e}, f\overline{f}, g\overline{g}, h\overline{h}.</td>
</tr>
<tr>
<td>(34)</td>
<td>ep_5 = a \oplus b \oplus c \oplus d \oplus e</td>
<td>Use inputs a\overline{a}, b\overline{b}, c\overline{c}, d\overline{d}, e\overline{e}. Connect f, g, h to ground, \overline{f}, \overline{g}, \overline{h} to +5 V. In this case ep_6 = ep_5.</td>
</tr>
<tr>
<td>(34)</td>
<td>ep_6 = a \oplus b \oplus c \oplus d \oplus e \oplus f</td>
<td>Use inputs a\overline{a}, b\overline{b}, c\overline{c}, d\overline{d}, e\overline{e}, f\overline{f}. Connect g, h to ground, \overline{g}, \overline{h} to +5 V. In this case ep_6 = ep_5.</td>
</tr>
<tr>
<td>(34)</td>
<td>ep_7 = a \oplus b \oplus c \oplus d \oplus e \oplus f \oplus g</td>
<td>Use inputs a\overline{a}, b\overline{b}, c\overline{c}, d\overline{d}, e\overline{e}, f\overline{f}, g\overline{g}. Connect h to ground, \overline{h} to +5 V. In this case ep_7 = ep_6.</td>
</tr>
<tr>
<td>(34)</td>
<td>ep_8 = a \oplus b \oplus c \oplus d \oplus e \oplus f \oplus g \oplus h</td>
<td>Use inputs a\overline{a}, b\overline{b}, c\overline{c}, d\overline{d}, e\overline{e}, f\overline{f}, g\overline{g}, h\overline{h}.</td>
</tr>
</tbody>
</table>

For more than an eight-bit word, use two or more boards and employ the spare "exclusive-OR" given in each board. For example:

```
ep_{16} = ep_8 \oplus ep_6
```
### LOGIC DIAGRAM

Numbers out of the logic symbols are finger-strip connector pins.

Numbers inside logic symbols are integrated circuit leads.

### ELECTRIC DIAGRAM

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).

Capital letters indicate the position of each IC package on the board.

### LOGIC FUNCTIONS/MODULE:
2

### INTEGRATED CIRCUITS/MODULE:
3

### INTEGRATED CIRCUITS USED:
3 × SN 7400 N

### LOADING FACTORS:
- PIN: 9, 11, 13, 15, 17, 19, 25, 23, 29, 27, 35, 31  
  1 unit
- PIN: 21, 33  
  6 units

### DRIVING ABILITY:
- PIN: 10, 12, 16, 14, 18, 20, 24, 22, 26, 29, 30, 32  
  10 units

### POWER DISSIPATION/MODULE:
120 mW (typ.)

### FUNCTIONAL DESCRIPTION:

This module includes two groups of six gates each. All the gates in a group have an independent input line, an independent output line, and a common transfer input. Each gate structure can be used for the common transfer control of six data signals.
READ/WRITE MULTIPLEXER

Logic Diagram

NPA 231 M05B
LOGIC DIAGRAM: 10.2
Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 10.3
Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.

LOGIC FUNCTIONS/MODULE: 6
INTEGRATED CIRCUITS/MODULE: 3
INTEGRATED CIRCUITS USED: 3 x SN 7474 N
LOADING FACTORS: PIN: 11,13,21,23,31,33 3 units
7,15,17,25,27,39 2 units
9,14,19,24,29,37 1 unit
35 12 units
DRIVING ABILITY: PIN: 12,10,18,16,22,20, 10 units
28,26,32,30,34,36
POWER DISSIPATION/MODULE: 240 mW (typ.)

FUNCTIONAL DESCRIPTION:
This module features D-type flip-flops; in this element, a single-ended data input (D) is transferred to the output on the positive edge of clock pulse. This module is especially suited for buffer registers and for input/output data storage. As a modular memory register, it is expandable with additional NPA 231 cards to any bit-length.
The clock line is common to all stages, whilst information, clear and preset inputs, and complementary outputs are all brought to the connector.
LOGIC DIAGRAM: 11.3

Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 11.4

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate
finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.
No connection between elements on a board has been indicated, with the exception of the
power and ground connections.

LOGIC FUNCTIONS/MODULE: 6

INTEGRATED CIRCUITS/MODULE: 3

INTEGRATED CIRCUITS USED: 2 x SN 7472 N
1 x SN 7400 N

LOADING FACTORS: PIN: 5,13,14,20
7,9,11,17,19,15,16,23,21,
26,28,22,31,29,25,27,33,35,
37,39,
10
2 units
1 unit
4 units

DRIVING ABILITY: PIN: 8,12,16,24,30,32,34,36
10 units

POWER DISSIPATION/MODULE: 120 mW (typ.)

FUNCTIONAL DESCRIPTION:

Useful in many applications where more elaborate input gate circuits are required, this
module contains two JK master-salave flip-flops (SN 7472 N) that are independent except for
the common clock line. The input gating provided on the card is sufficient for constructing
binary or decimal counters and shift registers.

1) SYNCHRONOUS DATA ENTRY (J1,J2,J3,K1,K2,K3)

a) Description

The entry of information at the synchronous inputs JK is under direct control of the
clock input. Input signals formed at the input "AND gates" are entered into the "master"
when the clock is high and are thereafter transferred to the "slave" when the clock becomes
low.

The synchronous inputs are thus inhibited when the outputs of the master-salave flip-
flop are changing.
b) **How to use the circuit**

A necessary and sufficient condition for trouble-free operation is that the asynchronous inputs may change only when the clock input is low.

2. **ASYNCHRONOUS DATA ENTRY (CLEAR, PRESET)**

a) **Description**

Asynchronous entry is made available at the "slave" flip-flop.

b) **How to use the circuit**

Low input at clear input sets master-slave flip-flop Q output to logical 0 independently of the clock.

3. **CLOCK**

a) **How to use the circuit**

For clock pulses derived at natural IC/TTL system speed, the flip-flop is a JK as shown in the truth table.

<table>
<thead>
<tr>
<th>$J = J_1 J_2 J_3$</th>
<th>$K = K_1 K_2 K_3$</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$Q_n$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$Q_n$</td>
</tr>
</tbody>
</table>

For clock pulses with slow clock voltage change-rate, the flip-flop will behave as a Set/Reset as shown in the truth table.

<table>
<thead>
<tr>
<th>$J = J_1 J_2 J_3$</th>
<th>$K = K_1 K_2 K_3$</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$=S$</td>
<td>$=R$</td>
<td>$Q_n$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>?</td>
</tr>
</tbody>
</table>

In this case, if it is still desired to have a JK flip-flop, it is necessary to connect $\overline{Q}$ to J input and Q to K input as shown in this figure.
SEQUENTIAL FF AND GATES

Logic Diagram

A

13 PRESET
7 J1 3
9 J2 4
11 J3 5
17 K1 9
19 K2 10
15 K3 11
5 CLEAR

B

20 PRESET
16 J1 3
23 J2 4
21 J3 5
10 CLOCK
12
16 K1 9
28 K2 10
22 K3 11
14 CLEAR

C

31
29
25
27
33
35
37
39

Q 12
\bar{Q} 8
Q 24
\bar{Q} 18

NPA 231 F02 B
SEQUENTIAL FF AND GATES
Electric Diagram
NPA 231 F02 C
LOGIC DIAGRAM: 12.7

Numbers out of the logic symbols are finger-strip connector pins.
Numbers inside logic symbols are integrated circuit leads.

ELECTRIC DIAGRAM: 12.8

Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.
No connection between elements on a board has been indicated, with the exception of the power and ground connections.

LOGIC FUNCTIONS/MODULE: 2

INTEGRATED CIRCUITS/MODULE: 8

INTEGRATED CIRCUITS USED: 2 × SN 7400 N
6 × SN 7472 N

LOADING FACTORS: PIN: 38
5, 14, 24, 26, 40
3, 4, 27, 29, 33, 37, 9, 11, 13, 19,
17, 23, 25

DRIVING ABILITY: PIN: 1, 2, 6, 11, 10, 16, 20, 26, 32
3, 36, 31, 37, 18, 15, 22, 21

POWER DISSIPATION/MODULE: 320 mW (typ.)

FUNCTIONAL DESCRIPTION:

This module contains a six-stage presettable shift register designed for parallel or serial input, and parallel and serial output.

The card is designed for series to parallel conversion, time sequencing, and pulse distribution.

The card behaves as a divide-by-N module where "N" is any integer from 3 through 12.
A number of these modules can be connected together to perform division by numbers greater than 12.

This module can also be used for counting. True and false outputs of each stage are brought out to the connector, together with a common Clear Input.

The use of a shift counter allows unique patterns to be created, which repeat at a rate corresponding to the division interval to be obtained. Thus one of the major advantages of the module-N counter is that each binary-stage in the chain counts at a maximum frequency of 1/\(m\), where \(m\) is the number of stages. This means that the minimum period of the input signal must not be smaller than the transition time of the memory element.
Let us consider a counter by ten: since the shift counters need 5 binaries to create 10 stable states, from the $2^5 = 32$ possible states 22 will be unassigned. There are many possible count sequences, or major modes, but there is only one mode that allows the simplest decoding in case the frequency divider has to be used as a counter. Namely,

<table>
<thead>
<tr>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The undesirable modes are suppressed by added logic. For example, always for the counter by 10, the 22 spurious configurations (the counter might enter in one of these configurations when the equipment is turned on or because of noise) are grouped into the following three cycles:

<table>
<thead>
<tr>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>1</td>
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<td>1</td>
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</tr>
</tbody>
</table>

In this case the undesirable modes are suppressed simply by adding a gate.
The logic prevents the transient interference from changing the counting sequence. The trade-off for the protection is the reduction of speed by about 20%.

Typical waveforms for a shift counter follow together with the various configurations necessary to obtain a counter by 3 to 12 with decoded outputs.
LOGIC DIAGRAM: 13.5
Numbers out of the logic symbols are finger-strip connector pins;
Numbers inside logic symbols are integrated circuit leads.
Small letters indicate connections on the board.

ELECTRIC DIAGRAM: 13.6
Numbers close to IC symbols are IC leads; numbers on both sides of the diagram indicate
finger-strip connector pins (even on one side, odd on the other).
Capital letters indicate the position of each IC package on the board.
No connection between elements on a board has been indicated, with the exception of the
power and ground connections.

LOGIC FUNCTIONS/MODULE: 1

INTEGRATED CIRCUITS/MODULE: 10

INTEGRATED CIRCUITS USED: 2 x SN 7472 N  2 x SN 7410 N  1 x SN 7441 N
2 x SN 7400 N  1 x SN 7420 N

LOADING FACTORS: PIN: 31  8 units
26  8 units
39,37,34,28  2 units
40  6 units

DRIVING ABILITY: PIN: 35  3 units  32  7 units
33  6 units  25  9 units
29  7 units  8  8 units
27  8 units  30  8 units

POWER DISSIPATION/MODULE: 415 mW (typ.)

FUNCTIONAL DESCRIPTION:

This card provides a reversible BCD counter operating in the 1248 code together with
decimal decoder and drivers for nixie tube display.

The counter circuit is controlled by "complementary" forward or backward level inputs,
and supplies normal and complemented outputs from each stage.

Preset inputs allow parallel storage transfer.

Two or more cards can be connected for construction of reversible counters of any
length.

A block diagram of the unit follows.
SYNC UP/DOWN BCD DECADE AND DECODER
When $X = 1$ the system performs the UP count; 
when $X = 0$ the system performs the DOWN count.

1. **CLOCK CHARACTERISTICS**

   The memory elements are JK master-slave flip-flops (SN 7472 N). They change state at 
   the trailing edge of the clock pulse. Information must be stable during the time the clock 
   pulse is higher than the switching level of $1.5 \text{ V}$. 
   
   The hold time ($t_h$) must then be higher than or equal to the applied clock-pulse width.

   The minimum clock-pulse width is 20 nsec.

   The propagation delay of each flip-flop is 50 nsec typically.

---

### Diagram

- **Clock**
  - $t_p$

- **Input**
  - $t_h$
  - $t_{pd}$

- **Output**
  - $t_{pd}$

**Recommended conditions:**

- $t_p \geq 20 \text{ nsec}$
- $t_h \geq t_p$
- $t_{pd} = 50 \text{ nsec/FF}$

Clock rise- and fall-time must be derived at standard TTL speed.
2) DECODING CIRCUIT FOR INTERCONNECTING BCD UP/DOWN COUNTERS (SERIAL CARRY)

3) NIXIE DECODER

It is suggested to employ diodes and a prebias voltage of 55 Volts as shown in figure.
LOGIC DIAGRAM: 14.3

Numbers associated with the logic diagram are finger-strip connector pin numbers.

ELECTRIC DIAGRAM: 14.4

PART LIST: 14.5

LOGIC FUNCTIONS/MODULE: 1

LOADING FACTORS: PIN: (36,38) 1 unit

DRIVING ABILITY: PIN: (5,8) 15 units

POWER DISSIPATION/MODULE: 380 mW

FUNCTIONAL DESCRIPTION:

This module includes one integrating multivibrator, with a trigger input (T), a gating input (G), a level output (OUT), a pulse output (OUT*) and six discrete variable delay taps.

Its characteristics include the ability to respond to trigger inputs even while in the "one" state, so that successive trigger inputs above a preset frequency can postpone the return to zero indefinitely.

Starting from the last trigger input "1" to "0" transition, output will stay in the "1" state for an interval of time determined by the time constant of the circuit.

If in this interval of time a trigger input "1" to "0" transition is encountered, the circuit will be reset to initial condition, i.e., the circuit will start to count again the whole interval of time.

The time constant of the circuit is continuously variable from 180 μsec to 1.3 sec; the necessary capacitors to cover this range are included in the module. An internal potentiometer is connected for fine delay adjustment within each range.

With no external pin connection made, the output pulse-width will vary between 180 μsec and 1.2 μsec. Pulse width between 1.2 μsec and 1.3 sec can be obtained by using the proper jumper connections. Each time the level output experiences a transition "1" to "0", a positive pulse (400 μsec wide) occurs. Typical waveforms follow.
**ELECTRICAL CHARACTERISTICS:**

\[
\begin{align*}
V_{IN} \text{ "0"} & \leq 0.4 \, V \\
V_{IN} \text{ "1"} & \geq 2.4 \, V \\
V_{IN} & \\
T_w & \geq 300 \, \text{nsec} \\
T_r & \leq 1 \, \mu\text{sec} \\
T & \geq t_{on} + t_w + t_r + t_{rec}
\end{align*}
\]

**V\text{IN}\text{"0"} INPUT LOADING FACTOR:** 1 TTL LOAD

<table>
<thead>
<tr>
<th>Minimum Load</th>
<th>Maximum Load</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_d)</td>
<td>50 nsec</td>
</tr>
<tr>
<td>(t_r)</td>
<td>20 nsec</td>
</tr>
<tr>
<td>(t_{on})</td>
<td>70 nsec</td>
</tr>
<tr>
<td>(t_w)</td>
<td>180 \mu\text{sec} \to 1.3 , \text{sec}</td>
</tr>
<tr>
<td>(t_r)</td>
<td>15 nsec</td>
</tr>
<tr>
<td>(t_{rec})</td>
<td>300 nsec</td>
</tr>
<tr>
<td>(t_{d*})</td>
<td>20 nsec</td>
</tr>
<tr>
<td>(t_{r*})</td>
<td>30 nsec</td>
</tr>
<tr>
<td>(t_{on*})</td>
<td>50 nsec</td>
</tr>
<tr>
<td>(t_{w*})</td>
<td>400 nsec</td>
</tr>
<tr>
<td>(t_{r*})</td>
<td>20 nsec</td>
</tr>
</tbody>
</table>

**GLOSSARY:**

- \(V_{IN} \text{ "0"}\): Input voltage at logical "zero" level
- \(V_{IN} \text{ "1"}\): Input voltage at logical "one" level
- \(T_w\): Input pulse-width
- \(T_r\): Input pulse fall-time
- \(T\): Input period
- \(t_d\): Output delay time
- \(t_r\): Output rise-time
- \(t_{on}\): Output on-time
- \(t_w\): Output pulse-width
- \(t_{fr}\): Output fall-time
- \(t_{rec}\): Recovery-time

![Diagram](image-url)
INTEGRATING MULTIVIBRATOR
Logic Diagram
NPA 231 S01B

OUT (5) WIDTH RANGE

<table>
<thead>
<tr>
<th>RANGE</th>
<th>FROM</th>
<th>TO</th>
<th>EX. CONNECTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>180 µsec</td>
<td>1.2 msec</td>
<td>21,26</td>
</tr>
<tr>
<td>2</td>
<td>1 msec</td>
<td>12 msec</td>
<td>21,26 - 31,33</td>
</tr>
<tr>
<td>3</td>
<td>3.5 msec</td>
<td>14 msec</td>
<td>21,28 - 31,33</td>
</tr>
<tr>
<td>4</td>
<td>13 msec</td>
<td>120 msec</td>
<td>21,28 - 31,33</td>
</tr>
<tr>
<td>5</td>
<td>115 msec</td>
<td>1.3 sec</td>
<td>21,30 - 31,33</td>
</tr>
</tbody>
</table>
INTEGRATING MULTIVIBRATOR
Electric Diagram
NPA 231 S01C
## INTEGRATING MULTIVIBRATOR

**NPA 231 S01 D**

**PART LIST (1)**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>VALUE</th>
<th>TOLERANCE</th>
<th>RATED POWER</th>
<th>SUPPLIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>1 kΩ</td>
<td>5%</td>
<td>1/4 W</td>
<td>ALLEN BRADLEY</td>
</tr>
<tr>
<td>R2</td>
<td>10 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R3</td>
<td>330 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R4</td>
<td>220 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R5</td>
<td>100 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R6</td>
<td>4,70 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R7</td>
<td>1 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R8</td>
<td>1,5 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R9</td>
<td>1 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R10</td>
<td>3,3 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R11</td>
<td>100 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R12</td>
<td>820 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R13</td>
<td>3,3 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R14</td>
<td>150 Ω</td>
<td>&quot;</td>
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<td>&quot;</td>
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<td>3 W</td>
<td>PAINTON</td>
</tr>
<tr>
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<td>&quot;</td>
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# INTEGRATING MULTIVIBRATOR

**NPA 231 S01 D**

**PART LIST (2)**

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<tr>
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<tr>
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<tr>
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<td>30 &quot;</td>
<td>&quot;</td>
</tr>
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<td>10%</td>
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<td>C7</td>
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LOGIC DIAgRAM: 15.3

Numbers associated with the logic diagram are finger-strip connector pin numbers.

ELECTRIC DIAgRAM: 15.4

PART LIST: 15.5

LOGIC FUNCTIONS/MODULE: 1

LOADING FACTORS: PIN: (26,29) 1 unit

DRIVING ABILITY: PIN: (5,7) 15 units

POWER DISSIPATION/MODULE: 380 mW

FUNCTIONAL DESCRIPTION:

This module includes one monostable multivibrator (one-shot) with a trigger input (T), a gating input (G), a level output (OUT), a pulse output (OUT'), and six discrete variable delay taps.

The time constant of the circuit is continuously variable from 150 nsec to 1.2 msec. The capacitors necessary to obtain this range are included in the module. An internal potentiometer is connected for fine delay adjustment within each range. With no external pin connection made, the output pulse width will vary between 150 nsec and 5 μsec with the help of an internal potentiometer. Pulse widths between 2 μsec and 1.2 msec can be obtained by using the proper jumper connections. A positive pulse at input T if enabled by the presence of a logical "T" at input G, will let OUT switch from logical level "0" to logical level "1" for the above-mentioned time constant, after which output OUT switches back to the level "0". Each time OUT switches back to "0", a positive pulse (duration 60 nsec or 110 nsec) occurs at OUT'.

The one-shot circuit is used to generate pulse widths of specified duration and to delay a pulse by a specified amount.
ELECTRICAL CHARACTERISTICS:

\[ V_{IN} \text{ "0"} \leq 0.4 \text{ V} \]
\[ V_{IN} \text{ "1"} \geq 2.4 \text{ V} \]
\[ V_{IN} \geq 300 \text{ nsec} \]
\[ T_r \leq 1 \mu\text{sec} \]
\[ T \geq t_{on} + t_w + t_f + t_{rec} \]

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<td>( t_d )</td>
<td>40 nsec</td>
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<tr>
<td>( t_r )</td>
<td>20 nsec</td>
</tr>
<tr>
<td>( t_{on} )</td>
<td>60 nsec</td>
</tr>
<tr>
<td>( t_w )</td>
<td>200 - 800 \mu\text{sec}</td>
</tr>
<tr>
<td>( t_f )</td>
<td>15 nsec</td>
</tr>
<tr>
<td>( t_{rec} )</td>
<td>300 nsec</td>
</tr>
<tr>
<td>( t_d^* )</td>
<td>20 nsec</td>
</tr>
<tr>
<td>( t_r^* )</td>
<td>30 nsec</td>
</tr>
<tr>
<td>( t_{on}^* )</td>
<td>50 nsec</td>
</tr>
<tr>
<td>( t_w^* )</td>
<td>150 nsec to 300 nsec</td>
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<tr>
<td>( t_f^* )</td>
<td>20 nsec</td>
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GLOSSARY:

\( V_{IN} \text{ "0"} \) Input voltage at logical "zero" level
\( V_{IN} \text{ "1"} \) Input voltage at logical "one" level
\( T_w \) Input pulse-width
\( T_f \) Input pulse fall-time
\( T_t \) Input period
\( t_d \) OUT delay-time
\( t_r \) OUT rise-time
\( t_{on} \) OUT on-time
\( t_w \) OUT pulse-width
\( t_f \) OUT fall-time
\( t_{rec} \) OUT recovery-time
MONOSTABLE MULTIVIBRATOR
Logic Diagram
NPA 231S02B

OUT (7) WIDTH RANGE

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<tr>
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<th>EX. CONNECTIONS</th>
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<tr>
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<td>2 µsec</td>
<td>38 µsec</td>
<td>31, 34</td>
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<tr>
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<td>12 µsec</td>
<td>250 µsec</td>
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<td>4</td>
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<td>1.2 msec</td>
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OUT* (5) WIDTH RANGE

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<tr>
<td>2</td>
<td>300 nsec</td>
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MONOSTABLE MULTIVIBRATOR

Electric Diagram
NPA 231 S02 C
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<tr>
<td>R2</td>
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<td>±%</td>
<td>±%</td>
</tr>
<tr>
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<td>±%</td>
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</tr>
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<tr>
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</table>
LOGIC DIAGRAM: 16.4

Numbers associated with the logic diagram are finger-strip connector pin numbers.

ELECTRIC DIAGRAM: 16.5

PART LIST: 16.6

LOGIC FUNCTIONS/MODULE: 2

LOADING FACTORS: PIN: (19,37) 1 unit
(5,7,23,27) See below the "clamping diode characteristics"

DRIVING ABILITY: PIN: (12,16,26,32) See below the "output characteristics"

POWER DISSIPATION/MODULE: 1000 mW

FUNCTIONAL DESCRIPTION:

This module contains two single input driver circuits. The function of each circuit is to convert standard TTL logic levels into outputs suitable for transmission over a balanced, terminated, twisted-pair, transmission line of the type shown in the attached diagram (16.3).

In quiescent conditions, the bias resisters of the line (2.2 K and 2.7 K) hold the line-to-line voltage at about 0.6 V.

When the transmitter is enabled by a logical "0" at the input, a current of about 26 mA is driven into the line and a full reversal of the line-to-line voltage takes place.

The information is then transmitted in the form of differential voltages.

Clamping diodes are provided (-CL and +CL) in order to inhibit the transmitter, where required.

1. CHARACTERISTICS

a) Input

The input accepts standard TTL logic levels with an equivalent loading factor of 1 unit.

b) Output

One transmitter can drive up to 20 receivers (see 17.1).
2. TRANSIENT CHARACTERISTICS

![Diagram showing input and output waveforms with rise-time, fall-time, delay-time, storage-time, and minimum pulse-width labels.

Rise-time \( t_r = 60 \text{ nsec} \)

Fall-time \( t_f = 30 \text{ nsec} \)

Delay-time \( t_d = 100 \text{ nsec} \)

Storage-time \( t_s = 40 \text{ nsec} \)

Minimum pulse-width \( t_w = 100 \text{ nsec} \)

3. CLAMPING DIODES

In order to inhibit the transmitter, \( V + CL \) must be lower than +1.5 V and \( V - CL \) must be higher than -1.5 V.

The current to be sunk from the clamping diode input is of about 43 mA for \( V + CL \) and \( V - CL \), equal to +1.5 V and -1.5 V respectively, and about 66 mA for \( V + CL \) and \( V - CL \) equal to zero.
TRANSMITTER
Logic Diagram
NPA 231 S03 B

+ OUT
26
- OUT
38

IN
37
- CL
27
+ CL
23

IN
19
- CL
7
+ CL
5

+ OUT
6
- OUT
16
TRANSMITTER
Electric Diagram
NPA 231 S03 C
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<td>5%</td>
<td>1/4 W</td>
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<td>R2</td>
<td>10 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R3</td>
<td>2.2 kΩ</td>
<td>&quot;</td>
<td>&quot;</td>
</tr>
<tr>
<td>R4</td>
<td>220 Ω</td>
<td>&quot;</td>
<td>&quot;</td>
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<tr>
<td>R5</td>
<td>1 kΩ</td>
<td>&quot;</td>
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</tr>
<tr>
<td>R6</td>
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</tr>
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<tr>
<td>R10</td>
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<td>3 W</td>
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<tr>
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<td>20%</td>
<td>25 V&lt;sub&gt;cc&lt;/sub&gt;</td>
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<td>16 μF</td>
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</table>
LOGIC DIAGRAM: 17.2

Numbers in the logic diagram indicate finger-strip connector pin numbers.

ELECTRIC DIAGRAM: 17.3

PART LIST: 17.4

LOGIC FUNCTIONS/MODULE: 2

LOADING FACTORS: PIN: (8, 14, 36, 40) See below on the "input characteristics"

DRIVING ABILITY: PIN: (22, 26) 9 units
(24, 28) 10 units

POWER DISSIPATION/MODULE: 400 mW

FUNCTIONAL DESCRIPTION:

This module contains two differential input receivers. The function of each circuit is to convert differential voltage transmitted over a balanced, terminated, twisted-pair, transmission line of the type shown on page 16.3, into standard TTL logic levels.

1. CHARACTERISTICS

a) Input

The input accepts differential voltages.

If the line is driven by a transmitter logic module, up to 20 receivers may be connected to the line.

b) Output

OUT this output has a driving ability of 10 units
OUT this output has a driving ability of 9 units

\[
\begin{array}{c}
\text{INPUT} \\
\text{OUTPUT} \\
\end{array}
\]

\[t_d = 0.4 \mu\text{sec}\]
\[t_s = 0.3 \mu\text{sec}\]
\[t_r = 8 \text{ nsec}\]
\[t_f = 10 \text{ nsec}\]
RECEIVER
Logic Diagram
NPA 231 S04 B

RE

+ IN
36

- IN
40

OUT
26

OUT
28

RE

+ 14

- 8

OUT
22

OUT
24
# RECEIVER

NPA 231 SOL D

## PART LIST

<table>
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<th>VALUE</th>
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<th>SUPPLIER</th>
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<td></td>
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<tr>
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<tr>
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<td>R6</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td>10 kΩ</td>
<td></td>
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<tr>
<td>R8</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>R9</td>
<td>220 Ω</td>
<td></td>
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</tr>
<tr>
<td>R10</td>
<td>1 kΩ</td>
<td></td>
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</tr>
<tr>
<td>R11</td>
<td>1 kΩ</td>
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</tr>
<tr>
<td>R12</td>
<td>2.7 Ω</td>
<td>3 W</td>
<td>PAINTON</td>
</tr>
<tr>
<td>R13</td>
<td>2.7 Ω</td>
<td></td>
<td></td>
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<tr>
<td>C1</td>
<td>16 µF</td>
<td>20%</td>
<td>25 V FO</td>
</tr>
<tr>
<td>C2</td>
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<td>TEXAS</td>
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<td>TTL2</td>
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</table>
LOGIC DIAGRAM: 18.2

Numbers in the logic diagram indicate finger-strip connector pin numbers.

ELECTRIC DIAGRAM: 18.3

PART LIST: 18.4

LOGIC FUNCTIONS/MODULE: 4

LOADING FACTORS: PIN: See Functional Description

DRIVING ABILITY: PIN: (6, 14, 30, 34) 9 units

(8, 12, 32, 36) 10 units

POWER DISSIPATION/MODULE: 650 mW

FUNCTIONAL DESCRIPTION:

The input logic level converter transforms negative voltage logic levels characteristic of the R and B DEC Series into positive voltage logic levels that can drive standard TTL integrated circuits. Each converter features TRUE and COMPLEMENT outputs. Four converters are available on a single card.

1. CHARACTERISTICS

a) Input

Upper level - 0.3 V

Lower level - 3.5 V

Sink current = 1.8 mA

Load current = 160 μA

b) Output

Delay-time

Storage-time

Rise-time

Fall-time

\( t_d = 30 \text{ nsec} \)

\( t_s = 10 \text{ nsec} \)

\( t_r = 20 \text{ nsec} \)

\( t_f = 15 \text{ nsec} \)
INPUT LOGIC LEVEL CONVERTER
Logic Diagram
NPA 231 S05 B

4 IN

IC

OUT 6
OUT 8

18

IC

14
12

26

IC

30
32

38

IC

34
36
INPUT LOGIC LEVEL CONVERTER

Electric Diagram
NPA 231 S05C
## INPUT LOGIC LEVEL CONVERTER

### NPA 231 305 D

### PART LIST

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<th>TOLERANCE</th>
<th>SUPPLIER</th>
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<tr>
<td>R1</td>
<td>1 kΩ</td>
<td>5%</td>
<td>1/4 W</td>
</tr>
<tr>
<td>R2</td>
<td>6.8 kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>1 kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>120 Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>100 Ω</td>
<td></td>
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</tr>
<tr>
<td>R6</td>
<td>2.7 Ω</td>
<td>3 W</td>
<td></td>
</tr>
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<td>R7</td>
<td>2.7 Ω</td>
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</tr>
<tr>
<td>C1</td>
<td>16 μF</td>
<td>20%</td>
<td>25 V DC</td>
</tr>
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<td>TLL1</td>
<td>1/4 SN7400 N</td>
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<tr>
<td>TLL2</td>
<td>1/4 SN7400 N</td>
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</tbody>
</table>
LOGIC DIAGRAM: 19.2
Number in the logic diagram indicate finger-strip connector pin numbers.

ELECTRIC DIAGRAM: 19.3

PART LIST: 19.4

LOGIC FUNCTIONS/MODULE: 4

LOADING FACTORS: PIN: (5, 14, 28, 36) 1 unit

DRIVING ABILITY: PIN: See Functional Description

POWER DISSIPATION/MODULE: 480 mW

FUNCTIONAL DESCRIPTION:
This module contains four signal converters which can be used to interface the positive logic levels or pulses of the NPA 231 Series to digital negative logic levels of -3 V and 0 V characteristic of the R and B DEG Series.

CHARACTERISTICS

a) Input
Loading factor: 1 unit

b) Output
Upper level Load current = 4.5 mA
Lower level Load current = 5 mA
Delay-time \( t_d = 60 \text{ nsec} \)
Storage-time \( t_s = 180 \text{ nsec} \)
Rise-time \( t_r = 10 \text{ nsec} \)
Fall-time \( t_f = 20 \text{ nsec} \)

![Input and Output Waveforms](image-url)
OUTPUT LOGIC LEVEL CONVERTER

Logic Diagram

NPA 231 S06 B
OUTPUT LOGIC LEVEL CONVERTER

Electric Diagram
NPA 231 S06C
<table>
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<th>VALUE</th>
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<tbody>
<tr>
<td>R1</td>
<td>1 kΩ</td>
<td>±5%</td>
<td>1/4 W</td>
</tr>
<tr>
<td>R2</td>
<td>10 kΩ</td>
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</tr>
<tr>
<td>R3</td>
<td>220 Ω</td>
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<td>&quot;</td>
</tr>
<tr>
<td>R4</td>
<td>1 kΩ</td>
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</tr>
<tr>
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