A DATA LINK BETWEEN TWO COMPUTERS

P. Marciano
Propriété littéraire et scientifique réservée pour tous les pays du monde. Ce document ne peut être reproduit ou traduit en tout ou en partie sans l'autorisation écrite du Directeur général du CERN, titulaire du droit d'auteur. Dans les cas appropriés, et s'il s'agit d'utiliser le document à des fins non commerciales, cette autorisation sera volontiers accordée.

Le CERN ne revendique pas la propriété des inventions brevetables et dessins ou modèles susceptibles de dépôt qui pourraient être décrits dans le présent document; ceux-ci peuvent être librement utilisés par les instituts de recherche, les industriels et autres intéressés. Cependant, le CERN se réserve le droit de s'opposer à toute revendication qu'un usager pourrait faire de la propriété scientifique ou industrielle de toute invention et tout dessin ou modèle décrits dans le présent document.

© Copyright CERN, Genève, 1965

Literary and scientific copyrights reserved in all countries of the world. This report, or any part of it, may not be reprinted or translated without written permission of the copyright holder, the Director-General of CERN. However, permission will be freely granted for appropriate non-commercial use.

If any patentable invention or registrable design is described in the report, CERN makes no claim to property rights in it but offers it for the free use of research institutions, manufacturers and others. CERN, however, may oppose any attempt by a user to claim any proprietary or patent rights in such inventions or designs as may be described in the present document.
ABSTRACT

A digital link is described which allows exchange of control and data messages between two computers, the CDC 6600 located in the CERN main computing area, and the SDS 920 located at a distance of up to 1 km in the experimental area.

Blocks of data can be transferred over the link at a rate of 24 bits/8 μsec in both directions. This is the first item of a system expandable to up to eight data links.
# CONTENTS

1. **INTRODUCTION** .... 1

2. **OUTLINE OF THE SYSTEM**
   2.1 The CDC 6600 .... 1
   2.2 The SDS 920 .... 2
   2.3 The data link .... 2

3. **DATA-LINK CONTROL UNIT**
   3.1 Data-link selection .... 4
   3.2 Control dialogue translation .... 4
   3.3 Format conversion and parity check .... 5
   3.4 Synchronization .... 6

4. **TEST PROGRAMME** .... 6

5. **FUTURE DEVELOPMENTS** .... 7

ACKNOWLEDGEMENTS .... 9

REFERENCES .... 10
1. **INTRODUCTION**

The SDS 920, a small-size medium-speed computer, is used in the experimental area for on-line data acquisition and checking.

Its size does not allow it to carry out complete calculations, and as a consequence data are recorded on magnetic tape for later processing on a larger and faster computer.

The CDC 6600, a large-scale, high-speed, time-sharing processor is the main CERN computer on which, inevitably, falls the task of performing laborious calculations. The 6600 can use a link with the 920 for inputting blocks of checked raw data after every accelerator burst (e.g. every 1.8 seconds), for performing immediate and complete calculations on a sample of the data recorded, and for outputting a summary of computed results to the experimental area within a very short time-delay. The construction of the link was decided upon following the recommendations of a Study Group on the on-line use of the 6600.

2. **OUTLINE OF THE SYSTEM**

2.1 **The CDC 6600**

The CDC 6600 consists of 11 independent computers, namely 1 Central Processor and 10 Peripheral and Control Processors, all of them sharing a large central memory.

In addition, each peripheral processor has a separate memory and shares with the other peripheral processors the use of 12 input/output channels. In order to facilitate the connection of the 6600 to external devices requiring input/output transfers at high rate, a Data Channel Adapter (DCA) is supplied by CDC on CERN request. When connected to one of the input/output channels, this unit performs two functions: a) conversion from 6600 high-speed pulse signals to level signals, and vice versa; b) relay synchronization of signals to and from other users of the same channel. Maximum input/output transfer rate via a DCA is 1 word (12 bits) per microsec. In addition, a multiplexer unit (MUX) operating on one of the channels allows connection of devices requiring input/output transfers at slow rate (maximum: 1 word per 100 µsec).
The basic programming tools for channel operation are:

a) output of function words (control);
b) output of data words;
c) input of status words (control);
d) input of data words.

2.2 The SDS 920

Use of the parallel input/output feature of the SDS 920 makes possible the transfer of blocks of data to and from the 920 at a rate of 1 word (24 bits) every 8 microseconds\(^4\).

Several input/output facilities are offered by the SDS 920; however, only the following ones have been used in connection with the data link:

a) EOM, Energize Output M, for output of function words;
b) POT, Parallel Output, for output of data words;
c) Interrupt System \(\) For input of function information

d) SKS, Skip if signal is not set

e) PIN, Parallel Input, for input of data words.

2.3 The Data Link

The data link consists of two items:

a) Data-link control unit, DLC located in the proximity of the 6600. Its functions are data-link selection, control dialogue translation, word format conversion, parity generation and testing, synchronization between the two computers which can produce and accept data at different rates.

b) Transmission equipment consisting of cables, transmitters, receivers, and special interface circuits.

Eight cables of the type described in CERN Report 65-5, Section 2.1\(^5\) are employed, and therefore a total of 80 signal lines is available.

Transmitters and receivers are of the type described in the reference mentioned above; however, some changes were made in order to improve the transmission rate (Fig. 1).
The cables are laid out in three sections, one from the 6600 area to the East compressor building, another from the East compressor building to the South Hall, the last one from the East compressor building to the East Hall (Fig. 2).

A junction box in the East compressor building is used in order to link the 6600 area to either the East Hall or the South Hall area, depending on the location of the experiment using the SDS 920.

Terminal boxes are present in the South Hall, in the East Hall, and in the CDC 6600 area. Flexible cables 25 m long connect these boxes to the racks containing the electronics.

The link is operated for the following purposes:

a) Transmission of blocks of data from one of the 6600 peripheral processors to the parallel input connector of the SDS 920 at the rate of 24 bits every 8 µsec. An even parity bit is generated and transmitted with each word.

b) Transmission of blocks of data from the parallel output connector of the 920 to one of the 6600 peripheral processors at the rate of 24 bits every 8 µsec. An even parity bit is transmitted and tested with each word.

c) Transmission and decoding of control functions set either by the 6600 (output flags) or by the 920 (input flags).

The approximate cost of the link was S.fr.s. 50,000. This includes the cost of components for the two items described above, and manpower cost for laying the cables. Approximate figures for the time spent on the project are: two man months for design, two-and-a-half man months for wiring.

Testing was done by a group of three people over a period of about five months requiring a total of 125 hours of SDS 920 time and about 150 hours of CDC 6600 time (half of this figure refers to time shared with other users of the CDC 6600). Test programme preparation is included.
3. **DATA-LINK CONTROL UNIT** (Fig. 3)

3.1 **Data link selection**

3.1.1 **By CDC 6600**

The first 6 bits of a PP (peripheral processor) function word are decoded in order to select the group of devices connected to one synchronizer, e.g. data channel adopter (3 bits) and one particular device e.g. one data link (3 bits).

3.1.2 **By SDS 920**

When a system control EOM instruction is executed, the presence of a timing signal (SYS) together with bit 19 of an SDS 920 output word will cause the data link to be selected.

3.2 **Control dialogue translation**

When the data link has been selected in the manner described in 3.1.1, the remaining 6 bits of a PP function word cause the previous setting of the output flags to be completely renewed, with the exception of OF9 which is set and reset manually.

The setting of three particular output flags will cause interrupt signals to the SDS 920 (OF1, OF2, OF3) (see Table, Fig. 4). They request immediate action provided no higher priority interrupts (e.g. from experiment) have been sent to the SDS 920.

Three other output flags (OF7, OF8, OF9) do not request action but inform the SDS 920 of error and operative conditions. They are tested by a special SDS 920 instruction (Skip - if signal is not set).

The three remaining flags (OF4, OF5, OF6) are simply commands to the data-link electronics, preparing it for the exchange of data or status information.

As for the input flags, they are completely renewed according to the information contained in bits 12 to 18 of an SDS 920 output word, when the link is selected in the manner described in 3.1.2.
Two exceptions exist. IF5 indicates a parity error and can be set either by the SDS 920 when an error has occurred during an output block transfer, or by the data-link control when an error has occurred during an input block transfer.

IF8, like OF9, is set and reset manually by means of a "link operational" switch located on the data link control rack.

Both of them remain on after setting provided the d.c. supplies of the data link stay within some performant limits of their nominal values. Input flags are transmitted to the CDC 6600 following a CDC 6600 status request (Fig. 4).

Some precautions must be taken in order to avoid reading the input flags while they are being set. For this purpose the presence of the above-mentioned SYS signal delays the execution of any supervening 6600 status request.

Input flags are also available to one of the multiplexer sub-channel inputs. A "character ready" signal signifies the presence of information at this input. This signal is removed for the duration of the SYS signal.

By reading the input flags via the multiplexer at regular intervals, the CDC 6600 operating system finds out whether or not the link is operational and the SDS 920 is ready before allocating to one of the peripheral processors the task of inputting or outputting data over the link.

3.3 Format conversion and parity check

One 24-bit 920 word is converted into two 12-bit 6600 words.

First of all, the word is "jammed" into a 24-bit register. Whilst the least significant half of this word is transmitted to the CDC 6600, the parity bit of the most significant part is generated and stored. Four microseconds later the positions of the two halves of the data word are interchanged so that the second half is transmitted to the CDC 6600, while the parity is generated for the least significant half. The parity bits of these two halves are used to produce the parity of the
complete 24-bit word and this is then compared with the parity received from the SDS 920. If they differ IP5 is set.

Conversely, two 12-bit 6600 words are assembled into one 24-bit 920 word.

Again the above-mentioned register allows the two words to be assembled and a total parity bit to be generated before transmission to the SDS 920. The SDS 920 stores the parity bit received with each word and checks it as soon as the word is unloaded from the memory. If an error is found at that stage, IP5 is set. Of course, this should be programmed to happen within a certain time limit.

3.4 **Synchronization**

Two kinds of synchronization are provided. First, a programmed sequence so that communication between the two computers might be established in an orderly fashion. By setting various input and output flags, the two programmes become synchronized, this phase ending with both computers waiting. A hardware sequence then takes place so that the transfer of words might proceed one by one at the rate imposed by the SDS 920, which is the slowest of the two computers.

Figures 5 and 6 show the timing relation between the various signals involved during input and output sequences.

More detailed information about layouts and circuits is contained in a Data-Link System Manual.\(^6\)

4. **TEST PROGRAMME**

A comprehensive programme has been prepared in order to test all the features built into the data-link system (Fig. 7).

The choice of the type of test, the generation of patterns, and the checking are all done by the SDS 920.
This reduces the amount of peripheral processor programme to a minimum, and it is in accordance with the principle that the user of the data-link system makes his choice of programme and directs part of the CDC 6600 activities while sitting close to the 920, which by means of the link becomes a remote extension of the central computing system.

The operator selects a required sequence of tests, which then runs until another sequence is requested. There is a choice between a functional test (input flag test) or a block transfer test.

In the latter case, there is the possibility of choosing a type of pattern, which can be repetitive or random. Blocks of data are transferred over the link to the CDC 6600 and then transferred back to the SDS 920, where a check is made against the original pattern.

The test includes printing of various codes at both ends, should an error or an unknown situation be detected at various points during the execution of the programme.

A typewriter connected to the CDC 6600 via the multiplexer is used to input and output messages to and from that computer, and for this reason the 6600 part of the test is loaded together with a "TT" driver. This is another peripheral programme which allows the operator of the typewriter to dump, display or alter the contents of other peripheral programmes.

5. FUTURE DEVELOPMENTS

The data link described is intended to be the first item of a larger system.

Logically there is, in fact, room for expansion to up to eight data links.

As can be seen from the tentative block diagram of an eight-link configuration (Fig. 8), some elements can be shared by all the links. They are the Data Channel Adapter, the two multiplexer subchannels, the CDC 6600 control, a certain number of conversion registers, and eventually a small fast buffer memory.
Other elements, particular to each link, are input flags, output flags, control of the device connected to the link, kind of control, and data signals transmitted. These elements cannot be designed in detail a priori without knowing the device to be connected but their design will follow common logical lines so as to facilitate their insertion in the system when the need arises. The system is planned so that control is centralized as far as possible, and each link services one particular device.

The other alternative would have been to plan the system with uniform and standard characteristics, and to provide each device requiring connection to the link with a control and conversion unit. A further step would be to imagine a high-speed serial teletype line running all over the CERN site, into which devices could just "plug-in" via their control and conversion unit.

Considering that only a limited and selected number of experimental devices located in clearly defined places can require connection to the CDC 6600 in the near future, planning of a system along those lines does not seem very practical at the present, and it would certainly result in greater difficulties of design and maintenance and higher costs.
Acknowledgements

The basic ideas which lead to the construction of the data link described, emerged in the course of conversations with several people, among whom T. Bell (NF) and P. Mercer (DD), who is the author of the TT driver programme. Both of them were very helpful with programming advice.

The following people were involved in the execution of the project: J. S. Austin (AERE, Harwell) who arrived at CERN when on-line tests were commencing and took an active part in them; Mlle M. L. Mignaux (DD) who prepared a large part of the test programme; and S. Bunodière who gave valuable assistance in the course of testing and designed the power supply control.

The project was realized in co-operation with the following people: H. Thorlud (MFS) whose staff was responsible for laying the cables; and F. Iselin (NF) whose group prepared the SDS 920 interface unit.
References


4) SDS 900 Series Input/Output SDS 900006A.


Figure captions

Fig. 1  :  Transmitter-receiver circuit diagram.
Fig. 2  :  Layout of cables.
Fig. 3  :  Block diagram of data link.
Fig. 4  :  Table of input-output flags.
Fig. 5  :  Timing diagram: input block transfer.
Fig. 6  :  Timing diagram: output block transfer.
Fig. 7  :  Test programme flow chart.
Fig. 8  :  Tentative block diagram of an eight-link configuration.
4 Receivers on 1 card

4 Transmitters on 1 card

DATA LINK
Transmitter/ Receiver circuits

IEP 2715

Fig. 1
### INPUT FLAGS

<table>
<thead>
<tr>
<th>No</th>
<th>DENOMINATION</th>
<th>SET BY</th>
<th>BOM</th>
<th>920 ADDRESS BITS</th>
<th>TESTED BY</th>
<th>DCA BITS</th>
<th>STATUS RESPONSE</th>
<th>MUX BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP1</td>
<td>920 READY FOR O/P</td>
<td>920</td>
<td>30 060</td>
<td>18</td>
<td>MUX, DCA</td>
<td>0</td>
<td>13</td>
<td>0</td>
</tr>
<tr>
<td>IP2</td>
<td>920 READY FOR I/P</td>
<td>920</td>
<td>30 120</td>
<td>17</td>
<td>&quot;</td>
<td>1</td>
<td>23</td>
<td>1</td>
</tr>
<tr>
<td>IP3</td>
<td>920 WAITING FOR O/P</td>
<td>920</td>
<td>30 220</td>
<td>16</td>
<td>&quot;</td>
<td>2</td>
<td>43</td>
<td>2</td>
</tr>
<tr>
<td>IP4</td>
<td>920 WAITING FOR I/P</td>
<td>920</td>
<td>30 420</td>
<td>15</td>
<td>&quot;</td>
<td>3</td>
<td>103</td>
<td>3</td>
</tr>
<tr>
<td>IP5</td>
<td>INPUT PARITY ERROR</td>
<td>DLC</td>
<td>31 020</td>
<td>14</td>
<td>&quot;</td>
<td>4</td>
<td>203</td>
<td>4</td>
</tr>
<tr>
<td>IP6</td>
<td>OUTPUT PARITY ERROR</td>
<td>920</td>
<td>32 020</td>
<td>13</td>
<td>&quot;</td>
<td>5</td>
<td>403</td>
<td>5</td>
</tr>
<tr>
<td>IP7</td>
<td>0/F NO OF WORDS ERROR</td>
<td>920</td>
<td>34 020</td>
<td>12</td>
<td>&quot;</td>
<td>6</td>
<td>103</td>
<td>6</td>
</tr>
<tr>
<td>IP8</td>
<td>LINK OPERATIONAL</td>
<td>DLC</td>
<td></td>
<td></td>
<td></td>
<td>7</td>
<td>203</td>
<td>7</td>
</tr>
</tbody>
</table>

### OUTPUT FLAGS

<table>
<thead>
<tr>
<th>No</th>
<th>DENOMINATION</th>
<th>SET BY</th>
<th>FUNCTION CODE</th>
<th>DCA BITS</th>
<th>TESTED BY</th>
<th>920 ADDRESS BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP1</td>
<td>6600 REQUESTS O/P</td>
<td>DCA</td>
<td>1B</td>
<td>0</td>
<td>920 INTERRUPT 213</td>
<td></td>
</tr>
<tr>
<td>OP2</td>
<td>6600 REQUESTS I/P</td>
<td>&quot;</td>
<td>2B</td>
<td>1</td>
<td>920 INTERRUPT 214</td>
<td></td>
</tr>
<tr>
<td>OP3</td>
<td>ERROR FOUND</td>
<td>&quot;</td>
<td>3B</td>
<td>0 x 1</td>
<td>920 INTERRUPT 215</td>
<td></td>
</tr>
<tr>
<td>OP4</td>
<td>0/F SELECT</td>
<td>&quot;</td>
<td>4B</td>
<td>2</td>
<td>DLC</td>
<td></td>
</tr>
<tr>
<td>OP5</td>
<td>I/P SELECT</td>
<td>&quot;</td>
<td>10B</td>
<td>3</td>
<td>DLC</td>
<td></td>
</tr>
<tr>
<td>OP6</td>
<td>STATUS REQUEST</td>
<td>&quot;</td>
<td>14B</td>
<td>2 x 3</td>
<td>DLC</td>
<td></td>
</tr>
<tr>
<td>OP7</td>
<td>I/P PARITY ERROR</td>
<td>&quot;</td>
<td>20B</td>
<td>4</td>
<td>920 SES 00001</td>
<td>23</td>
</tr>
<tr>
<td>OP8</td>
<td>0/F NO OF WORDS ERROR</td>
<td>&quot;</td>
<td>40B</td>
<td>5</td>
<td>920 SES 00002</td>
<td>22</td>
</tr>
<tr>
<td>OP9</td>
<td>LINK OPERATIONAL</td>
<td>DLC</td>
<td></td>
<td></td>
<td></td>
<td>920 SES 00004</td>
</tr>
</tbody>
</table>