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KEK Preprint 94-143
November 1994
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Submitted to Nucl. Instrum. Meth., A.

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A Stacked Dielectric Film for a Silicon Microstrip Detector*

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Abstract

Stacked thick dielectric films have been developed so as to be applied to a silicon microstrip detector (SSD). We expected that these stacked films would have superior properties for an integrated capacitor in terms of a high dielectric breakdown characteristic, reliability, a large capacitance and radiation hardness. We measured the capacitance and leakage current for test capacitors with single-layered silicon dioxide (SiO_2), single-layered silicon nitride (Si_3N_4), NO (Si_3N_4 - SiO_2), ON (SiO_2 - Si_3N_4) and ONO (SiO_2 - Si_3N_4 - SiO_2).

*ver.4.2 November 7, 1994 / submitted to Nucl. Instr. & Meth. section A

1 Introduction

The double-sided silicon strip detectors (DSSDs)[1, 2] to be used in a KEK B-factory experiment will employ integrated capacitors in order to prevent the saturation of a preamplifier which should be isolated from leakage current. In order to fully spread a depletion layer, the bias voltage requires $50 \sim 70\text{V}$ for a detector having a thickness of $300\mu\text{m}$ and a resistivity of $5 \sim 7\text{k}\Omega \cdot \text{cm}$. In the case of DSSDs, the integrated capacitors are to be operated at relatively large voltages across the capacitor dielectric. Voltages across the capacitors from 0V to the operating bias voltages are to be applied.

The integrated capacitor should satisfy following requirements:

- The leakage current in the capacitor should be sufficiently small.
- The dielectric breakdown voltages should be sufficiently high.
- In order to obtain a large charge-collection efficiency, the capacitance of the integrated capacitor is to be as large as possible compared to the interstrip capacitance or the pn -junction capacitance.
- The number of dielectric breakdowns before the intrinsic dielectric breakdown voltage should be sufficiently small.
- The time dependent dielectric breakdown (TDDB) should be sufficiently long in order to operate the DSSDs for a long time.
- The radiation hardness should be high.

In order to satisfy these conditions, ON, NO and ONO dielectric films [3, 4] were chosen to be used for an integrated capacitor.

The dielectric constant of Si_3N_4 , i.e. $\epsilon_{\text{sn}} = 7.4$, is larger than that of SiO_2 , i.e. $\epsilon_{\text{ox}} = 3.9$. The leakage current for a single-layered Si_3N_4 is larger than that for a single-layered SiO_2 when their thicknesses are the same. Stacked dielectric

films are expected to have superior properties: a large capacitance, a high dielectric breakdown voltage, long-term TDDB, less dielectric breakdowns before the intrinsic dielectric breakdown voltage and radiation hardness. SiO_2 and Si_3N_4 have different current-transport mechanisms. The current in SiO_2 flows by Fowler–Nordheim emission [5, 6] and the current in Si_3N_4 flows by Poole–Frenkel emission [7]. Fowler–Nordheim emission takes place according to electrons’ tunneling in SiO_2 ; the Poole–Frenkel emission of holes’ is dominated by the so-called internal Schottky emission in Si_3N_4 . Since the SiO_2 dielectric film limits electrons which are injected from the electrode to the Si_3N_4 dielectric film, we can expect a sufficiently small leakage current using a stacked dielectric film. Since the combination of different materials compensates for any weak spots and pin holes in each material, we can obtain dielectric films having fewer dielectric breakdowns before the intrinsic breakdown voltage, and have a long-term TDDB.

When we require that the intrinsic breakdown voltage is higher than 200V, the thickness of a dielectric film is at least 200nm with single-layered SiO_2 . Although stacked dielectric films have been studied only as thin films (less than 20nm) to be used for DRAM and EEPROM so far, they have not been studied for thick films (up to 20nm).

In this article we discuss the capacitance and leakage current of stacked dielectric films. In section 2 we describe the preparation of test samples. In section 3, after we explain the experimental procedures and results, we provide some discussions. In section 4 we conclude the results.

2 Preparation of Test Elements

In order to study the property of the difference for the type of silicon substrate, we employed *n*-type and *p*-type silicon substrates. In order to neglect any voltage drop in a silicon substrate, we used *n*-type and *p*-type silicon substrates with a bulk resistivity of $5 \sim 7\Omega \cdot \text{cm}$ and $2 \sim 4\Omega \cdot \text{cm}$, respectively. The silicon substrates

were 525 μm thick, $\langle 100 \rangle$ oriented and polished to a mirror-like finish. The SiO_2 on the substrate and the SiO_2 on the Si_3N_4 are called “bottom SiO_2 ” and “top SiO_2 ”, respectively. Figure 1 shows the structure of a capacitor using an ONO dielectric film having bottom SiO_2 , Si_3N_4 and top SiO_2 in that order from a silicon substrate. The typical thicknesses of the dielectric films were measured using an ellipsometer.

The bottom SiO_2 was made by a thermal growing process from a silicon substrate at 900°C in wet O_2 environment. The thickness of bottom SiO_2 ranged from 6.3 to 205nm.

The Si_3N_4 was made by reacting dichlorosilan (SiH_2Cl_2) at a gas flow rate of 70sccm* and ammonia (NH_3) at 700sccm at a temperature of 740°C and a pressure of 95Pa. This process is called low-pressure chemical vapor deposition (LPCVD). The thickness of the Si_3N_4 ranged from 84 to 298nm.

The top SiO_2 was thermally grown from Si_3N_4 at 1000°C in wet O_2 environment for about 70min. This condition was equivalent to forming SiO_2 of $420\text{nm} \pm 20\text{nm}$ on a silicon substrate. We could not measure the thickness of the thermal SiO_2 upon Si_3N_4 using an ellipsometer since the difference of the thicknesses between Si_3N_4 and top SiO_2 was too big. We, however, estimated that its thickness was much thinner than 2nm, since no differences in the capacitance were observed between an ONO capacitor with top SiO_2 of thermal SiO_2 and an ON capacitor without top SiO_2 . Table 1 lists the configuration of test capacitors.

After the dielectric films were made on a silicon substrate, polysilicon was deposited on the dielectric film so as to define the capacitor area and on the backside of the substrate to provide a backside contact. The polysilicon was sufficiently doped by phosphorus. The patterns of the capacitors were formed by standard photoresist techniques. The capacitors were formed as circular disks with radii of 125, 250, 500 and 1004 μm , and with the areas of the capacitor of $5.23 \times 10^{-4}\text{cm}^2$, 2.03×10^{-3} , 7.98×10^{-3} and 3.17×10^{-2} , respectively.

*sccm stands for standard cubic centimeters per minutes.

3 experiments and discussions

3.1 Capacitance

All of the measurements were made at room temperature. Figure 2 shows a schematic diagram of the setup for the electrical measurements for devices under test (DUTs).

Capacitance measurements for the capacitors were made using an HP4194A Impedance/Gain-Phase Analyzer. The measurement frequency was $10kHz$ and the amplitude was $500mV$. We determined the capacitance per unit area by taking an average over four capacitor sizes ($r = 125, 250, 500$ and $1004\mu m$). The difference of the capacitance per unit area between the direct measurement and calculation from the thicknesses of the dielectric films was $\pm 2nF/cm^2$ in maximum.

Figure 3 shows the capacitance of the capacitors using the SiO_2 , Si_3N_4 ON, NO and ONO dielectric films. The thickness ratio of $SiO_2:Si_3N_4$ in the ONO dielectric film was approximately 1:4. The capacitance per unit area (C_0) can be calculated using

$$C_0 = \frac{\epsilon_0}{\frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{sn}}{\epsilon_{sn}}}, \quad (1)$$

where ϵ_0 is the permittivity in a vacuum, ϵ_{ox} and ϵ_{sn} are the dielectric constants, and t_{ox} and t_{sn} are the thicknesses for SiO_2 and, Si_3N_4 , respectively. The solid, dotted and dashed lines were calculated using equation (1) of the ONO, SiO_2 and Si_3N_4 , respectively. The measured capacitance was consistent with the estimated value based on the measured thickness using an ellipsometer.

The capacitance of the ONO was approximately 1.7-times larger than the capacitance of single-layered SiO_2 when the thicknesses of capacitors were the same. The capacitance depended only on the thickness and the ratio of SiO_2 to Si_3N_4 .

3.2 Leakage Current

All of the measurements were made at room temperature in a dark box. We applied bias voltages and measured the current with a Keithley Model 237 high voltage source measure unit.

Approximately $200nm$ of single-layered SiO_2 is used for conventional integrated capacitors in an SSD. We measured current-vs.-voltage property for an integrated capacitor on a p^+ -strip in an SSD. The thickness of single-layered SiO_2 was $205nm$. Silicon strips with integrated capacitors were $6.5cm \times 5\mu m$. A schematic diagram of the measurement set up is shown in figure 4. A p^+ -strip was ground, and voltage was applied to a gate electrode. We swept the applied voltage at steps of $1V$. Figure 5 shows the typical current-vs.-voltage property for an integrated capacitor using $205nm$ SiO_2 on an SSD. Current produced by positive voltage was less than that by negative voltage. When positive voltage is applied to a gate electrode, the majority carriers (holes) in a p^+ -strip are swept away from the dielectric film by electric force, and a depletion region develops. The number of injected carriers to the dielectric film, therefore, become small. The applied voltage is divided between the dielectric film and the depletion region. When negative voltages are applied to a gate electrode, the majority carriers in the p^+ -strip are accumulated on a dielectric film. Fully applied voltages are across the dielectric film. In order to study the properties of the dielectric films, we decided that the voltage should applied to the accumulated direction. When we used test samples on an n -type silicon substrate, we could observe injected electrons from the silicon substrate and/or injected holes from the polysilicon gate electrode.

The setup for the electrical measurements was also same as that shown in Figure 2. The measured current divided by the area of capacitor equals the current density. We, therefore, used $1004\mu m$ -radius capacitors which had the largest area among the test samples, in order to observe the low-current density. We applied voltage in the accumulation-direction from a polysilicon gate electrode on a dielec-

tric film with a step of approximately $0.5MV/cm$ in term of the average electric field. The average electric field was derived from the applied voltage divided by the total geometrical thickness of the dielectric film. In order to fill up the traps in the dielectric film for each voltage step, it took $100 \sim 20000sec$ before the current reached a steady state condition, i.e. $\Delta I/I \leq 0.05\%/sec$, or the current decreased below the measurement limit, i.e. $I \leq 10^{-13}A$. The lower limit of the measurement was approximately equal to $10^{-10}A/cm^2$.

Since we wished to make a comparison with the leakage current for dielectric films, we introduced an effective electric field (E_{eff}). We normalized the thickness of the dielectric film in terms of SiO_2 equivalent as defined in the following discussion. Since the electric flux density was conserved, we supposed no charge in dielectric film;

$$\epsilon_{ox}\epsilon_0 \frac{V_{ox}}{t_{ox}} = \epsilon_{sn}\epsilon_0 \frac{V_{sn}}{t_{sn}}, \quad (2)$$

where V_{ox} and V_{sn} are the voltages across SiO_2 and Si_3N_4 , respectively. The applied voltage (V_0) is divided into SiO_2 and Si_3N_4 ;

$$V_0 = V_{ox} + V_{sn}. \quad (3)$$

From Eqs. (2) and (3), we obtain

$$\frac{V_{ox}}{t_{ox}} = \frac{V_0}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{sn}} \cdot t_{sn}}. \quad (4)$$

Therefore, the normalized thickness (t_{eff}) become

$$t_{eff} \equiv t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{sn}} \cdot t_{sn}. \quad (5)$$

We defined the effective electric field are

$$E_{eff} \equiv \frac{V_0}{t_{eff}}. \quad (6)$$

Figure 6 shows the current density vs. the effective electric field for single-layered SiO_2 dielectric films. After the last point of the plots, the dielectric films were broken. The current conduction for the electric field did not have any thickness

dependence. The Fowler–Nordheim conduction depends only on the electric field. For the silicon substrate dependence, the leakage current in $205nm$ SiO_2 using a p -type silicon substrate was less than that in $205nm$ SiO_2 using an n -type silicon substrate. The difference of Fermi-level between the n -type silicon substrate and the n -type polysilicon was about $0.2eV$. When the barrier height for electron is also changed according to variation of the Fermi level, we can explain the difference of the leakage current between using n -type silicon substrate and p -type silicon substrate.

Figure 7 shows the current density vs. the effective electric field for single-layered Si_3N_4 dielectric films. A thicker Si_3N_4 dielectric film had a smaller leakage current. The leakage current between $157nm$ Si_3N_4 on n -type silicon substrate and $157nm$ Si_3N_4 on p -type silicon substrate was not different.

When we made a Si_3N_4 layer onto a silicon substrate we could assume that the surface of silicon was oxidized with thin natural SiO_2 , which played the role of bottom SiO_2 . The estimated thickness of the natural SiO_2 was less than $2nm$ thick. We recognized that the single-layered Si_3N_4 actually consisted of natural SiO_2 and Si_3N_4 in that order. Figure 8, therefore, shows the current density vs. the effective electric field for ON which had a fixed thickness of $157nm$ Si_3N_4 , and varied the thickness of the bottom SiO_2 . When the bottom SiO_2 was thin, the leakage current for ON dielectric films was small. We can explain this phenomena as follows. If electrons are injected into thick SiO_2 , the injected electrons are accelerated by the electric field for a long distance in the SiO_2 conduction band. The thicker SiO_2 provides more energy for the electrons. In thick SiO_2 , the electrons have a good chance to excite another electron in the valence band to the conduction band. In thinner SiO_2 , electrons have less energy. The current for ON with thinner bottom SiO_2 , therefore, flows smaller than that for ON with thicker bottom SiO_2 . The leakage current for ON with $6nm$ bottom SiO_2 on an n -type silicon substrate was larger than that for ON with $6nm$ bottom SiO_2 on a p -type silicon substrate. Since the majority of conduction carriers in a SiO_2 dielectric film comprises electrons[8, 9], the leakage current depends on the kinds of injected carriers from the silicon

substrate: electrons are injected from the *n*-type silicon substrate and holes are injected from the *p*-type silicon substrate.

Figure 9 shows the current density vs. the effective electric field of ONO, ON, NO, SiO₂, Si₃N₄ and ONO on a *p*-type silicon substrate. Single-layered SiO₂ showed the lowest electric field for breakdown and the highest current density. On the other hand, the NO dielectric film showed the highest electric field for breakdown and the smallest current density. The NO also accompanies natural SiO₂ between silicon and Si₃N₄. When we inject carriers from a polysilicon electrode, the top SiO₂ decreases the current transport effectively. The difference between the Si₃N₄ and NO is due to the existence or nonexistence of top SiO₂. The difference between the ON and ONO is also due to the existence or nonexistence of top SiO₂. Top SiO₂ effectively plays the role of a barrier for holes from a polysilicon electrode. When we compared the property for an ONO dielectric film with that for an NO dielectric film, the NO dielectric film was better. We should therefore produce an ONO dielectric film with thin bottom SiO₂. The leakage current for ONO with 37nm bottom SiO₂ on an *n*-type silicon substrate was larger than that for ONO with 37nm bottom SiO₂ on a *p*-type silicon substrate. Just as in the same context discussed for figure 8, we can say that the majority of conduction carriers in a SiO₂ dielectric film comprises electrons. When a voltage of 100V is applied to a 200nm SiO₂ dielectric film, the electric field on it is 5MV/cm. The area of the readout capacitor on a silicon strip detector was typically $3.25 \times 10^{-3} \text{cm}^2/\text{strip}$. In order to obtain the low noise level, we have demanded that the leakage current in the dielectric film is under 1pA/strip, i.e. 0.3nA/cm². The leakage current for all test samples was sufficiently less than 0.3nA/cm² at 5MV/cm. Since the bias voltage was supplied for a very long time, approximately over one day from the start of the sweep until a breakdown, the dielectric breakdown included the effect of TDDB. Test samples satisfied the minimum requirement of the breakdown electric field.

4 Conclusion

This article provides data concerning thick stacked dielectric films, single-layered SiO₂ and single-layered Si₃N₄. We evaluated these dielectric films in terms of their capacitance and current transport. The capacitance of ONO was approximately 1.7-times larger than that of single-layered SiO₂. When we applied voltage to inversion-direction, the leakage current became small owing to the rejection of the majority carrier from insulator and the development of the depletion region. When we applied voltage to accumulation-direction for SiO₂, the leakage current for hole injection from a substrate was less than that for electron injection from a substrate. The leakage current in SiO₂ flows by the Fowler–Nordheim emission owing to tunneling at cathode electrode by electrons and that in Si₃N₄ flows by the Poole–Frenkel emission owing to conduction with the internal Schottky emission by holes. Owing to these mechanisms, ONO flowed less leakage current. We understood that the thinner SiO₂ layer on the side of electron injection passed less current. We found that ONO was more useful than thick single-layered SiO₂; the leakage currents for single-layered SiO₂ and ONO dielectric film were $7.0 \times 10^{-7} \text{A/cm}^2$ and $1.0 \times 10^{-10} \text{A/cm}^2$ at 7MV/cm, respectively. We can therefore conclude regarding the leakage current that the better dielectric film is the ONO type, which is covered with thin SiO₂ dielectric films with less defects.

Acknowledgement

The authors sincerely appreciate the co-operation of the silicon micro-vertex detector group for KEK B-factory and of J. Yamanaka, M. Kamiya and S. Miyahara from Seiko Instruments Inc.. The directors of KEK, Profs. H. Sugawara, Y. Kimura, S. Iwata, and F. Takasaki are appreciated for their continuous encouragement.

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List of Tables

1	Test samples.	13
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Table 1: Test samples.					
	bottom SiO ₂	Si ₃ N ₄	top SiO ₂	n-type	p-type
SiO ₂	9nm	—	—	○	
	37nm	—	—	○	
	205nm	—	—	○	○
Si ₃ N ₄	—	83nm	—	○	
	—	157nm	—	○	○
	—	298nm	—	○	
ON	6nm	157nm	—	○	○
	20nm	157nm	—	○	
	37nm	157nm	—	○	
NO	—	157nm	< 2nm	○	
ONO	37nm	157nm	< 2nm	○	○

Open circles shows prepared samples.

List of Figures

1	Structure of a capacitor using ONO dielectric film.	15
2	Experimental setup.	15
3	Capacitance of single-layered SiO ₂ , single-layered Si ₃ N ₄ ON, NO and ONO.	16
4	Measurement setup for a conventional integrated capacitor on a SSD.	17
5	Polarity dependence of the current-transport property for an integrated capacitor using 205nm SiO ₂ on a SSD	18
6	Current-conduction property for the single-layered SiO ₂ dielectric films.	19
7	Current-conduction property for the single-layered Si ₃ N ₄ dielectric films.	20
8	Current-conduction property for the ON dielectric films which varies with the bottom SiO ₂ thickness.	21
9	Current conduction property for ONO, ON , NO, SiO ₂ , Si ₃ N ₄ and ONO dielectric films on the p-type silicon substrate.	22

Figure 1: Structure of a capacitor using ONO dielectric film.

Figure 2: Experimental setup.

Figure 3: Capacitance of single-layered SiO₂, single-layered Si₃N₄, ON, NO and ONO.

Figure 4: Measurement setup for a conventional integrated capacitor on a SSD.

Figure 5: Polarity dependence of the current-transport property for an integrated capacitor using 205nm SiO₂ on a SSD

Figure 6: Current-conduction property for the single-layered SiO_2 dielectric films.

Figure 7: Current-conduction property for the single-layered Si_3N_4 dielectric films.

Figure 8: Current-conduction property for the ON dielectric films which varies with the bottom SiO_2 thickness.

Figure 9: Current conduction property for ONO, ON, NO, SiO_2 , Si_3N_4 and ONO dielectric films on the p -type silicon substrate.