The Compact Muon Solenoid Experiment
Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

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Longevity studies and Phase 2 electronics upgrade for CMS Cathode Strip Chambers in preparation for HL-LHC

Bingran Wang for the CMS Collaboration

Abstract

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Longevity studies and Phase 2 electronics upgrade for CMS Cathode Strip Chambers in preparation for HL-LHC

Bingran Wang
On behalf of the CMS Muon Group
Northeastern University, USA

Abstract

The Cathode Strip Chamber (CSC) is the primary system for muon detection in the CMS endcap region. Starting in 2026 both the instantaneous luminosity and CMS level 1 latency will be increased significantly, which will exceed the design specifications of the CSC electronics. The large integrated particle flux also increases the potential for chamber aging and performance degradation. This paper presents the studies of CSC electronics and CSC longevity performed at the CERN GIF++ facility.

1. Introduction

Figure 1: CSC layout (left) and signal development on anode and cathode (right)

The Cathode Strip Chamber (CSC) is a gaseous ionization detector used for muon detection, triggering and track reconstruction [1]. Each CSC chamber

4 has six layers of anode wires and cathode strips with high voltage applied to
 5 the anode planes (Figure 1). A charged particle passing through the detector
 6 ionizes the gas mixture (40% Ar, 50% CO₂, and 10% CF₄), and in the strong
 7 electric field in the vicinity of an anode wire an avalanche of charged particles is
 8 created which produces an electrical signal on the anode and an induced charge
 9 distribution on the cathode plane. Because the cathode plane is divided into
 10 strips a precise position orthogonal to the strip direction can be deduced. This
 11 is combined with a less precise position from the anode wires to give a 2D hit
 12 position on each layer. These hits on the six layers in a chamber are combined
 13 into straight-line muon track segments, that are used as input to the full muon
 14 track reconstruction.

Figure 2: Quarter view of CMS

15 There are 540 CSCs in CMS. Each CMS endcap has four stations of CSCs
 16 (Figure 2). Station 1 has three rings of chambers while station 2 to 4 each
 17 have two rings of chambers. Muon track reconstruction uses a Kalman filter
 18 technique to combine the segments in multiple stations with a track from the
 19 inner Tracker. The momentum of the muon is estimated from the bending of
 20 the track in the CMS solenoidal magnetic field.

Figure 3: HL-LHC background rate extrapolated from run-1 data

From 2026 the luminosity of LHC will be boosted to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, which is 7.5 times higher than the original LHC design, and the CMS level-1 (L1) trigger latency will also be nearly 3.5 times higher. The short term effect is that the current CSC electronics will not be able to accommodate the high rates, and the long term effect is the possibility of chamber aging and performance degradation from high integrated luminosity, which is expected to reach 4000 fb^{-1} . This motivates studies of electronics upgrades and chamber longevity, especially for the most forward CSCs (ME1/1 and ME2/1) since they will experience the highest particle rates (Figure 3) [2].

2. Electronics Upgrade

Figure 4 shows an overview of the CSC electronics upgrades. The main upgrade focuses on the inner ring chambers, and it includes both on-chamber and off-chamber electronics.

2.1. Cathode Front-End Board (CFEB) Upgrade

The CFEB is an electronic board for readout of the cathode strips. Each strip uses 96 capacitors in a Switched Capacitor Array (SCA) on the CFEB to store the charge induced on the strips as it awaits digitization. Twelve blocks

Figure 4: CSC electronics layout before (left) and after (right) upgrades for ME234/1

are used to group these 96 capacitors, and each event uses two blocks for storage,
so the SCA of a strip can store up to 6 events.

Figure 5: Simulated CFEB data loss of inner ring CFEBs and ME2/1 DCFEB

The expected number of events in the SCA is Poisson distributed and is proportional to the trigger rate and L1 latency, both of which will be increased in HL-LHC and may lead to data loss due to limited CFEB storage. Figure 5 shows the expected CFEB data loss as a function of instantaneous luminosity. At the HL-LHC data rate, all the inner ring chambers would have unacceptable data losses, and thus upgrades to the electronics are needed.

The upgraded version of the CFEB is the Digital Cathode Front-End Board

Figure 6: Comparison between CFEB and DCFEB

(DCFEB) (Figure 6). The design of the DCFEBs for HL-LHC is based closely on a successful DCFEB board that was installed in the ME1/1 ring in 2014. It uses Flash ADCs (Analog-to-digital converter) to digitize the strip signals continuously, and stores the digitized signals in the deep pipeline of a Virtex-6 FPGA. This upgrade will significantly reduce the event loss at HL-LHC (Figure 5).

2.2. Anode Local Charged Track (ALCT) Upgrade

The ALCT board reads signals from the AFEB (Anode Front-End Board) and finds hit patterns to form an anode trigger. The ALCT boards at present use Virtex E FPGA (except for ME1/1 and ME4/2), whose pipeline length cannot cope with the L1 latency at HL-LHC, so the FPGA needs to be upgraded to Spartan 6.

2.3. Other Electronics Upgrades

The inner ring chambers in station 2 to 4 are currently using copper readout, which has a limited bandwidth of 1.6 Gbps. The higher data rate at HL-LHC requires at least a three times larger DAQ rate for the inner ring chambers, so their copper readout will be upgraded to optical links. The trigger and data

64 motherboards (TMB and DMB) will also be upgraded to optical trigger and
 65 data motherboards (OTMB and ODMB) with more powerful FPGAs.

66 ME1/1 chambers experience the highest level of radiation in the CSC system.
 67 The EPROM used in the ME1/1 ALCTs and DCFEBs is not radiation hard, and
 68 can sometimes suffer firmware failure. Therefore, a fast optical programming
 69 path via GBTx will be implemented to allow recovery from such a failure.

70 3. Longevity Study

Figure 7: The GIF++ layout, with the typical radiation exposure shown at different locations. The temperature scale is in the unit of micro-gray per hour

71 Gas ionization causes plasma reactions that may damage the chamber via
 72 corrosion, deposition, or cracks on the wires. The high integrated luminosity of
 73 HL-LHC may lead to chamber damage, thus reducing operational stability and
 74 deteriorating performance. The CERN GIF++ facility (Figure 7), built around
 75 a muon test beam, employs a 14 TBq ^{137}Cs source to produce a high radiation
 76 environment.

77 The CSC aging study included measurements of dark and source trigger
 78 rates, gas gain (a measure of avalanche size), inter-strip resistance, and dark
 79 currents. Polymerization on anode wires can increase wire diameter and cause
 80 a reduction in gas gain. Two CSCs (ME1/1 and ME2/1) have been irradiated
 81 up to an accumulated charge equivalent to three times that expected at the

Figure 8: ME1/1 relative gas gain

82 maximum HL-LHC integrated luminosity, and no noticeable decrease in gas
 83 gain has been observed (Figure 8). All other recorded parameters (dark current,
 84 dark rate, inter-strip resistance, etc.) were stable throughout the irradiation as
 85 well.

86 There is no evidence of significant chamber damage under HL-LHC condi-
 87 tions, but the high radiation dose may still degrade chamber performance. The
 88 muon test beam in GIF++ is used to study the performance after successive
 89 periods of irradiation with the ^{137}Cs source, and with the high background
 90 occupancy provided by this source.

91 Spatial resolution is an essential characteristic of CSC performance. An
 92 estimate of the resolution can be obtained by comparing the hit position on one
 93 layer with the expected position obtained from the segment formed from the hits
 94 on the other 5 layers. The study in GIF++ shows that increased instantaneous
 95 luminosity could cause a 10% deterioration in resolution, but it is stable up
 96 to an integrated luminosity equivalent to three times the expectation for HL-
 97 LHC (Figure 9), so CSC performance degradation is unlikely to be an issue at
 98 HL-LHC.

Figure 9: ME1/1 spatial resolution

99 4. Summary

100 In the absence of upgraded electronics, the inner rings of the CSC system
 101 are not able to digest the higher trigger and data rates, and CMS level-1 trigger
 102 latency, expected at HL-LHC. We have presented several improvements to both
 103 on-chamber and off-chamber electronics, including the CFEB, ALCT, DMB,
 104 and TMB boards, and the copper readout. Studies have also shown that the
 105 integrated radiation will not cause any significant chamber aging or performance
 106 degradation. Therefore, the upgraded CSC system will operate reliably in HL-
 107 LHC.

108 References

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