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RADIATION DAMAGE INVESTIGATION FOR THE DESIGN OF A HARDENED FAST BIPOLAR MONOLITHIC CHARGE SENSITIVE PREAMPLIFIER

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Abstract

In order to implement a high-speed, radiation hardened, Charge Sensitive Preamplifier (CSP) in the monolithic $2\mu\text{m}$ BiCMOS technology (called HF2CMOS), the performance of the available NPN and PNP transistors were measured, before and after neutron irradiation. Furthermore, also monolithic CSPs, realized with the same technology, were irradiated and investigated. Results on the neutron irradiation effect on the base spreading resistance ($r_{bb'}$) of the CSP input NPN-transistor are presented. Design strategies, to reduce the radiation damage effects in the CSP performance, were studied. Results confirm that the HF2CMOS process is suitable to sustain the radiation environment of the future LHC collider. A design for a new CSP version is proposed. A novel method for measuring the series noise of the CSP, at large input capacitances, was used. The method minimized the errors caused by the CSP rise-time.

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1. INTRODUCTION

Detector read-out channels for future LHC collider experiments face stringent requirements regarding speed, noise, and radiation hardness. High speed of operation is required, since very short shaping time of the detector signals is necessary, for the foreseen, high interaction, event rate. Radiation hardness is needed, since the electronics must be close to the detector and the expected radiation environment, in the highly exposed regions, is a neutron fluence of about $10^{14}n/(cm^2 \text{ year})$ and a dose of photons and charged particles of a few Mrad/year.

The goal of this research is to implement a low-noise, high-speed, radiation hard, monolithic Charge Sensitive Preamplifier (CSP) using BiCMOS technology [1, 2] (called HF2CMOS). Discrete HF2CMOS devices and preliminary CSP prototypes were tested, before and after irradiation with neutron fluences, ranging from about $10^{12}n/cm^2$ to $3 \times 10^{14}n/cm^2$. The obtained results, enable to evaluate neutron radiation effects on the performance of the future CSP, in order to study proper design for the increase of CSP radiation hardness.

The short shaping-time range of operation (tens of nsec) makes the use of a Bipolar Junction Transistor (BJT) input device [3] advantageous in terms of noise and are, therefore, employed in the realized CSP. A low series noise, for low biasing currents, is obtained and the parallel noise of the input device affects negligibly the total noise performance. Thus, discrete, HF2CMOS BJT devices and CSPs were irradiated and tested.

A new design of the dimension of the input NPN device, based on the irradiation results obtained for both the HF2CMOS CSP and NPN transistor, and the silicon detectors to be used [4], is analyzed.

The measurements of the radiation effects on the BJTs devices (HF2CMOS process) and the noise performance of the CSP, before and after the irradiation, are presented. A novel series noise measurement set-up was used for finding $r_{bb'}$. The method reduces the error introduced by the CSP rise time in the extraction of the noise parameters. The design of a new radiation hardened CSP, is described.

2. INVESTIGATION OF IRRADIATED BJTs

The read-out electronics of experiments at LHC will be exposed to high fluences of neutrons and a dose of photons and charged particles. The two types of radiation cause different effects in BJT and MOS devices. BJT devices are less sensitive to photon radiation, but their performance is

being degraded by neutron irradiation, which creates generation-recombination (G-R) centers into the energy gap of the semiconductor. These centers diminish the minority carrier mean life-time and increase the recombination current, thus, the base current, I_B . As a result, the current gain, β , decreases. The induced neutron degradation in BJTs, is inversely proportional to their transition frequency (f_T) [5], which is very large in the NPN ($f_T = 6GHz$) and in Vertical Isolated PNP transistors ($f_T = 2GHz$), available in HF2CMOS.

MOS devices are less sensitive to neutron radiation, being majority carrier devices (the only effect is an increase of the $1/f$ noise); but ionizing radiation, like charged particles or photons (which produce free charges), may damage this kind of devices. In fact, the free charges, generated in the silicon bulk, can fully recombine, while in the silicon oxide the recombination is limited. Therefore, irradiation causes an accumulation of charge in the oxide, which may modify the characteristics of the MOS device [5] and results, mainly, in a threshold voltage shift and transconductance change.

The high operation speed imposed by the event rates, requires the use of a BJT input device. For this reason, great attention has been given to BJT transistors (both NPN and PNP, produced in HF2CMOS technology). Their radiation hardness properties were studied, before and after irradiation, with neutrons.

The irradiations were done at two different laboratories, at CBNM (Geel, Belgium) up to a fluence of $1.3 \times 10^{13}n/cm^2$ and at the PSAIF facility (CERN) at $3 \times 10^{14}n/cm^2$. At the CBNM facility the detectors were exposed to neutrons with an energy of about 2 MeV. The neutrons were produced by a proton beam, accelerated by a Van de Graaf machine onto a tritium target. A maximum fluence of $4.5 \times 10^{13}n/cm^2$ was obtained. At the CERN-PSAIF facility, a fluence of $3 \times 10^{14}n/cm^2$ was obtained with neutrons of an energy around 1 MeV, produced by a proton beam, incoming on a fixed target. The neutron spectrum had an important low energy component. At both facilities, the values of the fluence was determined by measuring the activation of indium foils.

A net increase of the base current, I_B , caused by the trapping of the minority carriers in the G-R centers, after irradiation, results in a lower current gain, β , for low collector current, I_C , since in this case, the contribution of generation-recombination becomes significant with regard to the drift contribution.

The decrease of β , due to a $1.3 \times 10^{13}n/cm^2$ neutron irradiation, at low I_C values for HF2CMOS NPN transistors can be seen in Fig. 1, where the percentage of β modification is plotted as a function of I_C . All the irradiated transistors were of the smallest area permitted by HF2CMOS

technology. After irradiation, a decrease of the current gain (β) of less than 20% for $I_C > 50\mu A$, was found. Nevertheless, this variation does not impair the usage of NPN transistors for this specific application.

The same studies were performed for a lateral PNP device. In Fig. 2 it can be seen that the β reduction for an L-PNP transistor, at the same fluence ($1.3 \times 10^{13} n/cm^2$) is larger than that of the NPN. This is due to the dependence of the induced neutron degradation in BJT with the device transition frequency (f_T) [5]. The relationship between $(1/\beta)$ and the neutron fluence ϕ is:

$$\Delta \left(\frac{1}{\beta} \right) = \frac{\phi}{2\pi f_T K} \quad (1)$$

where K is the damage constant.

For the available devices, the transition frequency of the L-PNP is smaller ($f_T = 20MHz$) than that of the NPN ($f_T = 6GHz$).

The new available Vertical PNP transistors for a stronger irradiation ($3 \times 10^{14} n/cm^2$) had a β variation of less than 75%, from about 100 to 25, for a standing current I_C larger than $150\mu A$, as shown in Fig. 3. Although this degradation is quite large, it will be shown that a proper design can make its effect negligible to the overall CSP performance.

3. INVESTIGATION OF NON- AND IRRADIATED CSP

The CSPs (Fig. 4) [1] were irradiated at the Dubna facility, at a neutron fluence of up to $10^{14} n/cm^2$, at the CERN PSAIF facility at $3 \times 10^{14} n/cm^2$ fluence, and at the $\Sigma \Sigma$ facility, Bucharest, up to $1.1 \times 10^{14} n/cm^2$.

a. Set-up for series noise measurements

The value of the base spreading resistance, $r_{bb'}$, was determined by measuring its effect on the series noise of the device. The set-up used is shown in Fig. 5. The Device Under Test (DUT) is the input element of the CSP.

The output of the preamplifier feeds a bandpass filter with multi poles and zeros, having the same roll-off time constant, τ , and transfer function:

$$T_f(j\omega) = \frac{(j\omega\tau)^n}{(1 + j\omega\tau)^{(n+m)}} \quad (2)$$

where n is the number of zeros and $m+n$ the number of poles. The noise is proportional to the Root Mean Square (RMS) voltage at the output of the chain. The gain was calibrated by injecting a small charge, Q_i ($Q_i = V_i C_T$, V_i being a step voltage) at the CSP input. The Equivalent Noise Charge (ENC), the RMS charge to be injected at the CSP input for obtaining a signal to noise ratio equal to one, satisfying $V_0(t_{\max})/Q_i = V_{0RMS}/ENC$, is [3]:

$$ENC = \left[\frac{\alpha}{\tau} (C_D + C_f + C_i + C_T)^2 \bar{e}_a^2 + \beta \tau \bar{i}_a^2 \right]^{1/2} \quad (3)$$

where C_D is the capacitance simulating the detector, C_f is the feedback capacitance, C_T is the injection capacitance, and C_i is the input capacitance of the CSP; α and β are coefficients depending on the number of poles and zeros of the filter (Eq.(2)) and τ is the filter time constant. $\bar{e}_a^2 = 4kT(r_{bb'} + 0.5/g_m)$ is the series noise of the DUT, given by the base spreading resistance, $r_{bb'}$, and the collector shot noise, $0.5/g_m$; $\bar{i}_a^2 \approx 2qI_B$ is the parallel noise of the base current, T is absolute temperature, and k is the Boltzmann constant.

Usually, the procedure for extracting the series noise is as follows: a low time constant τ which makes the contribution of the parallel noise negligible, is chosen. For each C_D , at different increasing values, the noise is measured. Thus, ENC becomes linearly dependent on C_D , with a slope proportional to the square root of $\bar{e}_a^2$ (Eq.(3) for large C_D values).

So far, a non negligible systematic error is introduced in the measurement. With bipolar devices the parallel noise is relatively large, thus, the best choice is to get τ as small as possible, otherwise the parallel noise may add to ENC a non-negligible term. But the value of τ must be larger than the rise time, t_r , of the CSP, otherwise t_r affects the noise measurements.

The effect of the CSP rise time can be taken into account by adding a further pole to the filter transfer function:

$$T'_f(j\omega) = \frac{1}{1 + j\omega(2.2t_r)} \frac{(j\omega\tau)^n}{(1 + j\omega\tau)^{(n+m)}} \quad (4)$$

If t_r approaches τ , Eq.(3) which is based on the ideal transfer function of Eq. (2), is no longer valid, and the pole, due to t_r , should be taken into account in the evaluation of ENC.

Another problem, correlated with t_r , is the following: at first approximation t_r is given by

$$t_r \sim t_0 \frac{C_D + C_T + C_f + C_i}{C_f} \quad (5)$$

where t_0 depends on the CSP. From Eq.(5) it is evident that, for increasing values of C_D , t_r increases,

limiting the possibility of an accurate extraction of the noise parameters from the measured noise with very large C_D s, as needed with bipolar devices.

One possible way to correct this error is to take into account Eq.(4) in the calculation of ENC, but a complicated formula would be obtained. Moreover, this requires the measurement of both the RMS noise and t_r for each value of C_D .

We used instead, a simple and very efficient way for avoiding the error due to t_r , based on the following consideration: from Eq.(3) we see that the series noise is proportional to the sum of C_D, C_T, C_i , and C_f , regardless of their relative values. Simultaneously, the rise time t_r of the CSP, given in Eq.(5), is proportional to the ratio of the above sum and the feedback capacitance C_f , regardless of their absolute values. If, each time we change C_D we change also C_T and C_f by the same factor, we satisfy at the same time both the condition of increasing ENC and maintaining t_r constant, thus, also the overall transfer function. A second dominant pole, in the open loop response of the CSP, given by $1/C_f R_0$, where R_0 is the open loop output impedance of the preamplifier, may limit the frequency response of the CSP, for large values of C_f . Then, low values for R_0 are required. This can be obtained by simply increasing the bias current of the output stage to a suitable level, since R_0 is inversely proportional to its transconductance [6].

b. Results and discussion

This new method was used to measure the effect of neutron irradiation on the monolithic CSP made by the HF2CMOS process [1].

As can be seen in Fig. 5, a bandpass filter is connected at the output of the CSP. The general purpose filter was set as an RC-CR filter with one pole and one zero (where $n=m=1$, (Eq.2)). In Fig. 6, ENC versus C_D , for two different shaping times (τ), 100ns and 200ns, is presented.

In all the measurements, a feedback gain $([C_D + C_T + C_f + C_i]/C_f)$ of 15 was set, obtaining $t_r < 20nsec$. It can be seen that despite the range (200pF to 6800pF) of C_D , the results are straight lines for both curves, as predicted from Eq.(3). The ratio of the two slopes is $\sqrt{2}$, the expected square root of the ratio of the two time constants used.

The obtained straight lines enable extrapolation of the series noise parameters, in a simple way, from Eq.(3). Without this method, the two curves would have exhibited saturation at a relatively low value of C_D , preventing the use of Eq.(3) for the calculation of the series noise. The value for $r_{bb'}$ for the evaluated sample was found to be about 300Ω .

Fig. 7 shows the histogram of the obtained $r_{bb'}$, before irradiation, taken from two different

wafers. The area of the input NPN transistor of the evaluated CSPs is three times larger than the minimal area. The average $r_{bb'}$ of the first batch (Fig. 7a) was $233\ \Omega$ and of the second batch (Fig. 7b) was 313Ω . It can be seen that the expected spread of the values is, from wafer to wafer, within 34%.

Samples with higher $r_{bb'}$ (average , before irradiation was 313Ω) were irradiated at the Dubna facility (up to neutron fluence of $10^{14}n/cm^2$) and at the CERN PSAIF facility at $3 \times 10^{14}n/cm^2$ fluence. In the Dubna facility, the neutrons (generated by a nuclear reactor) had a mean energy spectrum, which in lethargy units has a peak at about 1.5 MeV. The $r_{bb'}$ increased with irradiation and measurements, after a few months, were published [7]. However, about three years after the irradiations, the $r_{bb'}$ values were between 235 to $245\ \Omega$ (23% lower than the $r_{bb'}$ values before irradiation). This indicates that there is a self annealing process. Furthermore, successive irradiation was carried out.

Samples with lower $r_{bb'}$ (average, before irradiation was 233Ω) were irradiated at the $\Sigma\Sigma$ facility, Bucharest, where a maximum fluence of $9.9 \times 10^{13}n/cm^2$ was obtained. The neutrons, produced by a nuclear reactor and moderated by filters, had a mean energy spectrum which, in lethargy units has a peak at about 1 MeV [8]. The fluences were determined by using three fission chambers. Measurements after irradiation at $1.1 \times 10^{13}n/cm^2$, $4.5 \times 10^{13}n/cm^2$, and $1.1 \times 10^{14}n/cm^2$, were performed. The results are presented in Table 1:

Table 1: $r_{bb'}$ at different neutron fluences and time periods after irradiation.

After irradiation (months)	$r_{bb'}[\Omega]$		
	$(1.1 \times 10^{13}n/cm^2)$	$(4.5 \times 10^{13}n/cm^2)$	$(1.1 \times 10^{14}n/cm^2)$
9.0	234.5	243.2	246.4
10.5	219.5	230.5	227.0
12.5	212.0	224.0	222.0

It can be seen that the values of $r_{bb'}$ decrease as a result of self annealing. After about 9 months, $r_{bb'}$ reaches the initial value (before irradiation) and after about one year, it becomes about 10% lower.

Considering that the quoted neutrons fluence was applied for a very short time, but that the expected experimental conditions will reach that level after 10 years of running, the results are

adequate. Furthermore, the experimental results show that the decrease of the $r_{bb'}$ values after irradiation is consistently observed, independent of the irradiation facility used.

In order to optimize the noise performance (in particular the $r_{bb'}$ maximum value) the overall system has to be analyzed.

4. RADIATION HARD CSP DESIGN STRATEGY

The designed CSP will satisfy the requirements of high-speed, low-noise and radiation hardness. It will combine a technology with a known behavior after irradiation and a design, able to reduce, compensate or take into account such radiation effects.

There is a trade-off between the noise of $r_{bb'}$ and the radiation hardness of the structure. The larger the area of the CSP input NPN, the lower $r_{bb'}$ becomes; also, the lower the current density is, the larger the reduction of β becomes after irradiation. The obtained results after irradiation, suggested to consider a current density of about $50\mu A$ per minimal area for the input NPN transistor. Setting the maximum bias current at $3mA$, $r_{bb'} \approx 20\Omega$ is expected, matching the detector at $C_D = 150pF$.

The key issue, in order to improve the radiation hardness, was found to be the choice of the folding device: the use of a PMOS (Fig. 4) implies an increase of threshold voltage (up to a few volts) for ionizing radiation damage resulting in a similar reduction of the output voltage swing. For this reason a V-PNP device will replace the P-MOS as a folding device [9]. V-PNP transistors (like NPN) are sensitive to neutron fluences: the V-PNP, when irradiated at $3 \times 10^{14}n/cm^2$, with a current of about $150\mu A$, has shown a reduction of current gain (β), from 100 to about 25 (Fig. 3). In this configuration, the current gain of the transistor is given by $\beta/(1 + \beta)$. This factor varies by about 3% when β decreases from 100 to 20. For this reason the large β variation is expected to produce a little effect on the CSP open loop gain. Extrapolation of the NPN gain degradation to a neutron fluence of $3 \times 10^{14}n/cm^2$, leads to a reduction of about 30% in β . This effect is obviously not important for the CSP open loop gain and results in a slight shift of the output bias voltage ($\Delta V_0 = 200mV$). The expected increase of noise is also negligible. For the foreseen operating condition of $C_D \sim 150pF$ and $\tau = 20$ ns, the increase of ENC is expected to be less than 5%, when $r_{bb'}$ is 20Ω and I_B degraded by 30%.

5. CONCLUSIONS

A characterization of the HF2CMOS monolithic process, after neutron irradiation, was made with the purpose of developing a very fast Charge Sensitive radiation-hardened Preamplifier (CSP). HF2CMOS discrete NPN and PNP transistors were irradiated at neutron fluences of up to $3 \times 10^{14} n/cm^2$.

The dynamic performance of NPN transistors after irradiation showed that the current gain decreased by about 30%. The degradation of PNP transistors lead to a decrease of current gain of less than 70%.

An experimental CSP version was equally irradiated. The noise performance was marginally affected. Self-annealing, by employing a novel measuring set-up, lead towards improved series noise performance.

The values of $r_{bb'}$ decreased with self annealing and reached the initial value (before irradiation) after about 9 months. Values, lower than the initial ones, were reached for longer periods of self-annealing. The series noise measurements were performed, employing a novel setup.

The increase of the input current, caused by the current gain decrease, contributes to a noise degradation of only 5%, when the right shaping time (20 ns) is used.

The obtained irradiation effects on HF2CMOS discrete components and CSPs, are being utilized for the design of a radiation hardened CSP.

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FIGURE CAPTIONS

- Fig. 1 Current gain change $\Delta\beta/\beta$ in % vs. the collector current (I_C) for a minimal area NPN, at $3 \times 10^{13} n/cm^2$ fluence.
- Fig. 2 Current gain change $\Delta\beta/\beta$ in % vs. the collector current (I_C) for a minimal area-lateral PNP transistor, irradiated at $3 \times 10^{13} n/cm^2$ fluence.
- Fig. 3 Current gain change $\Delta\beta/\beta$ in % vs. the collector current (I_C) for a minimal area Vertical Isolated PNP, at $3 \times 10^{14} n/cm^2$ fluence.
- Fig. 4 A simplified diagram of the monolithic CSP.
- Fig. 5 Set-up for noise measurements of the CSP. Main noise sources are included.
- Fig. 6 ENC vs. C_D for two RC-CR filters, with $\tau_1 = 100 ns$ and $\tau_2 = 200 ns$, respectively. The lines are to guide the eye.
- Fig. 7 Histogram of measured $r_{bb'}$ for 20 samples from two different wafers, (a) and (b).

Fig.1

Fig.2

Fig.3

Fig. 4

Fig. 5

Fig. 6

Fig. 7