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DATA SCANNER SYSTEM OF THE BELLE SILICON VERTEX DETECTOR

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Abstract

A data scanner system, which is a part of the front-end data acquisition system of the BELLE silicon vertex detector, makes an analog-to-digital conversion of preamplified signals from the detector and stores digitized data into local memory. The sequence control and buffer managing are performed by a software process of an on-board CPU. With this data scanner system, we can achieve the data taking with less than 10 % the dead time up to 800 Hz trigger rate.

I. INTRODUCTION

The BELLE detector is now being constructed at KEK in order to observe CP violation in the B meson decay. The B mesons are generated from $\Upsilon(4S)$ s created by asymmetric e^+e^- collisions at the KEK B-factory. For this purpose, an excellent vertex detector to tag B mesons is indispensable. The simplest way to tag B mesons is to identify their decay points with precision less than 100 μm .

An optimized way to achieve this high space resolution is to install a vertex detector with double-sided silicon micro-strip read-out. Figure 1 shows the r- ϕ view of the BELLE vertex detector(SVD) [1] together with the beam pipe. We have an octagonal configuration of two super layers. Each layer has two sub-layers, where double-sided silicon detector modules are installed.

Fig. 1 The cross section view of the BELLE SVD and beam pipe.

In our present design, the strip pitch of the junction side is 55 μm and the pitch of the ohmic one is variant from 75 to 250 μm . The radii of the inner and outer super layers are 27 mm and 48 mm, respectively. The effective widths are 25.6 mm and 44.8 mm for the inner and outer ones. The number of detector modules is 16 for both super layers. The aggregate number of read-out channels will be thus order of 100000.

The number of hit channels per trigger will be, however, 1000 on average, where only ten to twelve hits will be due to track signals. Considering this fact together with high trigger rate thanks to high beam currents, we applied a sparsified read-out mechanism at this stage, where only channels which give signals are read-out. With this mechanism at the pre-amplification, we could expect reduction of the read-out and data transfer time.

We must handle a signal always with its original channel number(tagging) owing to this zero suppression (sparsification) mechanism. The preamplifiers and the control circuit on a detector module will output the analog data and their channels. The main tasks of signal processing in the next(second) stage are, therefore, to do data formatting, Analog-to-Digital(AD) conversion of the signals and data buffering. Since we can not send analog data over long distance and we can not put the AD converters at the detector because of EMI and power consumption, we install another electronics board, which is called a data scanner, 1 m away from the detector in order to do the second level processing.

Main design idea of the data scanner is to install a CPU on board. As whole control of the signal processing is initiated by a software program, we can avoid a complicated hardware logic from the data scanner. Moreover by installing a buffering mechanism in the software process, the dead time will be expected to be greatly diminished. In the following sections, we describe the hardware and software aspects of the data scanner, and the system performance measured using the prototype board recently constructed.

II. DATA SCANNER SYSTEM

On a detector module, we have four read-out blocks at both plane of both edge. A detector module of the inner(outer) super layer has four(seven) preamplifiers on each read-out section. One preamplifier has 128 input channels. Hence

total 16 and 28 preamplifiers per detector module for inner and outer layers, respectively. One(two) data scanner board cover(s) for a detector module of the inner(outer) layer. Total 48 data scanners will be employed in the SVD DAQ system. The data from each data scanner are eventually assembled in the next(third) level data processing.

The data scanner will not be installed in the vicinity of the detector, but located about 1 m away as discussed in the last section to maintain EMI immunity and to reduce handshake latency.

A. Hardware system

The building blocks of the hardware system of the data scanner are Transputer T805(30MHz) as CPU and its 128K memory, FIFO memory, two AD converters, custom VLSI sequencer, custom VLSI data receiver and ancillary logic circuit. A block diagram of the hardware system is shown in Fig.2.

Fig. 2 The Block diagram of the data scanner system

A pair of dedicated custom VLSIs transmits and receives hit data information(analog signals and digital data of hit channels) between a detector module and data scanner. A custom VLSI called control-A chip makes data formatting in ten stage sequence. It picks up a module and chip identification code and put them into FIFO, puts channel number received from the detector module as well as digitized data after AD conversion also into FIFO. One hit information is wrapped in a packet of eight bytes. The sequence of both the data sparcification and data formatting are driven by a 16 MHz clock.

The Transputer T805 initiates control-A chip by setting a flag(DATA-BEGIN) into a control-A control and status register(CSR). When control-A finishes its all sequence, it sets an another flag called DATA-END. The Transputer makes a DMA transfer from FIFO to its internal memory by detecting this flag. Actually an interrupt to a Transputer process is occurred by DATA-END and Event Trigger flags. Besides these flags, data abort and overflow flag will cause the interrupt. Since a Transputer recognizes only one interrupt, one must analyze the source of the interrupt by examining the bit pattern of the control-A CSR in a software process. After completion of the DMA data transfer into the internal memory where a software process

manages the buffer access, the Transputer issues a reset signal for the preamplifiers in order to restore the base line and moves the hardware to wait for the next trigger.

Two AD converters are used because each hit channel sends two analog data of before and after trigger, which comes a sampling scheme for noise filtering of the preamplifier. Detailed design idea of the hardware system of the data scanner will be found in [2], [3].

B. Software System

As discussed earlier in the last subsection, the most characteristic aspect of the hardware design is to introduce a Transputer for whole control of the board function. The characteristics of the Transputer will be summarized as following three points:

- a Transputer has four embedded serial interfaces called INMOS link(20Mbps) for data communication, one can construct any topological Transputer network using these interfaces and design a flexible parallel and/or distributed system with multiple Transputers,
- using serial data transfer nature of the INMOS link, we can reduce the number of cables output from a data scanner as well as the space necessary for cabling,
- a complicated parallel process in a Transputer can be constructed relatively easily using C or a dedicated Transputer language called OCCAM, since one need not to introduce an operating system for this purpose, one can implement an efficient and simple software system on a CPU with small overhead.

The present software system of the data scanner consists of basically two parallel processes. One is a command and interrupt handler and the other one is a buffer manager. The command and interrupt handler waits two different kinds of signals, which are a software command(DAQ GO/STOP) issued by the central data acquisition system and an hardware interrupt signal generated by the control-A chip. Once an interrupt by an event trigger is occurred, the Transputer notifies the control chip to start the data formatting sequence. The state and transition diagram of this command and interrupt analysis chain is shown in Fig.3. There are several states introduced in the diagram. The main states are, however, *Active*, *Interrupt handle*, *Data Accept* and *Data transfer*. A state transition between *Inactive* and *Active* is performed by a command given to this data scanner from the central DAQ control system. The *Interrupt handle* state is excited by an interrupt to the Transputer through the event channel [4]. In this state an analysis for CSR of the control-A chip is done. According to a bit pattern which indicates the source of the interrupt, transition to one among several states will be made. If the interrupt is an event trigger(TRIGGER), then the *Data Accept* will be selected and a CSR flag DATABEGIN is set in this state. This DATABEGIN is the signal to initiate the control-A chip for its data formatting sequence. Normally after this DATABEGIN, we expect to receive another interrupt due to the DATAEND flag of the CSR. The DATAEND flag notifies the Transputer the end of whole sequence of the control-A chip. After data transfer to the

buffer manager in the state of *Data Transfer*, the system goes down to *Active* to wait for another interrupt. Therefore the Transputer should react to two interrupts for one event Trigger in a standard data processing. One is due to the TRIGGER interrupt and one due to DATAEND interrupt.

Fig. 3 A state and transition diagram for the interrupt handling process

The buffer manager process applied in the system is a simple FIFO type memory management, which we have adopted a method given by R.Cok [5]. The buffer manager firstly runs solely to fetch data from then event buffer and prepare to output. Then the process branches into two sub-processes. One sub-process called producer put data into an event buffer from actual FIFO memory with a DMA transfer while the other one called consumer sends data which have been extracted from the buffer in advance. This rather involved scheme comes from a restriction of Transputer software system that two parallel processes can not share the parameters [6]. The buffer parameters should be kept in a single process.

III. SYSTEM PERFORMANCE

In this chapter performance of the system with the prototype data scanner board is discussed. The hardware components we have used for the measurement in this study are a prototype data scanner board, a detector module digital emulator, a Transputer and a workstation. The

component setup is shown in Fig. 4.

Fig. 4 A hardware setup of the study for a prototype data scanner board and detector module digital emulator

The workstation is used as a server for the Transputer on the data scanner and so called root Transputer, which is connected to the workstation via INMOS B300 gatebox. The root Transputer relays commands(DAQ-GO/STOP) from the work station to the data scanner. It also receives data sent by the buffer manager in the data scanner Transputer. The root Transputer sends monitoring information to the work station time to time during a run. The gatebox works as a router to transmit INMOS link protocols on ethernet cables.

Although the present data scanner board is called prototype, the global design and the devices used are almost final ones. Main difference is only its dimension. The speed and timing optimization might be also needed. Though it is almost final one, we get an evaluation for the system performance with this prototype.

The main purpose for the construction of the prototype is to check the stability of the ADC system and functionality of the digital circuit in conjunction with the custom VLSIs. The detector module digital emulator has constructed to give facility only for these check items. The analog signals which the preamplifiers output are generated in the DACs of the data scanner and eventually returned to the data scanner. These signals are simply passed over the emulator. Number of hit channels is controlled currently as 28 in the emulator board. In the present setup, hence, the data scanner always gets the same analog values from 28 channels with every trigger, whereas the scanner has its full functionality.

No obvious modification for the control software has been made either. In the present software system for the data scanner Transputer, however, we have added a process to generate the interrupts to the control-A chip besides two concurrently running processes of the interrupt handler and the buffer manager. The third process generates interrupts randomly according to exponential distribution with a given average trigger rate. The CSR of the control-A has a bit for the forced trigger. If the software sets this bit, an interrupt is generated immediately and normal sequence for the data formatting is started in the control-A

chip.

We have discussed so far the data scanner itself. The data acquisition system of the SVD has another(third) signal processing system. Since the performance of the third system has not yet quite known, we have introduced a parameter for the processing time in this system and denoted it as T_{proc} . In the current configuration, the data scanner and the root Transputer which receives data from the data scanner is connected with 1.7 MByte/sec standard INMOS link. The time for the data transfer needed with this link is about 120 μ sec for data transfer of 28 hits. T_{proc} means that we may consume 120 μ sec + T_{proc} for communication with the third signal processing element.

The performance of the data scanner itself is greatly influenced with T_{proc} . Figure 5 shows this effect. In this figure the live time fraction of the data scanner is plotted with the trigger rate condition of 200, 500 and 1 KHz as a function of T_{proc} . Our definition of the live time fraction ϵ is defined as $\epsilon = \frac{1}{1+f\tau}$ where f is the trigger rate and τ time needed to process one trigger. We have measured τ and calculated the live time according to the equation. While in lower trigger rates the live time is more than 90 % even T_{proc} exceeds 1 msec, the live time becomes less than 80 % already when T_{proc} is about 700 μ sec for 1 KHz trigger rate. We have an internal guide for the design of a data acquisition system for the BELLE sub-detector components. It requires to have live time greater than 90 % when the trigger rate is 500 Hz. Hence we have to keep anyway T_{proc} less than 1 msec.

Fig. 5 Live time fraction versus Data Transfer time(T_{proc}) in μ sec

In Fig. 6 another dependence of the live time fraction is shown, which plots it in terms of the trigger rate with three situation of T_{proc} . If we can keep T_{proc} less than or equal to 1 msec, we can keep live time fraction 90 % until 800 Hz trigger rate. However, if T_{proc} is 2 msec, the live time fraction is reduced to about 80 % at 400 Hz. Hence in order to extract the full performance of the data scanner,

it is important to keep T_{proc} less than 1 msec.

Fig. 6 Live time fraction versus Trigger rate

The data shown so far have been accessed with the buffer depth of the buffer manager 16. We have examined this buffer depth dependence of the live time with four T_{proc} case. In Fig. 7 the live time fraction is plotted as the buffer depth varied from 1 to 64.

Fig. 7 Live time fraction versus Buffer Depth

The trigger rate has been fixed as 800 Hz. We can find that an effect to gain the live time fraction with increasing the buffer depth is more evidently demonstrated when T_{proc} becomes larger, although the effect will be stabilized anyway if the buffer depth is greater than 16.

IV. SUMMARY

A prototype of the data scanner has been constructed. The data scanner makes data formatting and Analog-to-Digital conversion of the preamplified data of the BELLE silicon vertex detector and sends them to the local event builder system after data buffering. We have designed to emplace a CPU on the data scanner in order to initiate the data formatting sequence and data buffering. We have intended to use buffering mechanism in the data scanner for reducing the dead time which might be due to data transfer for long

distance. With this design we could simplify the hardware configuration.

Although we have not yet a clear idea about the time duration necessary for the data transfer from the data scanner to the next signal processing stage, we could achieve live time fraction greater than 90 % with trigger rate up to about 800 Hz if this time duration is less than 1 msec. The 1 msec estimation is longer than time needed to transfer over 1000 m with optical fibers [7]. Alternatively saying, we can endure the transfer speed 0.2 MByte/sec between the data scanner and the next stage if this time duration is used only for the serial link communication. Thus this time must be considered as the worst case. The buffer manager system was found to improve the live time fraction about 10 % when the trigger rate is 800 Hz and the time duration in the next stage is greater than 0.8 msec. If we can construct the next level processing system with the time duration less than 1 msec for process of the signal from a data scanner, we can conclude that the present system passes our self requirement of the live time fraction more than 90 % at trigger rate 500 Hz.

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